ROD HW status

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ROD firmware design

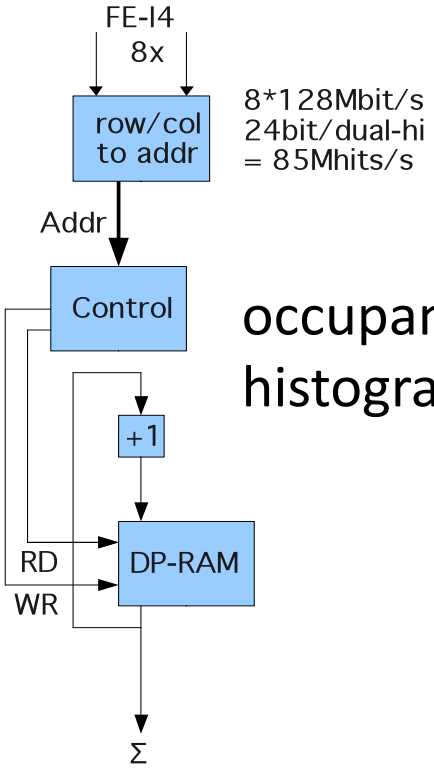
The main goals are:

- to re-use as much of the available VHDL+C code as possible → available code simulation in progress

- to build a VHDL testbench of the whole ROD system that can be simulated with Modelsim (including also PowerPC)

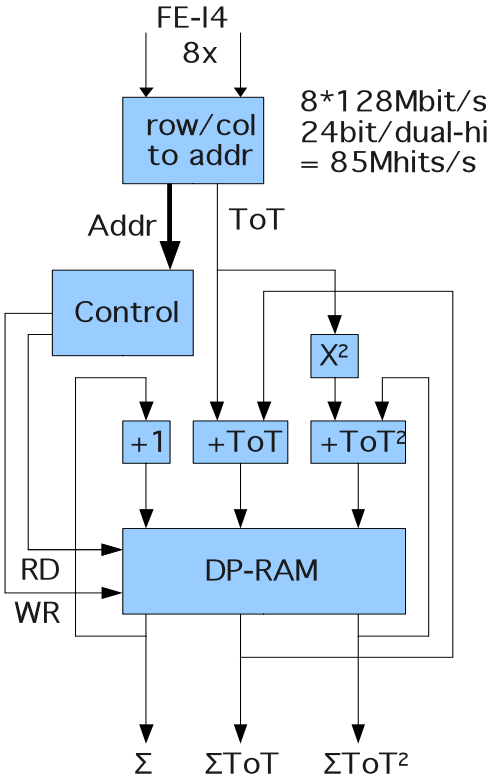
HISTOGRAMMING

- Histograms for **occupancy**, **TOT** and **TOT²**
- All processing of histograms is outsourced to a PC farm (Mannheim)
- Easy environment w.r.t. embedded processors

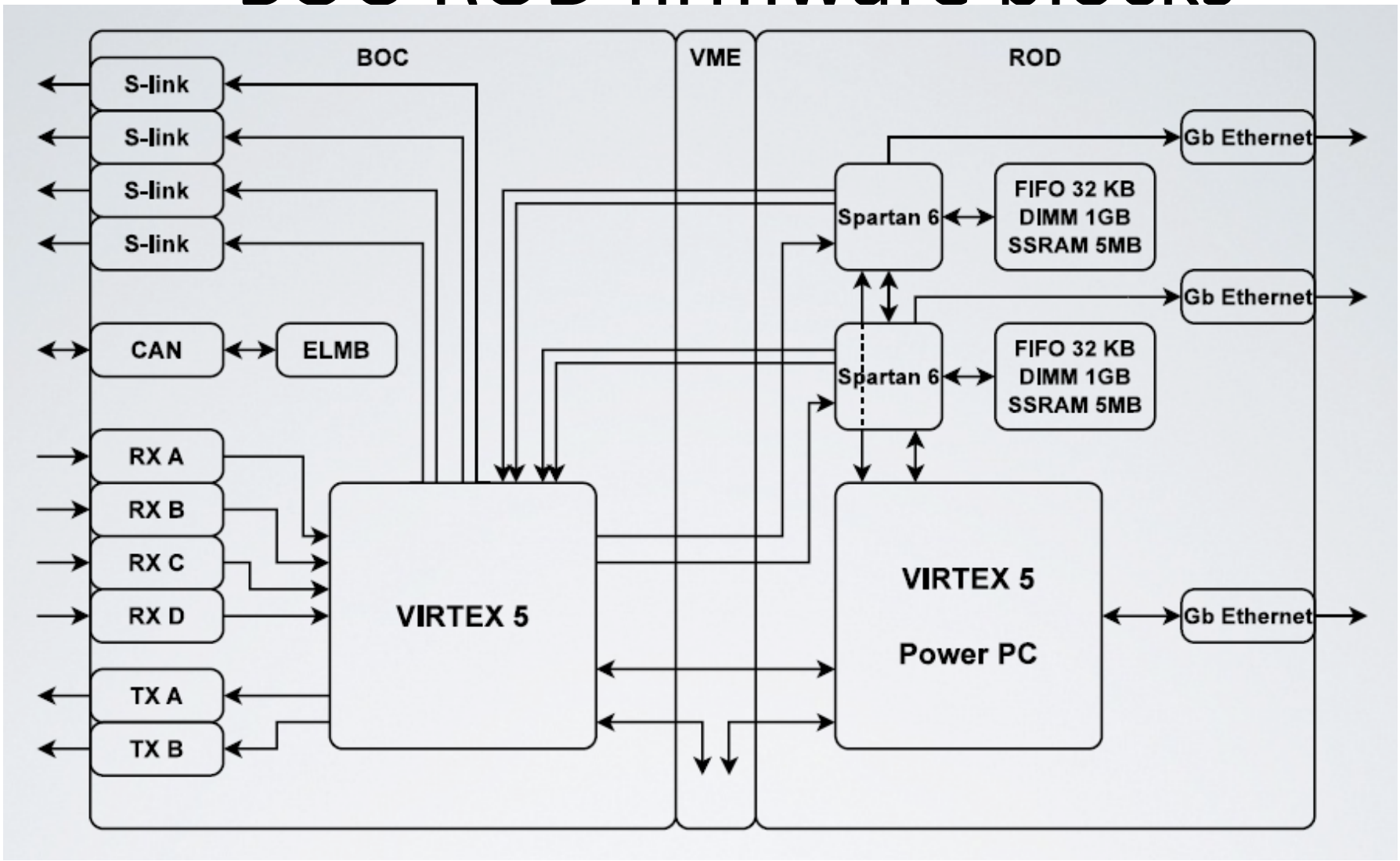


occupancy
histogramming

occupancy
+ ToT + ToT²
histogramming

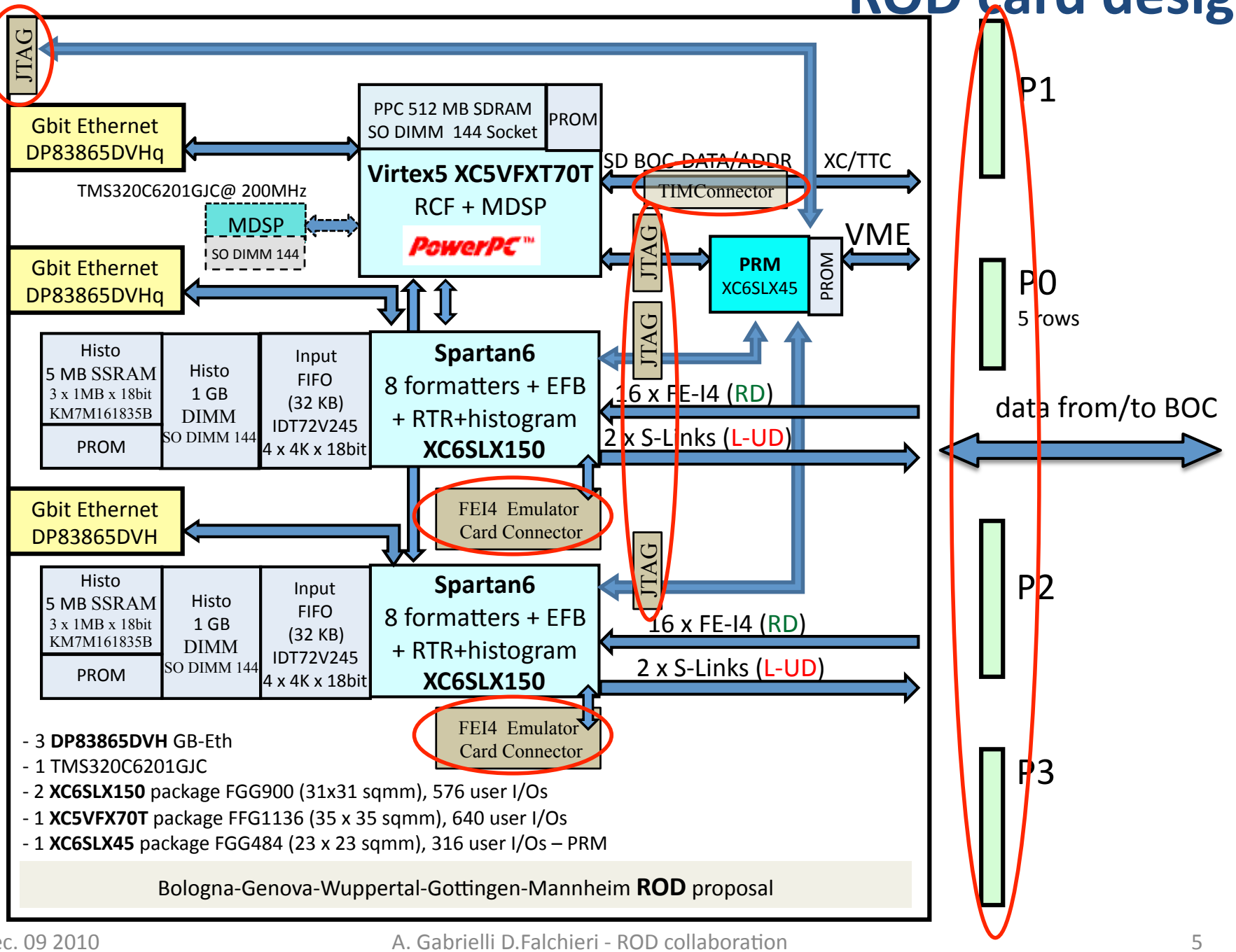


BOC-ROD firmware blocks

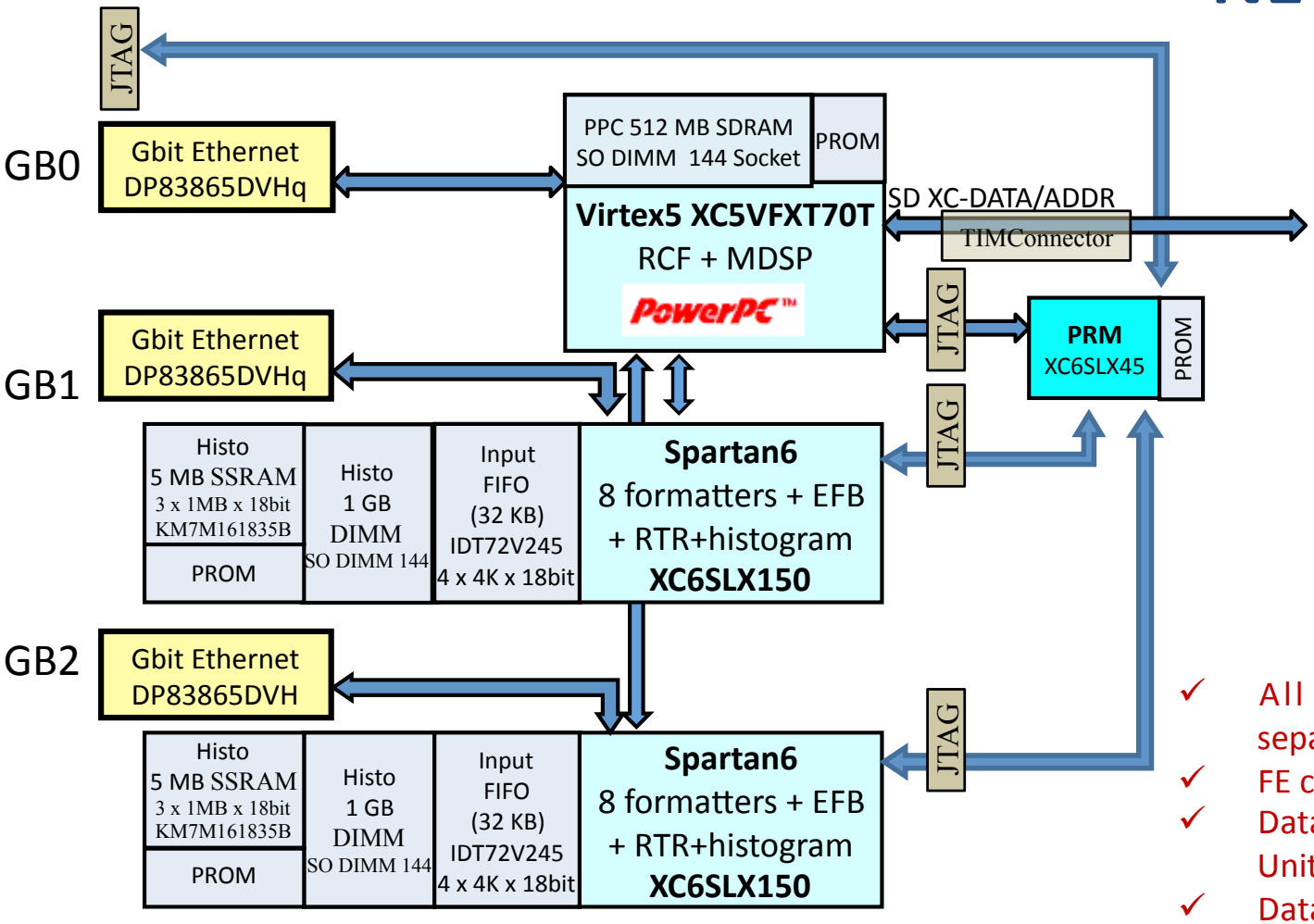


J. Dopke and A. Gabrielli at TWEPP 2010

ROD card design



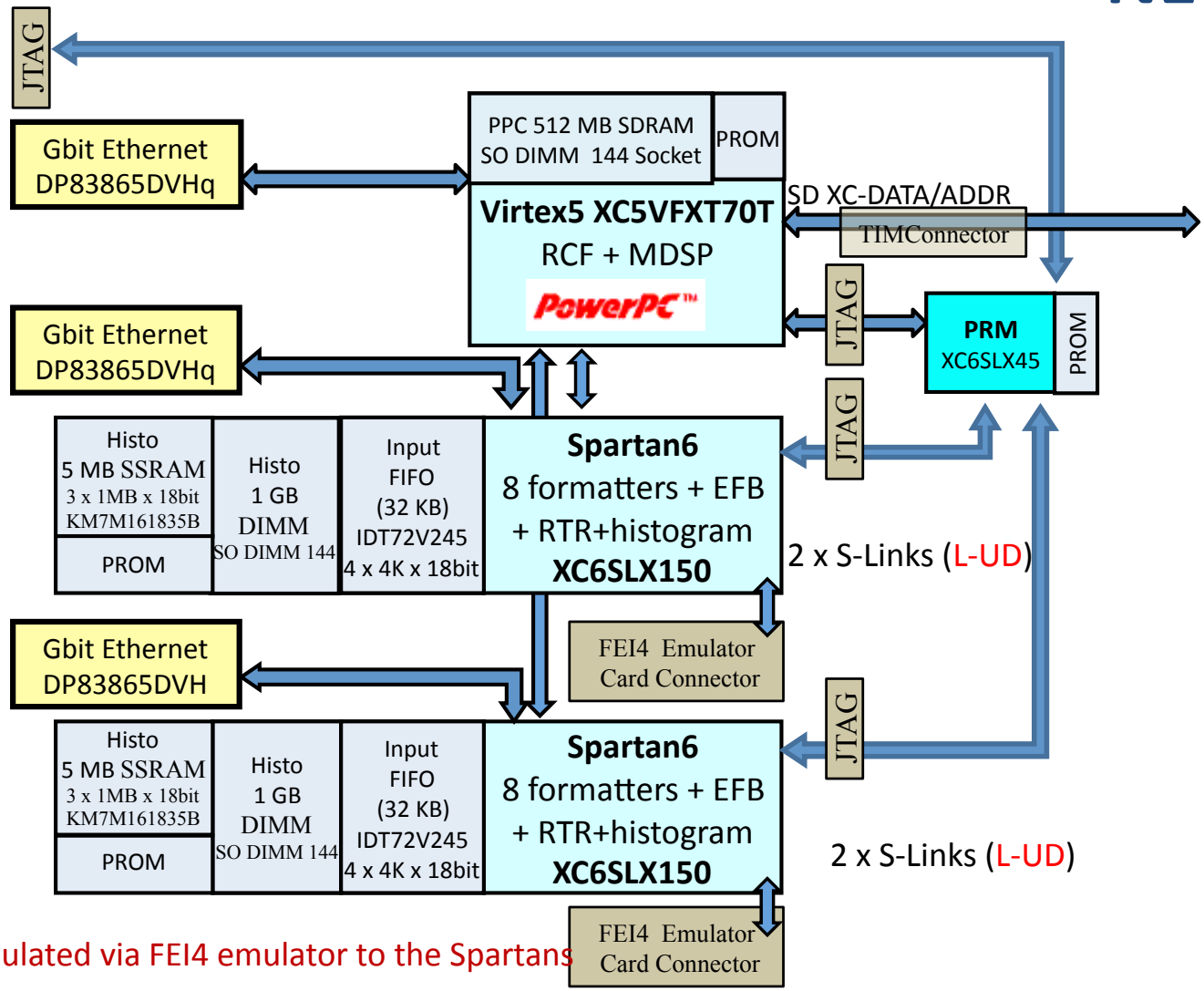
NEW FEATURE



- ✓ All devices programmed separately via JTAG connectors
- ✓ FE commands passed via GB0
- ✓ Data emulated via Pattern-Units into the Spartans
- ✓ Data Taken and Calibration output via GB1/2 from the Spartans

Mode 1: Test without VME, all via GB-Eth

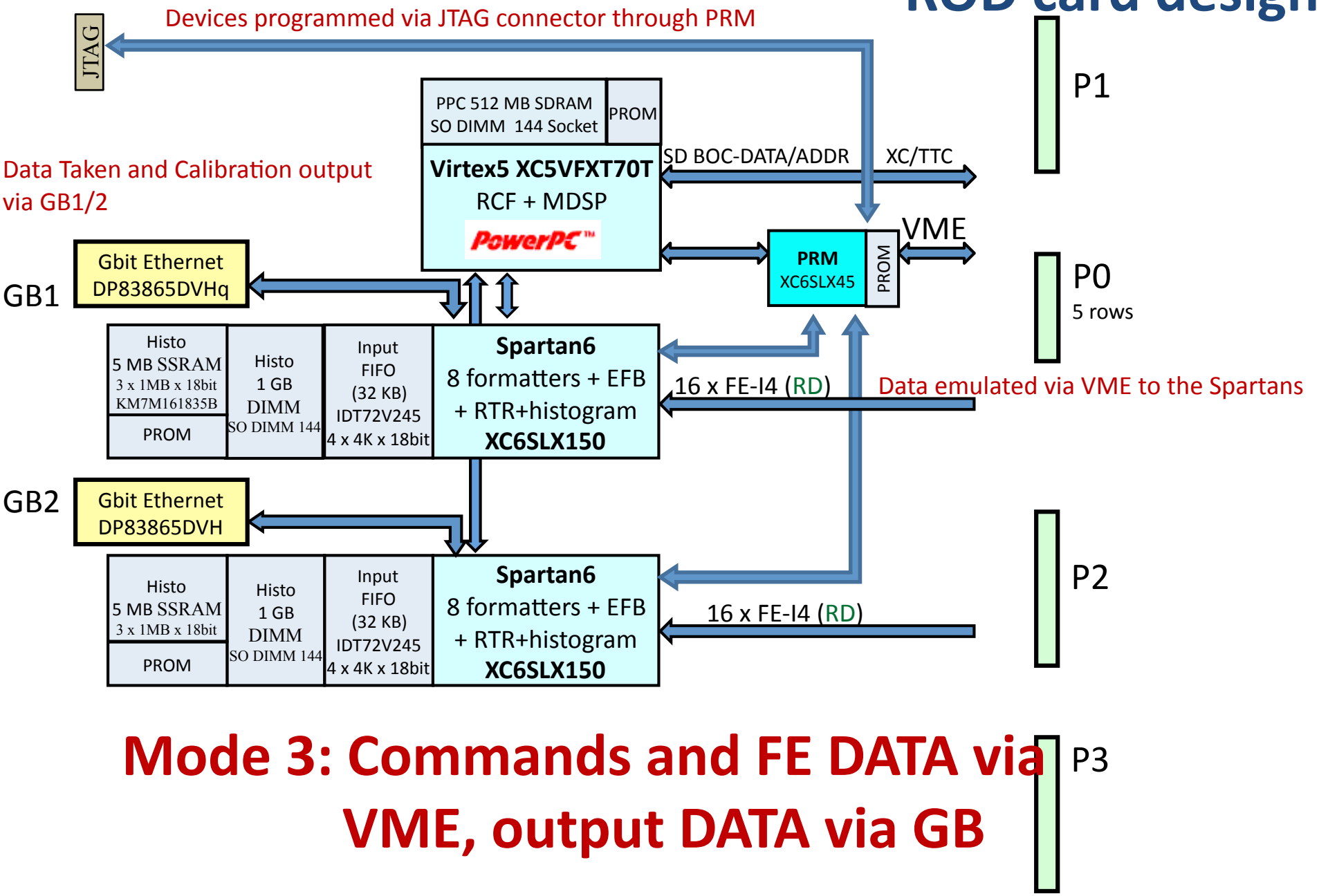
NEW FEATURE



Data emulated via FEI4 emulator to the Spartans

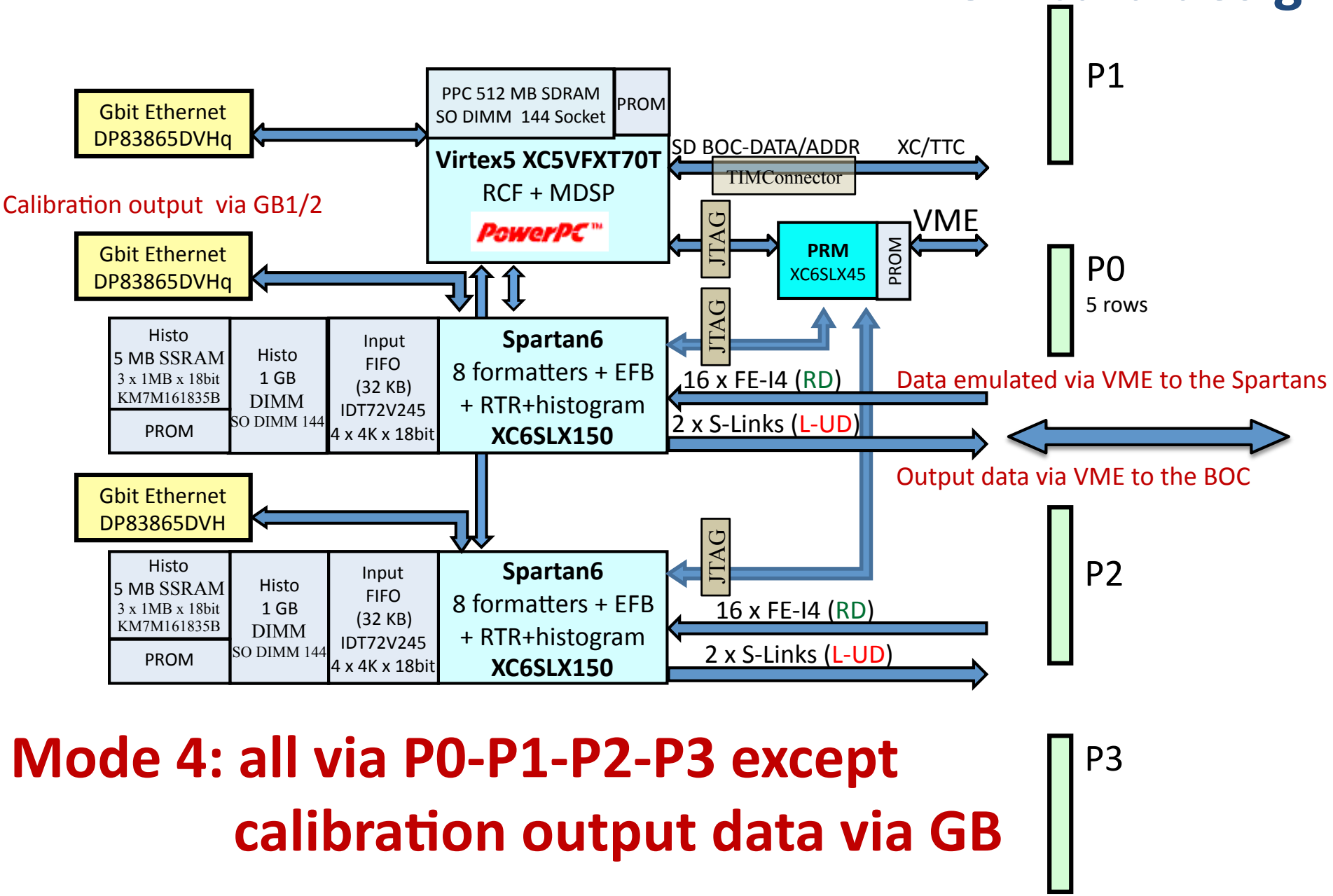
Mode 2: NO VME, FE-I4 emulator card compatibility (tests)

ROD card design



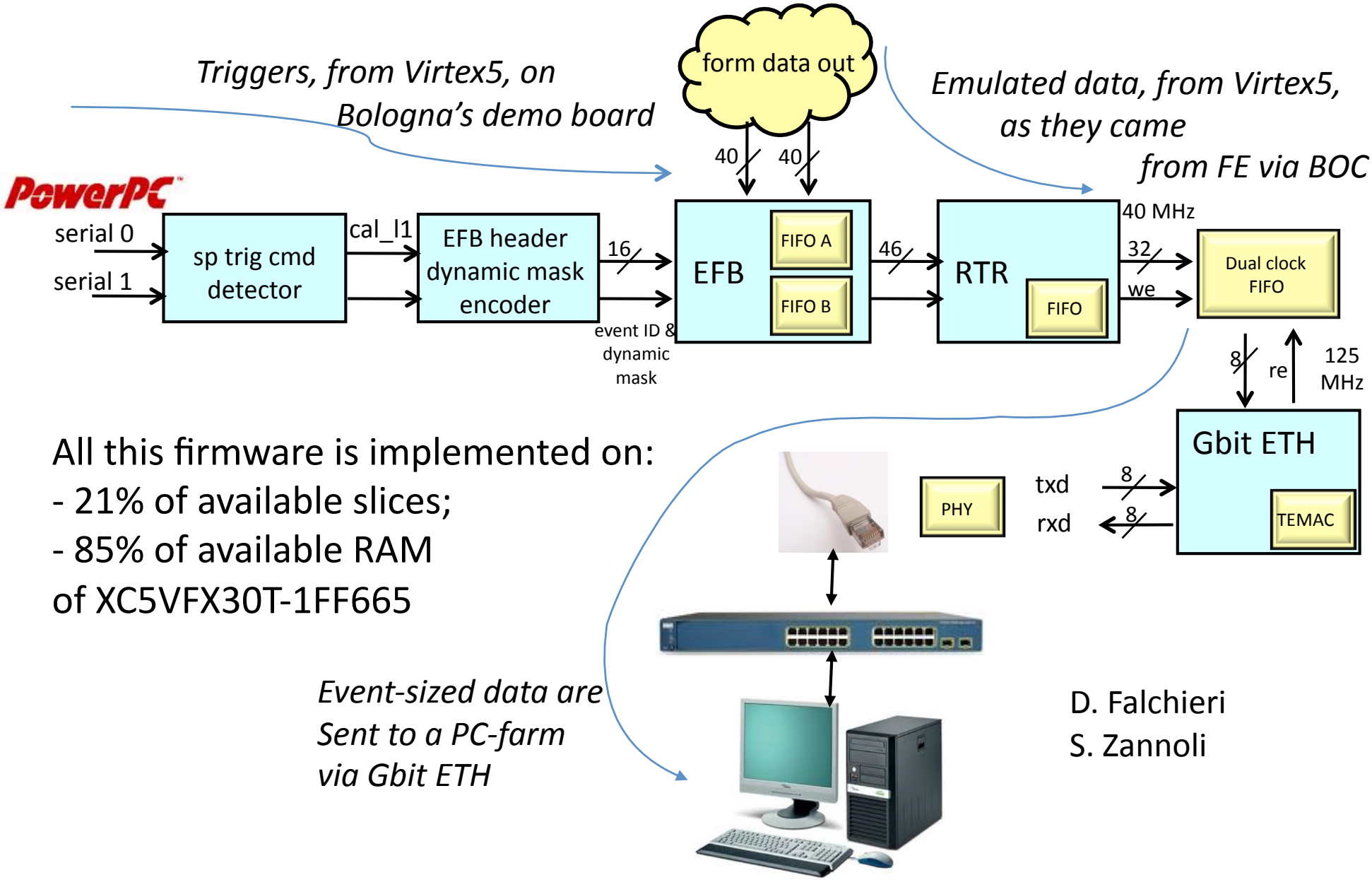
Mode 3: Commands and FE DATA via VME, output DATA via GB

ROD card design



Mode 4: all via P0-P1-P2-P3 except calibration output data via GB

About to be tested on the VIRTEX5 demo board in BO



All this firmware is implemented on:
- 21% of available slices;
- 85% of available RAM

of XC5VFX30T-1FF665

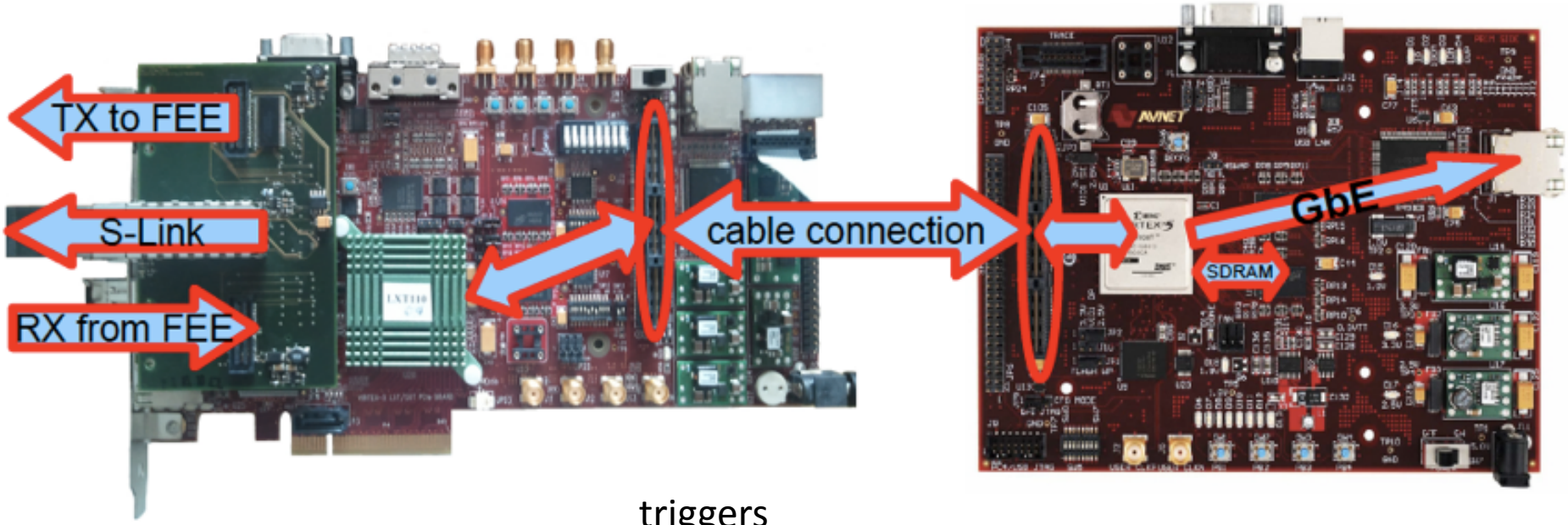
Event-sized data are Sent to a PC-farm via Gbit ETH

D. Falchieri
S. Zannoli

BOC-ROD test boards

J. Dopke and N. Schroer
Wuppertal/Mannheim

D. Falchieri and *S. Zannoli*
Bologna



triggers

STEP 1

Data from FE

STEP 2

Events ROD-to-BOC

STEP3

Time Plan

- Test on BOC-ROD system by early 2011 using the XILINX demo-boards (Bologna-Wuppertal)
- ROD schematic closure is ongoing (feedbacks from LNBL, Wuppertal and Mannheim), then layout design can start

- Two Bologna's VME-based 64x CRATEsBOC-ROD & DAQ systems foreseen (Robin cards, crates, TIM modules ordered)
  - One at CERN, already present
  - One in Bologna
- 2 ROD board prototypes – *one-channel demonstrator* – by March/April 2011

- **Time-Plan compatibility with 2013/14 shutdown depending on man-power and support available**