TOF manutenzione straordinaria
TRM 2 plans

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The context

- ✓ see Andreas's presentation: short version: 50 TRMs "off"
- ✓ some of them repairable, some of them not
- ✓ access extremely difficult
- ✓ need to know failure analysis
- ✓ 25 spares available

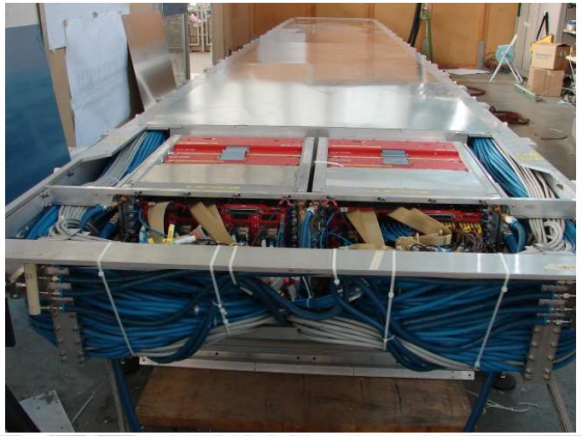
- ➢ TRM-1 IMPOSSIBLE to be produced: no FPGA, the HPTDC problem
- ➢ for a TRM-2 not a full production (684) but a production for having enough spares(100)

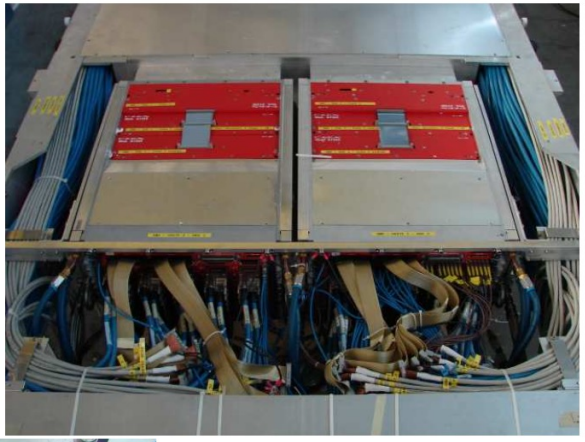
- ❑ TRM 2 also good "gym" opportunity as part of generation handover
- ❑ synergy with AIDA Innova

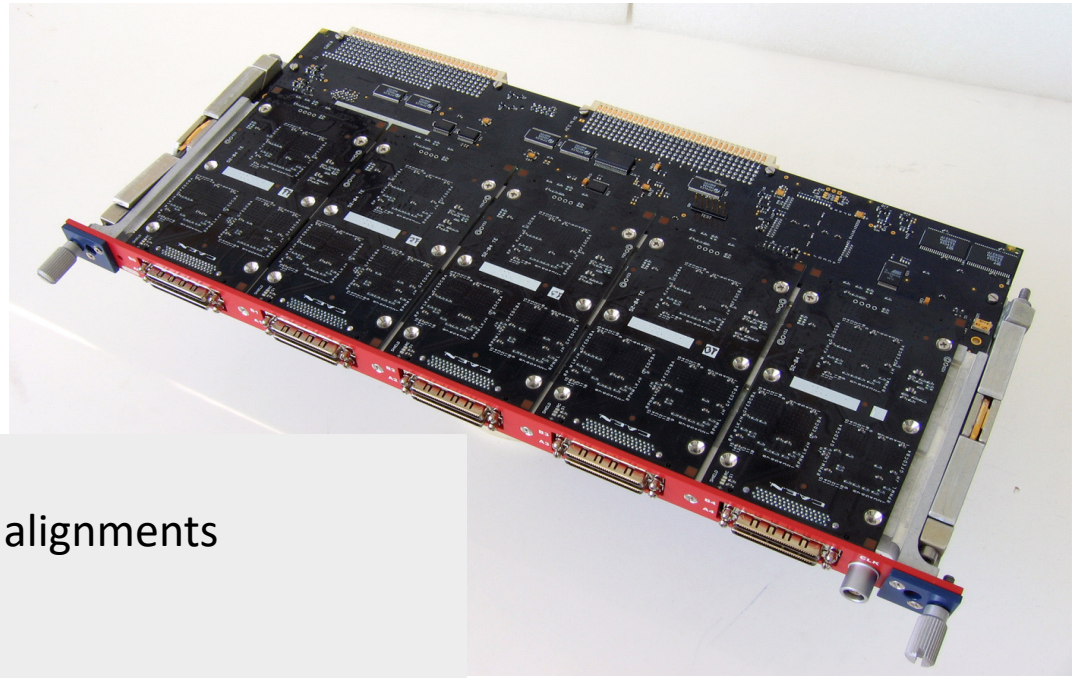
Task 7.2.1: MRPCs for fast timing

technology state-of-the-art @ 2000 (more or less): CMOS 0.25 um HPTDC (8 channels @ 25 ps)
produced in 2006-2008
FPGA: Actel APA750 (Flash based, requires special programming voltages)

1 W / HPTDC → 30 W @ 3.3V → 10 A /card

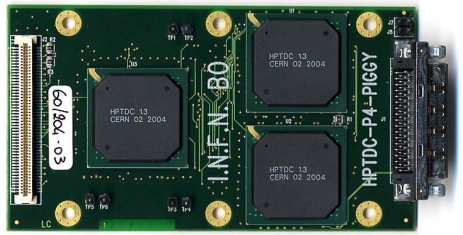




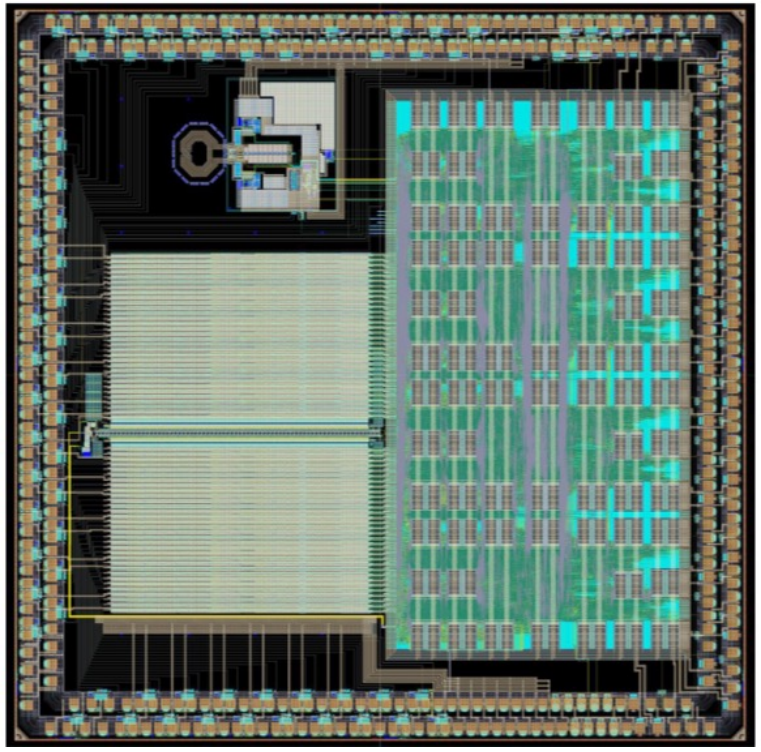


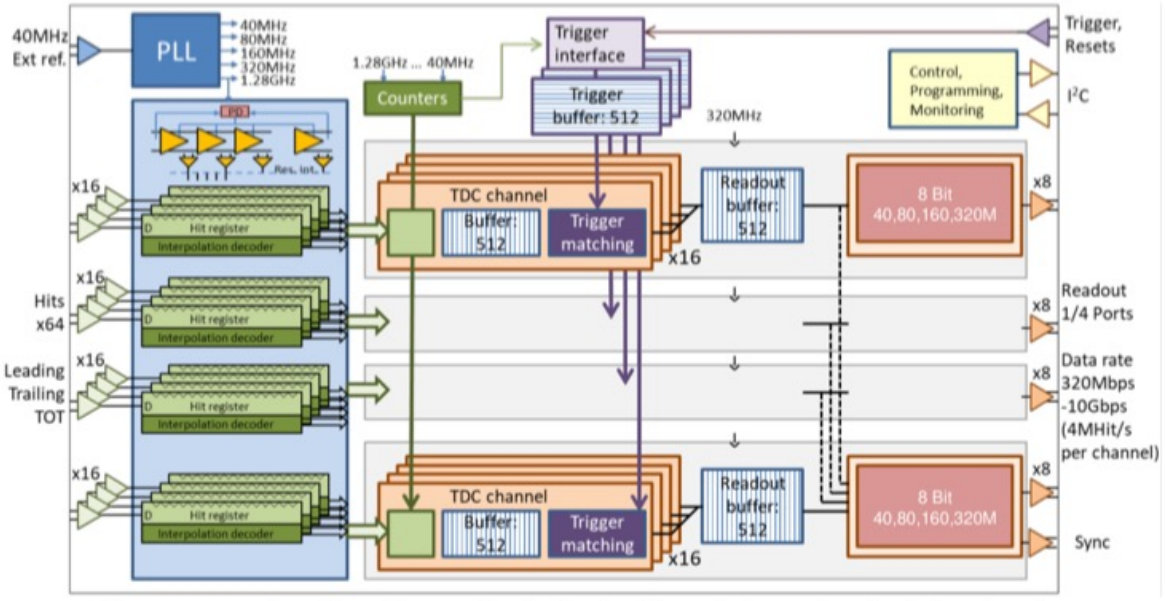
Very custom:

- non standard VME connector alignments
- 6Ux9U
- water cooled
- central aluminium bar
- front panel connectors for Amphenol cables (VHDCI)
- front panel connector for clock (Fisher tri-polar)
- custom bus on P2



picoTDC: context





natural HPTDC successor, similar architecture but... 20 years later:

- 250 nm → 65 nm
- 8 channels → 64 channels
- 1 W/8 ch → 0.85 W/64 ch
- 25 ps LSB → 3/12 ps LSB

Power Domains

All power domains should be supplied with 1.2V typical.

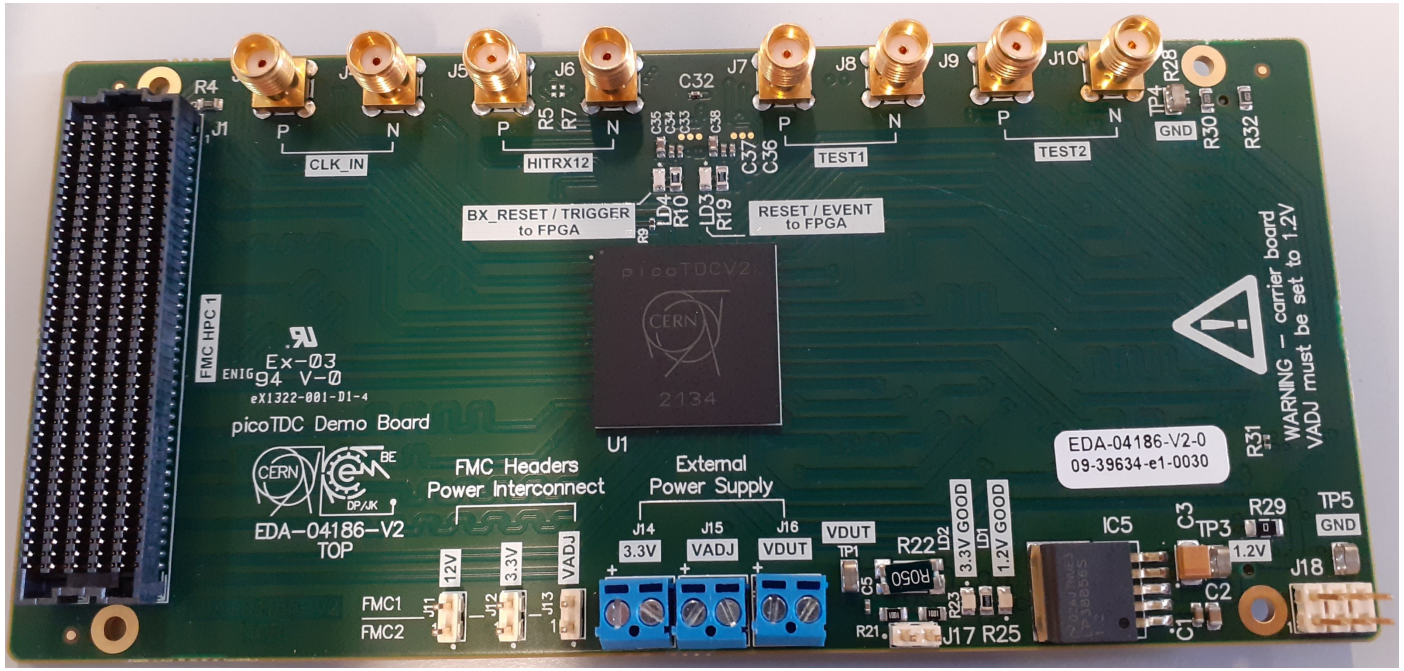
Power Domain	#Pads GND	#Pads VDD	Power [mW] High Resolution	Power [mW] Low Resolution	Power [mW] Low Res., 32 Channels
PLL	9	9	50	50	50
DLL	9	9	50	50	50
Timing Macro	31	29	700	250	150
Digital	26	25	500	500	300

https://espace.cern.ch/PicoTDC/_layouts/15/start.aspx#/SitePages/Home.aspx

picoTDC @ INFN – BO (I)

picoTDC demo board

64 channels



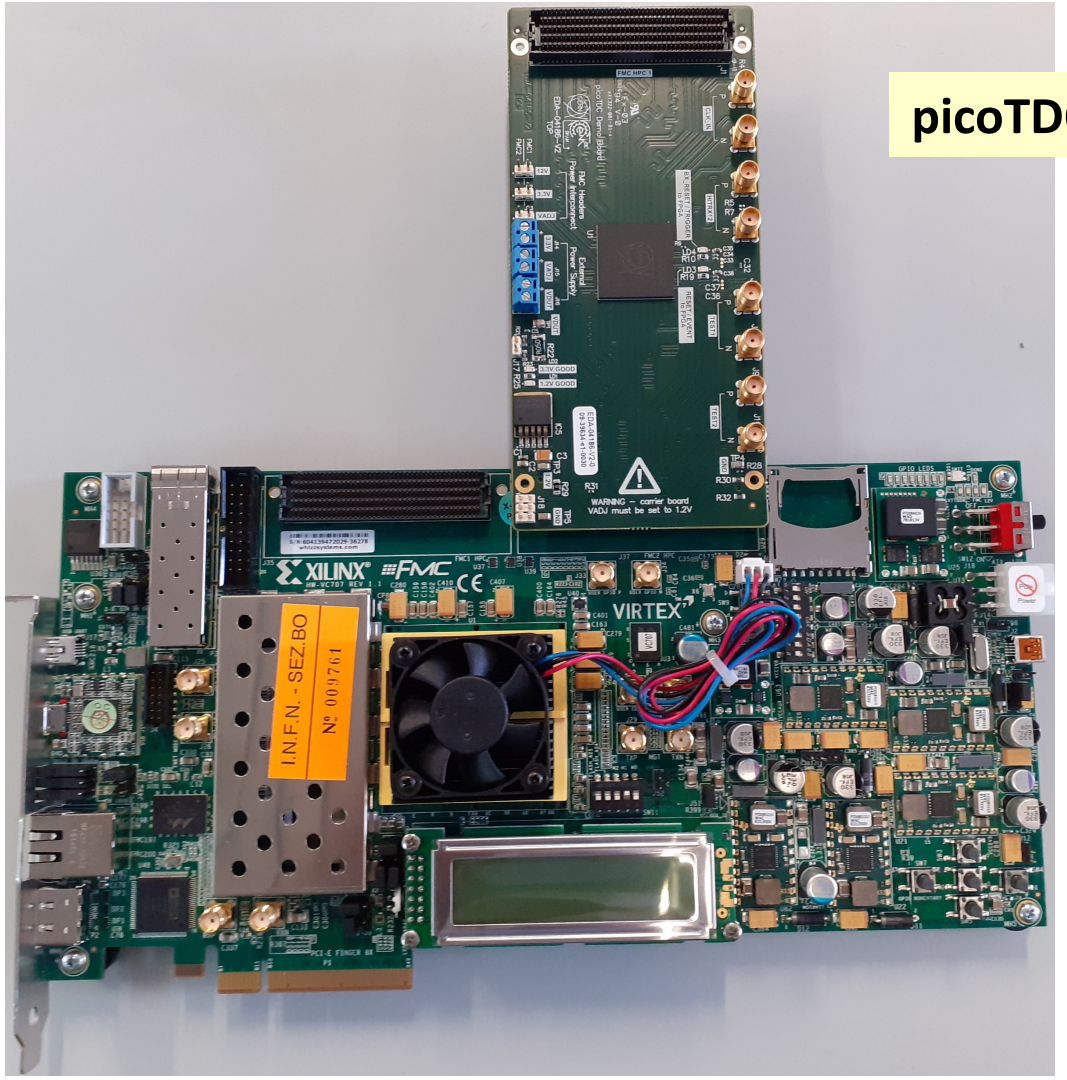
data to FPGA

A pair of these picoTDC demo boards are now finally in Bologna (since beginning of June 2022!)
in order to begin tests with the picoTDC ASIC (we also have 10 packaged picoTDC chips)

picoTDC @ INFN – BO (II)

- The first step is to control and readout the picoTDC via the FPGA using the **Ipbus** software
- Target → July/August 2022

1 Gbps ETH



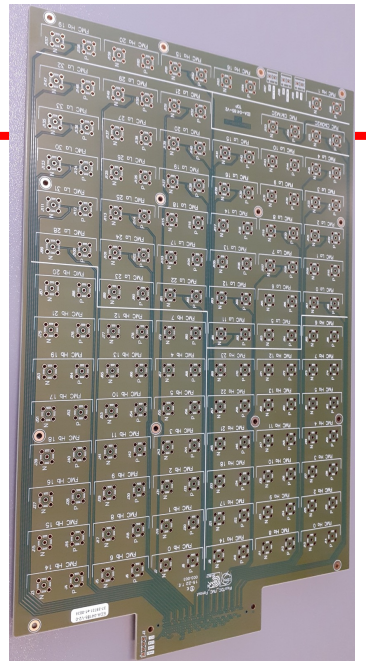
picoTDC demo board

VC707 (FPGA board)

picoTDC @ INFN – BO (III)

ALICE

FMC fanout board



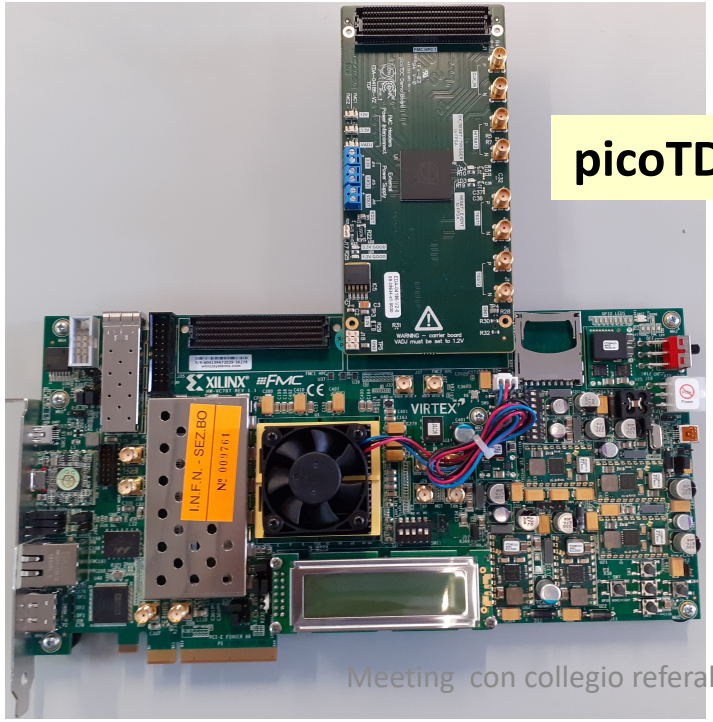
Via the FMC fanout board and the instruments, we will repeat qualification tests for picoTDC

Lab instruments available

Colby dual electromagnetic "**trombone**" CPDL-200A with MT-100A microterminal

Berkeley Nucleonics: Model 745T **Femtosecond Digital Delays** with 5 ps jitter

SRS **Clock Generator** - CG635 2 GHz



picoTDC demo board

1 Gbps ETH

VC707 (FPGA board)

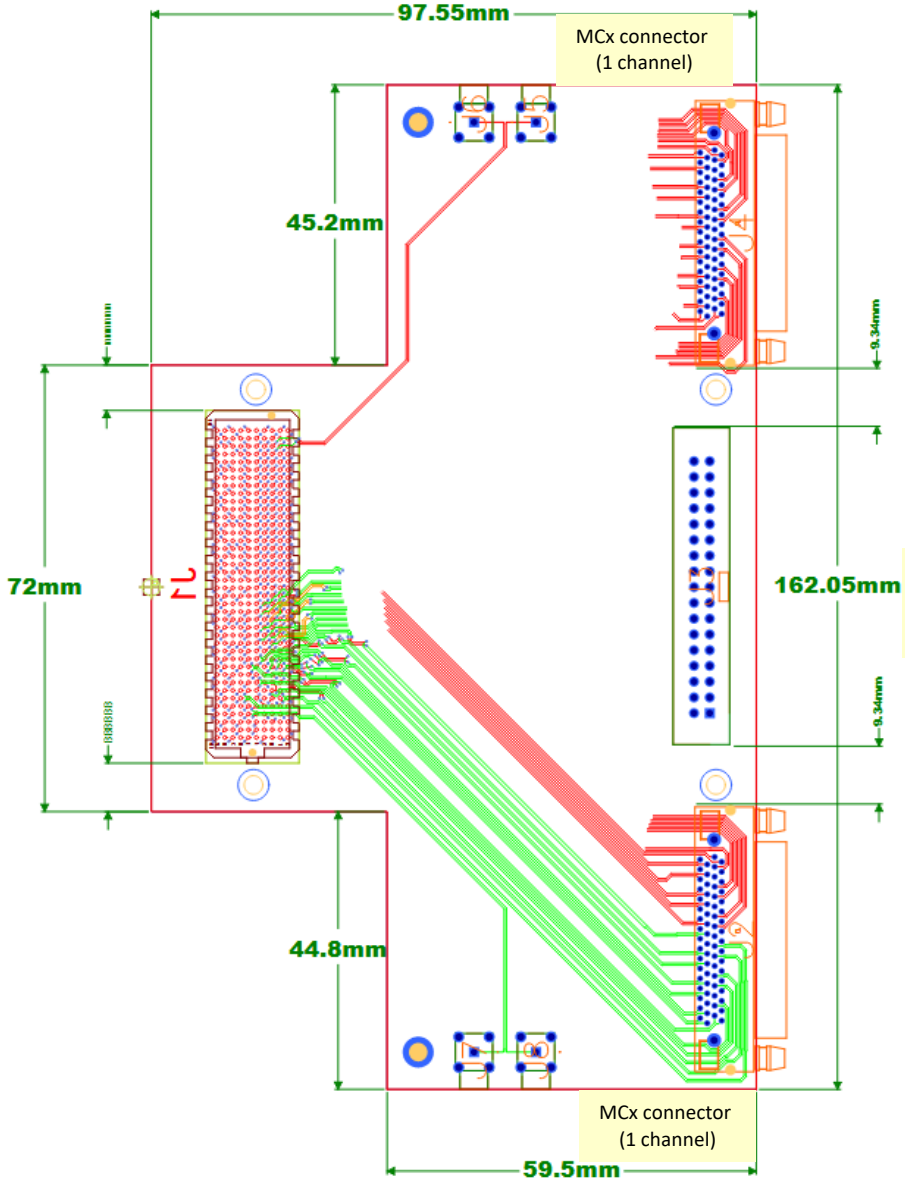
picoTDC @ INFN – BO (IV) → towards TRM2

adapter board

In the meanwhile, an adapter board is being designed.
It allows to route the 64 channels to the picoTDC to 3 types of connectors:

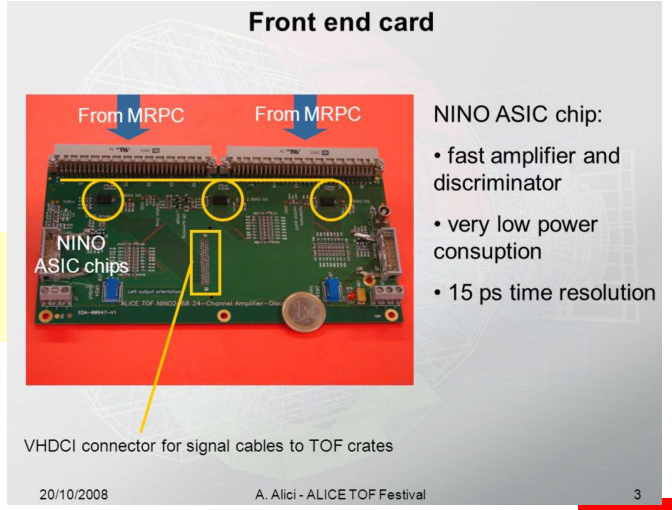
- VHDCI 68 pin
- dual in line
- MCx

We plan to have this board built and tested by the end of July 2022



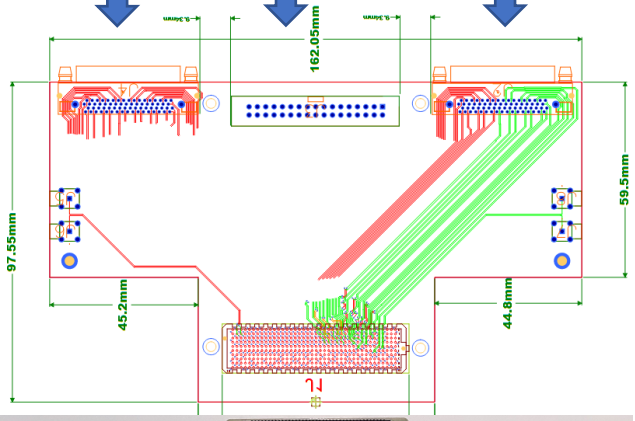
VHDCI connector
(24 channels)

dual in line connector
(14 channels)



picoTDC @ INFN – BO (V) → towards TRM2

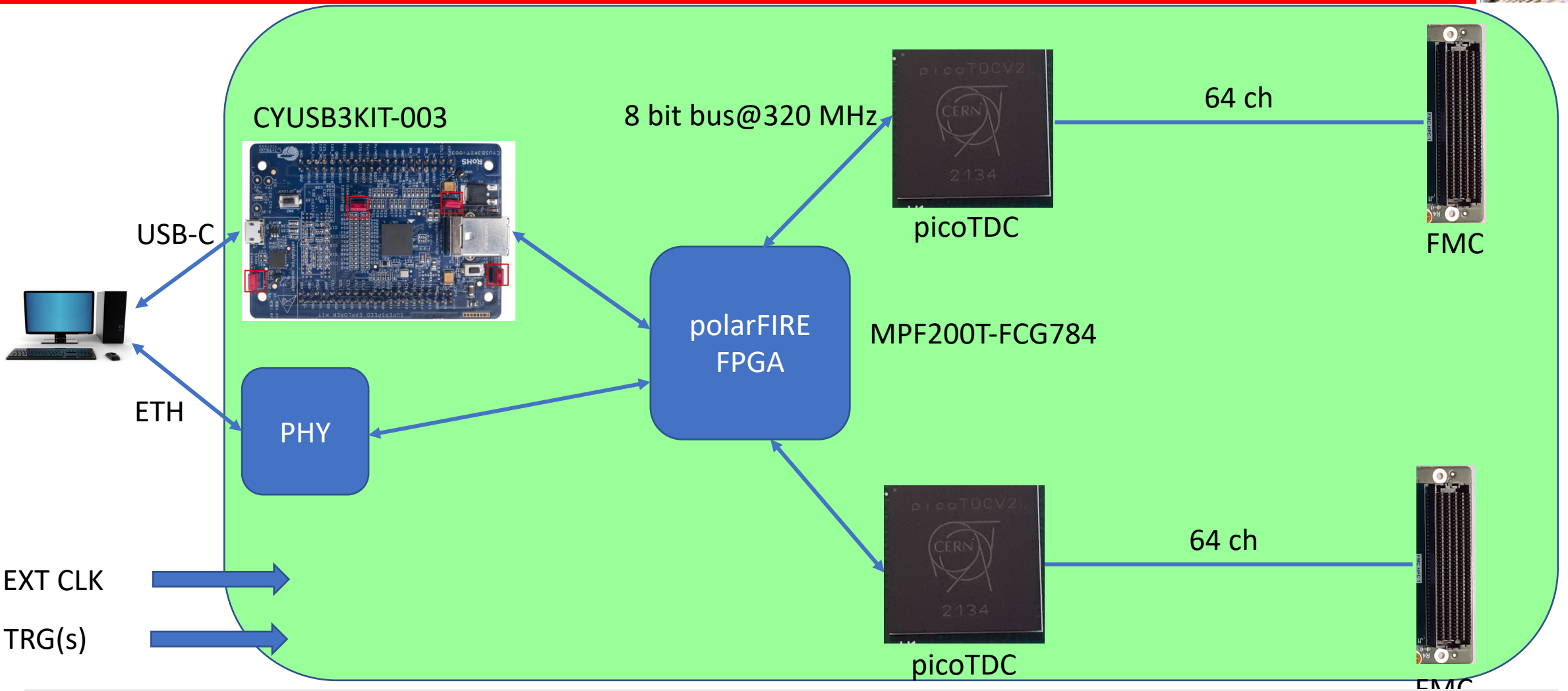
from MPRCs front -end



This is the hardware setup we plan to use in October 2022 for a test beam with MRPCs (eco-gas + new glasses)

1 Gbps ETH

picoTDC custom board (synergy with AIDAinnova)



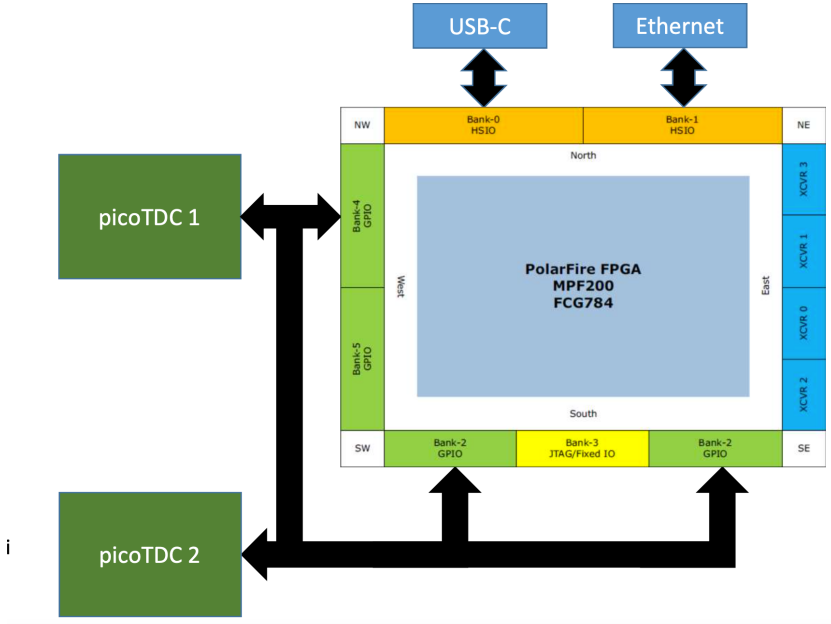
We are designing a custom board with 2 picoTDCs and 1 FPGA up to 128 ch. and higher data rates : (ready by first semester 2023)

- request to CSN3 in September 2022 (10-15 KEU)
- it is a generic card but we will test all solutions for "TRM2", especially new FPGA, databus readout and possibly irradiation qualification

Identifying candidate FPGA: PolarFIre: **MPF200T - FC784 (29x29, 1.0 mm)**

Design choices:

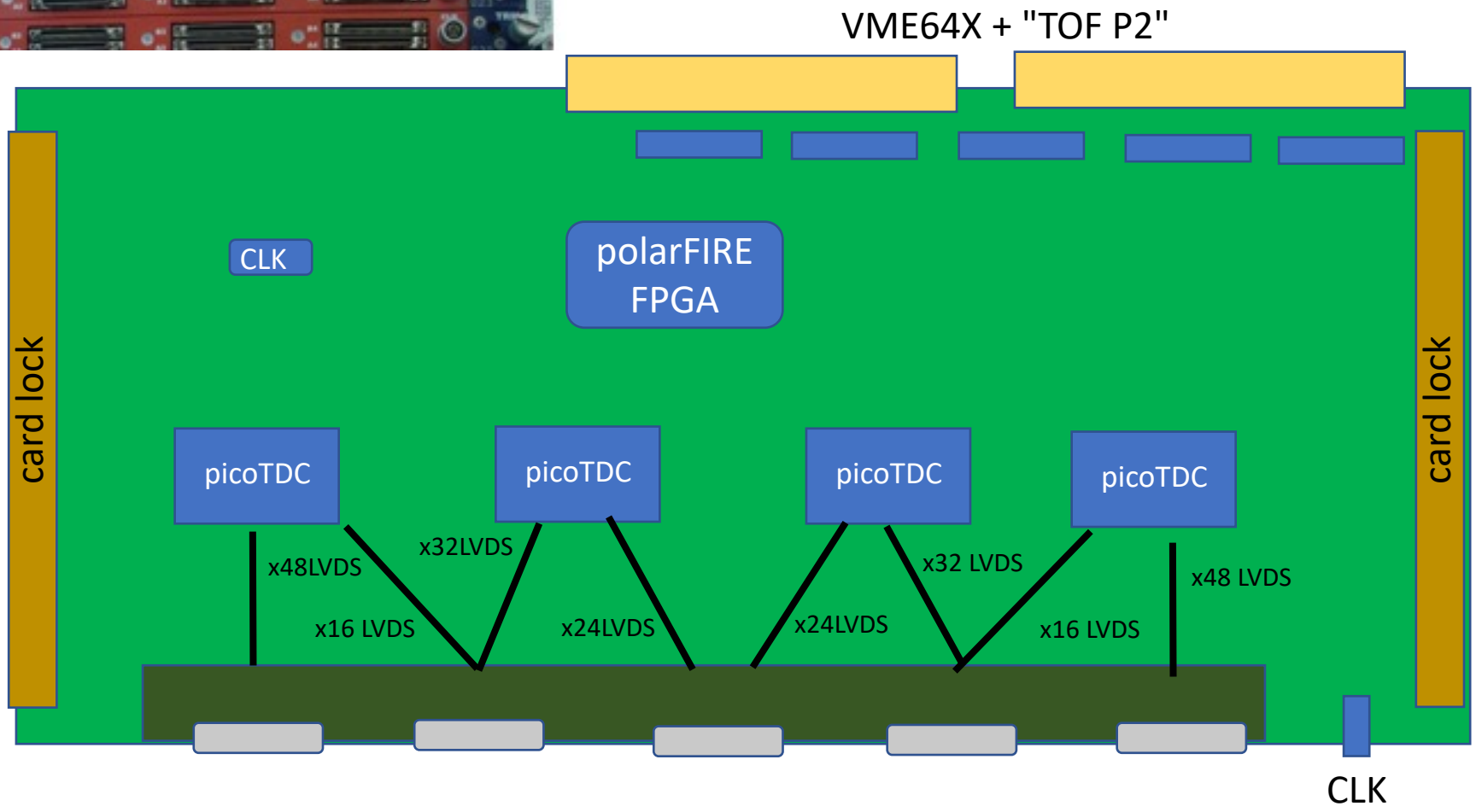
- learn new building bricks of TRM2
- portable & easy to use
- pluggable to different FE-ASIC via FMC
- massima bandwidth: 64 pin dif x picoTDC ma anche schema a 16



	Features	PolarFire FPGA				
		MPF050T	MPF100T	MPF200T	MPF300T	MPF500T
FPGA Fabric	K Logic Elements (4LUT + DFF)	48	109	192	300	481
	Math Blocks (18x18 MACC)	150	336	588	924	1480
	LSRAM Blocks (20k bit)	160	352	616	952	1520
	uSRAM Blocks (64x12)	450	1008	1764	2772	4440
	Total RAM Mbits	3.6 Mbits	7.6 Mbits	13.3 Mbits	20.6 Mbits	33 Mbits
	uPROM Kbits	216 Kbits	297 Kbits	297 Kbits	459 Kbits	513 Kbits
	User DLL's/PLL's	8 each	8 each	8 each	8 each	8 each
High Speed I/O	250 Mbps to 12.5 Gbps SERDES Lanes	4	8	16	16	24
	PCIe Gen2 End Points/Root Ports	2	2	2	2	2
Total IO	Total User IO	176	284	368	512	584
Packaging Commerical (0°C-100°C)& Industrial(-40°C to100°C)STD and -1 R0HS	PackageType/Size/Pitch	Total User I/Os (HSIO/GPIO), SGMII CDRs/Transceivers				
	FCSG325 (11x11, 11x14.5*, 0.5 mm)	164(84/80) 6/4	170(84/86)7/4	170(84/86)7/4*		
	FCSG536 (16x16, 0.5 mm)			300(120/180)15/4	300(120/180)15/4	
	FCVG484 (19x19, 0.8 mm)	176(96/92) 7/4	284(120/164)13/4	284(120/164)13/4	284(120/164)13/4	
	FCG484 (23x23, 1.0 mm)		244(96/148)12/8	244(96/148)12/8	244(96/148)12/8	
	FCG784 (29x29, 1.0 mm)			364(132/232)18/16	388(156/232)18/16	388(156/232)18/16
	FCG1152 (35x35, 1.0 mm)				512(276/236)19/16	584(324/260)19/24

Team: P. Antonioli, M. Colocci + 1 post-doc (since 1/11/22, AidaInnova funding)
D. Falchieri, C. Baldanza, G. Torromeo

TRM2 how it could look like



2 piggyback (5 x side) with VHDCI connector (24 ch each, on two sides → 48 ch)
4 picoTDC.(nb.: 64 ch x 4 = 256!! 1 TRM1 = 240 ch and 30 HPTDC!)

TRM2 miscellanea and potential timeline

- 4 picoTDC or 5 picoTDC: 16 diff. I/O x chip
- just one PCB
- cooling & power: from 30 W to 4-5 W
- low drop protection
- no jumpers
- automatic clock selection
- FW upgrade + special VHDCI "port"
- NINO and picoTDC inputs
- RAM inside FPGA (or external?): FIFO dual port
- microcontroller as latchup watchdog
- radiation tolerance qualification (EIC--> TIFPA)
- "obsolescence"

Main idea:

- having a sizeable amount of spares to be deployed during LS3 and in future RUN4
- target: 100 TRM2

Project as "DRM2" + INFN/CAEN accordo quadro

- test card: design & production → Bologna
- design (schematics) & firmware → Bologna
- layout + engineering → CAEN (estimated 3000 hours ET)
- production → CAEN

June 2023 → 100 KEU for 5 prototypes from CAEN
Late 2024 → production order under "accordo quadro" (700 KEU)
by end of 2025 → production ended
→ ready for LS3 effort

Note:
CSN3 should consider best spending profile
TOF costs: 13 MEU so far, spend 1 MEU to stay until RUN4 is less than 10%

Other miscellanea upgrades: Slow Control Cluster

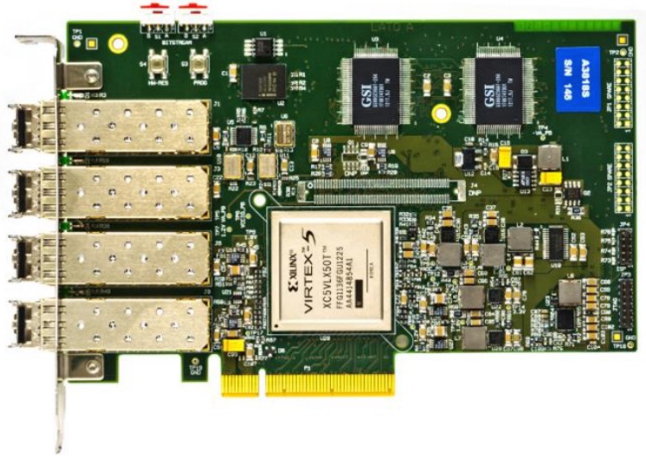
Slow Control Cluster and Slow Control Links

- 2 central servers (RAID) HP-DL380
- 18 servers (1 per Supermodule) + CAEN A3818 (PCIExpress V2.0 fully complaint but cannot guarantee compliance with V3)
- bought in 2014 (HP): at LS3 will be 12 years old

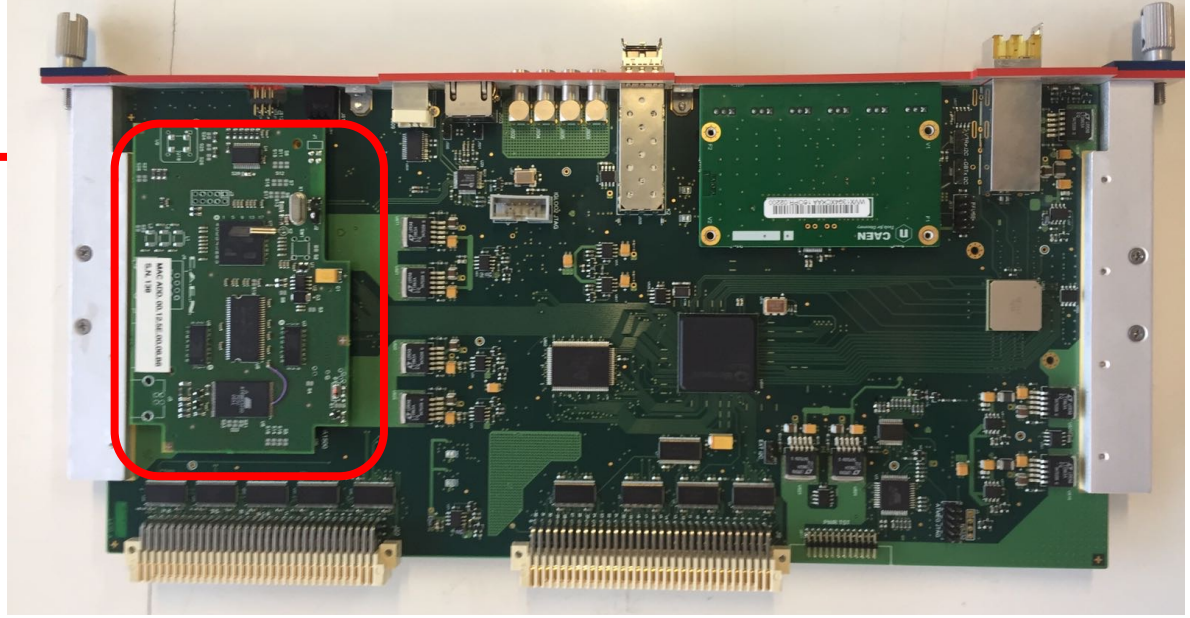
- We managed to buy HP spare parts to avoid problems (FANS, batteries) but we cannot expect having these PC working in 2032(20 years later). We will need to replace the factory during LS3 for RUN4
- CAEN is now producing A5818 (PCIExpress Gen 3x8) and servers available in 2026 will likely not be compatible with A3818

Indicative investment needed (in 2026/7): → 100 KEU

- 21 A5818: → 3740 EU/each → 78540 EU
- servers (in 2012: 24709 CHF for 21 HP-DL320 + 6 KEU 2 HP-DL380) → 30 KEU



Other upgrades: A1500 → BeagleBone Cortex-A8?



A1500 card now obsolete, used in DRM1/2 to upgrade firwmare
It also mount a very old ARM CPU and a very old µLinux (BusyBox)
CAEN until now sold it at 600 EU/each, now obsolete.

A1500

A1500

ARM Based General Purpose
OEM Single Board Computer

Obsolete

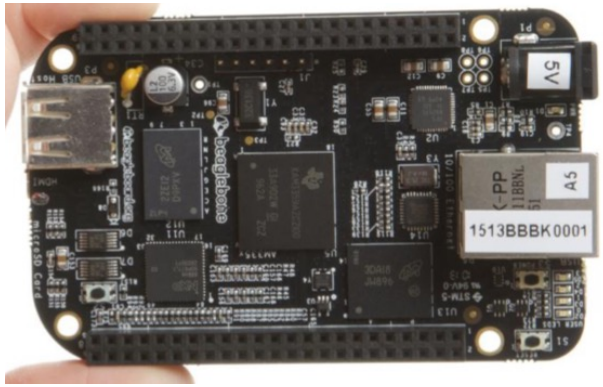
Core: 200MIPS at 180Mhz ARM920T CPU with MMU - 16K I-Cache - 16K D-Cache.

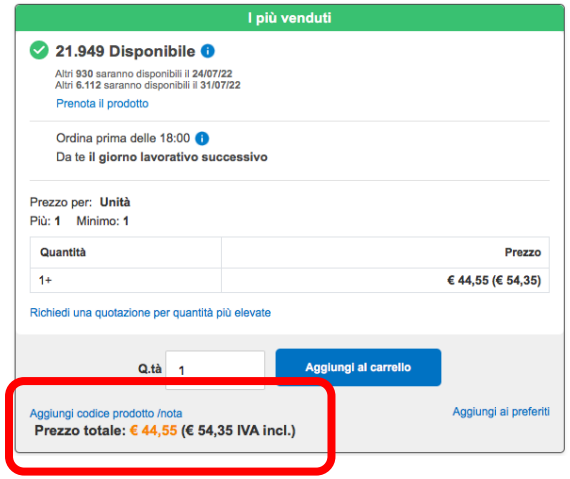
RAM: 16Kbyte internal SRAM and 32Mbyte 32-Bit Wide external SDRAM.

FLASH: 2Mbyte 16-Bit Wide parallel and 8Mbyte serial DataFlash.

	A1500	BBB
MEM	32	512
FLASH	512	4096

BeagleBone Black, MCU ARM Cortex-A8 AM3358, memoria flash eMMC incorporata 4GB, interfaccia USB





- Occorre fare schedina di adattamento
- Testare il sistema / geometrie
- Test in radiazione

➢ Potrebbe essere opzione per A1500 che si rompono (da fare a "bassa intensità", e costa poco)

➢ Task che piace a servizi elettronica e PhD smanettoni.. ;-)

Concluding remarks to ALICE referees 5th July 2019 (PA/TOF)

TOF toward 2030...

Not for action, just for thoughts...

All TOF modules have now passed more than 10 years of operations, some of them assembled in 2006, with electronics basically chosen in 2003/2004.

Given LS3 extension, it is now likely ALICE will end operations in 2030.

"TOF core" has been the financial tool so far. After interventions from GE (- 1M€ & then some re-fill 210k€ (2017) + 100k€ (2018) we have just 60 k€ (still to be paid CRU and A1395 refurbishments + other CERN items) → we should stay at zero end of 2019.

CSN3 / TOF / GE should start to **think financially *long term***. No major upgrades but... to maintain operations until 2030 some robust TOF expenses will almost certainly happen.

- Part of TRM modules could need to be re-engineered to produce "brand new spares"?
- PC for slow control (18 +2 cluster) bought in 2014, unlikely to stay until 2030
- ...

TOF core "on demand"?
Normal CSN3 budget (but adjust...)?

First SM installation / Oct 2006

Last SM in / 24 Oct 2008

TOF extraordinary maintenance: final overview

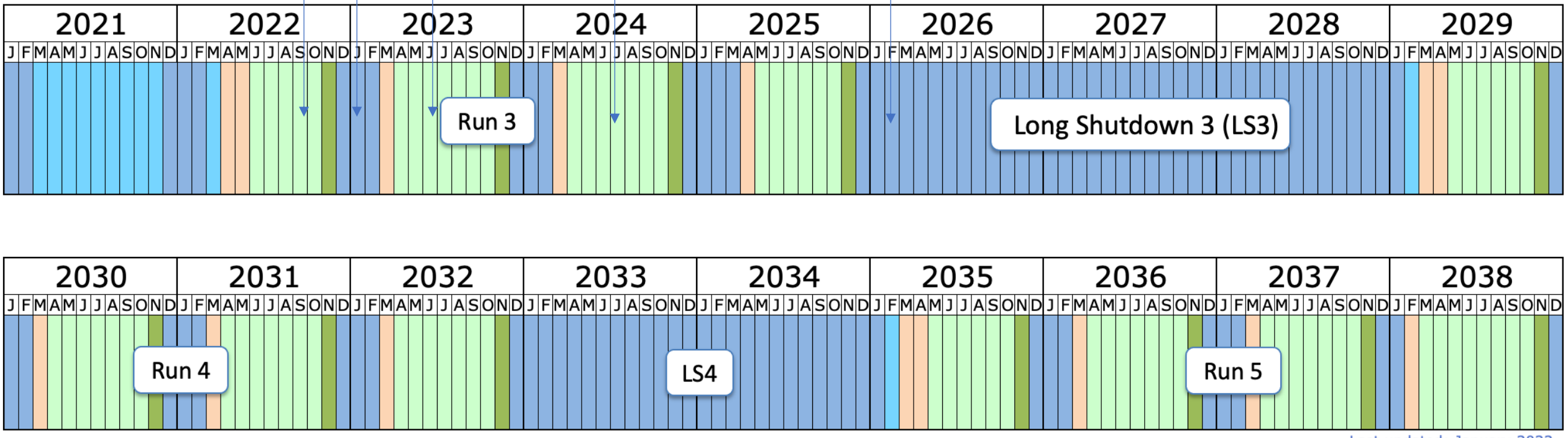
DC/DC spares: 84 KEU

TRM2 test:
15 KEU

TRM2 proto:
100 KEU

TRM2 prod:
700 KEU

A5818+servers
110 KEU



Last updated: January 2022

Shutdown/Technical stop
Protons physics
Ions
Commissioning with beam
Hardware commissioning/magnet training

TOF extraordinary maintenance:
- 1 MEU in 4 YEARS
- spending profile?