Aggiornamento ALICE ITS3 2021-22

S. Beolé

21 Luglio 2022

OUTLINE

- ITS organization and INFN responsibilities
- ITS status and plans
- ITS3 status and plans

Project Organization

Institute Board

Team Leaders, Project Leader, Deputy Project Leader, ITS3 sub-project leaders, Technical Coordinator

Project Leader

S. Beolè

Deputy Project Leader

A. Di Mauro

ITS3 sub-project

Sub-project Leaders

A. Kluge, M. Mager

Work Packages Conveners

Physics and Performance/A. Kalweit, **A, Rossi**

Chip Design/G. Aglieri, W. Snoeys

Chip Characterization/M. Suljic, S. Senyukov

Thinning, Bending and Interconnection/

G. Contin, ***D.Colella***

Mechanics and Cooling/C. Gargiulo

ITS2

Technical Coordinator

F. Reidt

Deputy: M.Keil

System Run Coordinator

J. Liu (6/22)

N. Valle (12/22)

Electronics Coordinator

G. Aglieri

Software Coordinator

I. Belikov – M. Concas

Sub-system Coordinators

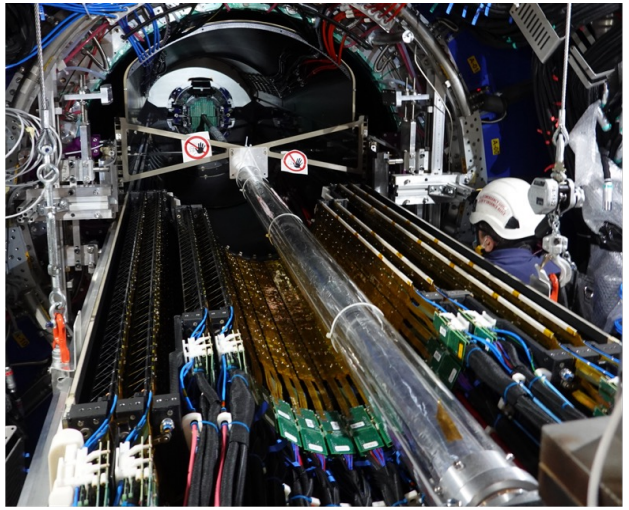
DCS/M. Keil

ITS2S/P. Martinengo

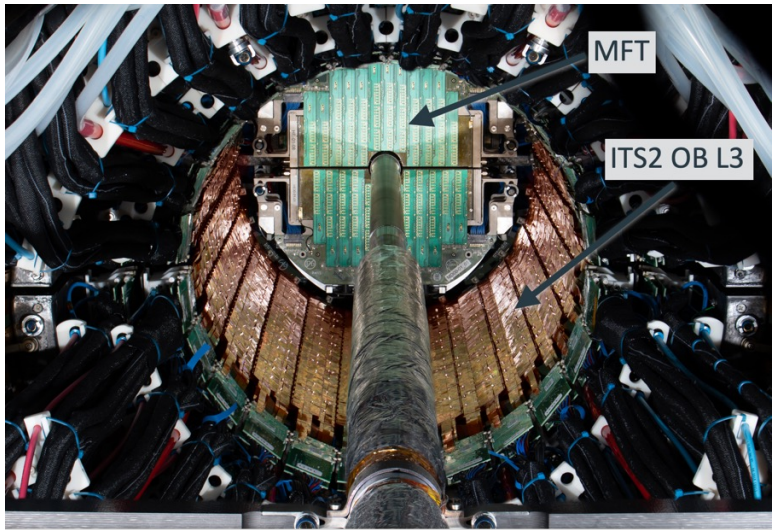
Cooling/S. Senyukov

ITS

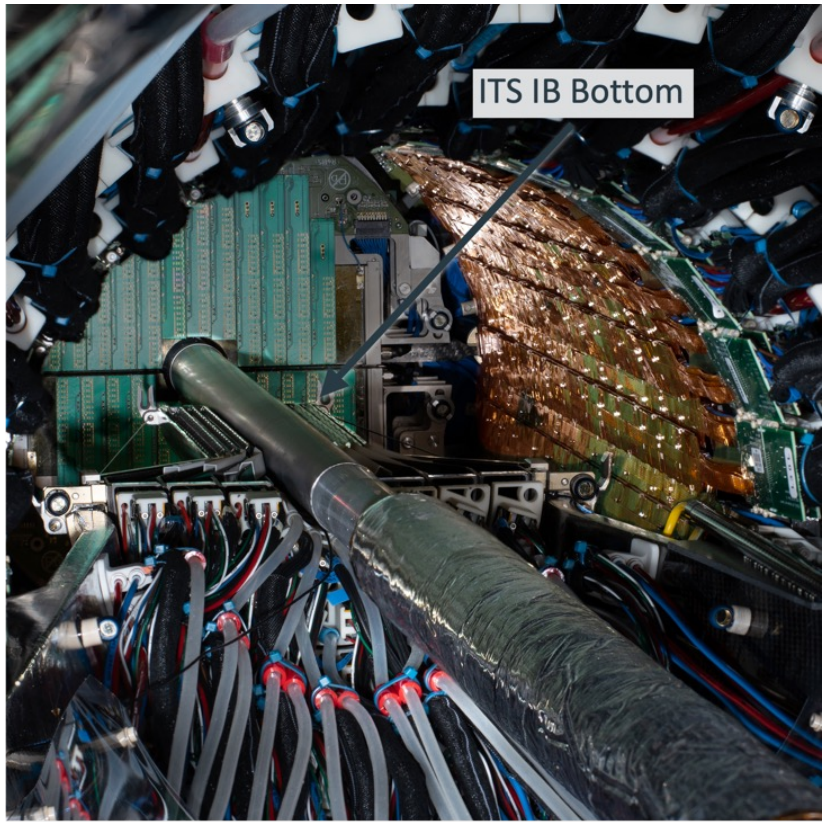
ITS installation: May 2022



Outer Barrel Bottom being inserted on the rails inside the TPC



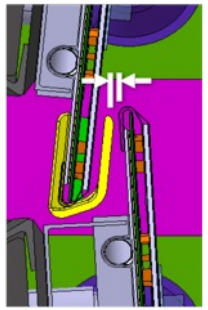
ITS Outer Barrel surrounding the beam pipe, MFT in the back



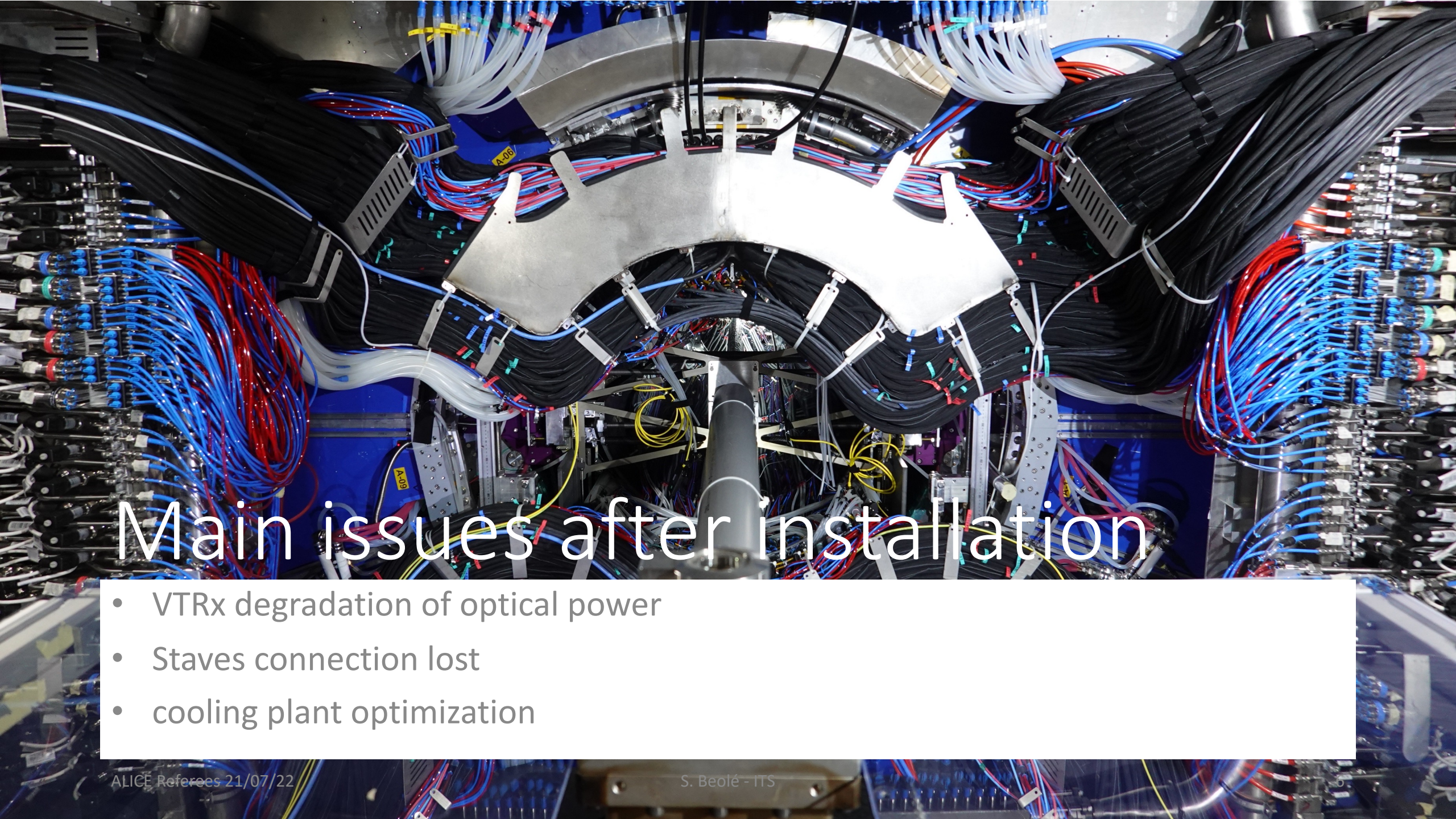
ITS Inner Barrel Bottom and Outer Barrel

- Installation challenges
  - Precise positioning around the beam pipe (nominal clearance ~ 2 mm)
  - Manipulating from 4 m distance
  - Difficult to see actual position by eye
  - precise mating of top and bottom barrel halves (clearance between adjacent staves ~ 1.2 mm)
- Dry-installation tests on the surface to test and exercise procedures
- Use of 3D scans, surveys and cameras

1.2 mm nominal clearance



OB stave edge clearance when fully mated



Main issues after installation

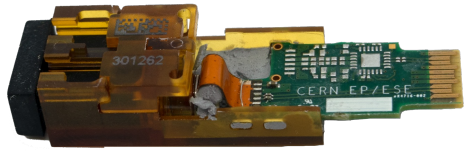
- VTRx degradation of optical power
- Staves connection lost
- cooling plant optimization

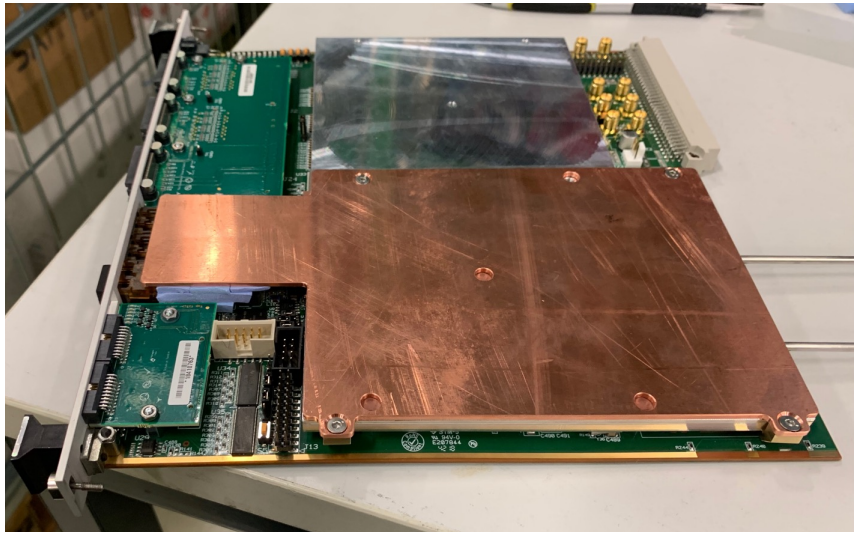
VTRx saga – Executive Summary

ISSUE: degradation of optical power due to presence of dirt coming from badly cured glue around the lens

SOLUTION: bake the modules + install cooling plates

- Set of post-cured modules (12x 300h + 24x 500h) installed mid July, no degradation observed until mid-September (when the cooling was installed)
- Modus operandi
  - Reworking on 4 sub-racks in parallel to speed up
    → small detector portion available for runs, but rework more boards while magnet is off
  - Full disconnection and extraction of Readout Units and Power boards
  - Rework and test the RU in the cavern (behind A-side racks)
- Issues:
  - ~3 weeks shipping delay for the cold plates from the UK
    → Used time to commission the test setup and replacement of VTRx modules
  - Yield: few broken modules after adding gap pad, VTRx SM spares could be insufficient
    → potentially need to wait until late September to complete IB
  - Readout Unit more sensitive too mechanical stress than foreseen
  - Subset of the gap pads too rigid for our application
  - Main cold plate not always well fixed (caused by too long screws)
- Operation completed successfully



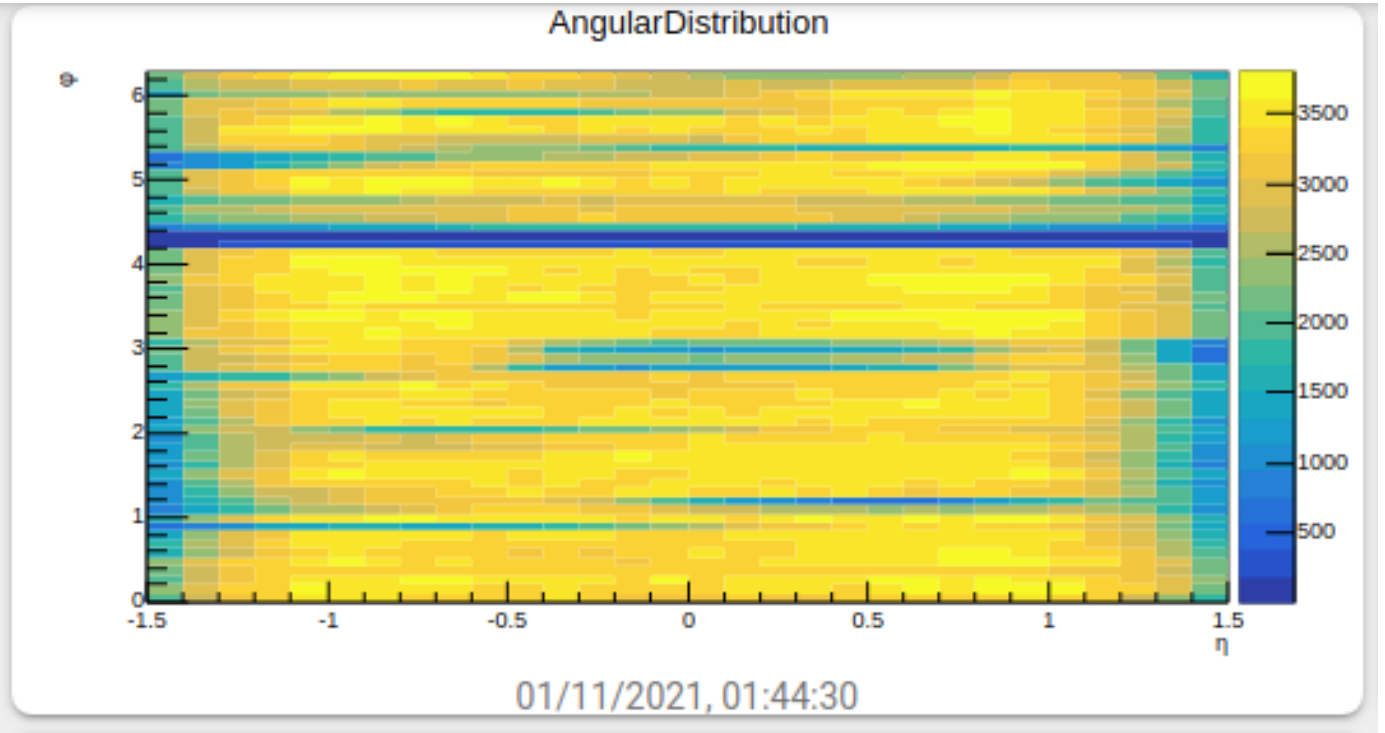


Thanks a lot to full team!

Andrea Triolo (Messina), Antoine Junique (CERN), Corrado Gargiulo (CERN), Daniel Battistini (Torino), Elisa Laudi (CERN), Felix Reidt (CERN), Francesco Mazzaschi (Torino), Marc Imhoff (IPHC), Luca Aglietta (Torino), Mario Ciacco (Torino), Pascal Secouet (CERN), Piero Giubilato (Padova), Stefano Politanò (Torino)

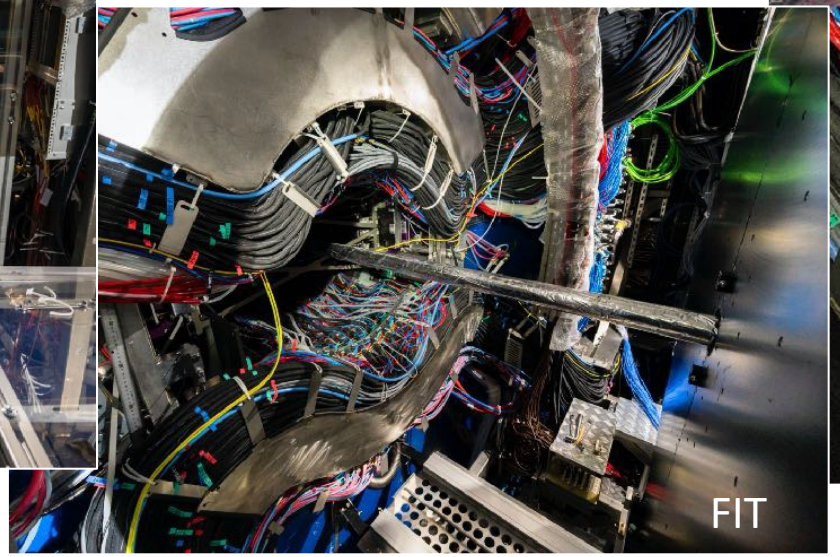
Issues after FIT installation: staves disconnected

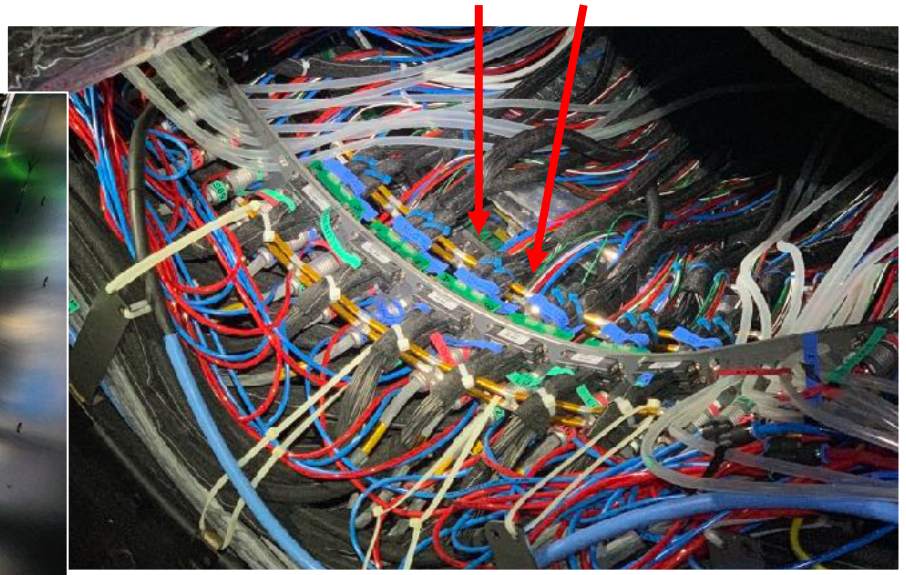
- “hole” in the eta-phi tracks distribution: due to missing L3_16 and L4_22



Recovery of L3_16 and L4_22

- **FIT displaced** first week of December by **Corrado Gargiulo's team and members of the FIT team**
- A big thank you from the ITS to our colleagues!
- Not (too) inconvenient access to PP2, but the **beam pipe exposed**
- Concerned part of OB data hidden underneath the IB-BOT cables
- Detached IB cables and cooling tubes from the intermediate fixation behind the IB PP2 to obtain access without disconnection of IB-BOT

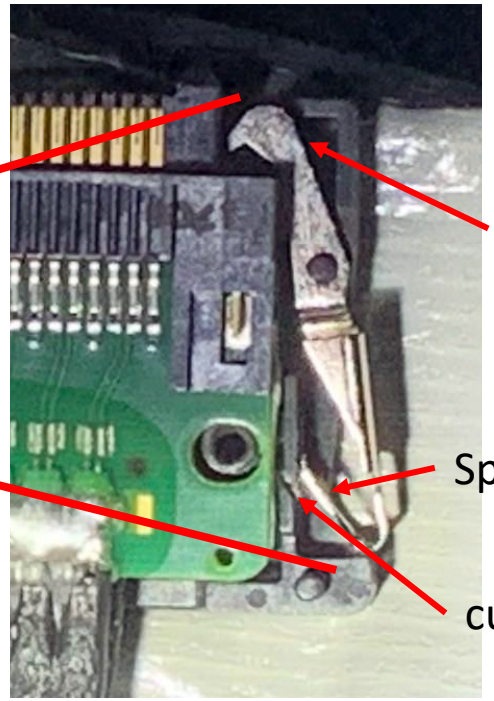




Recovery of L3_16 and L4_22

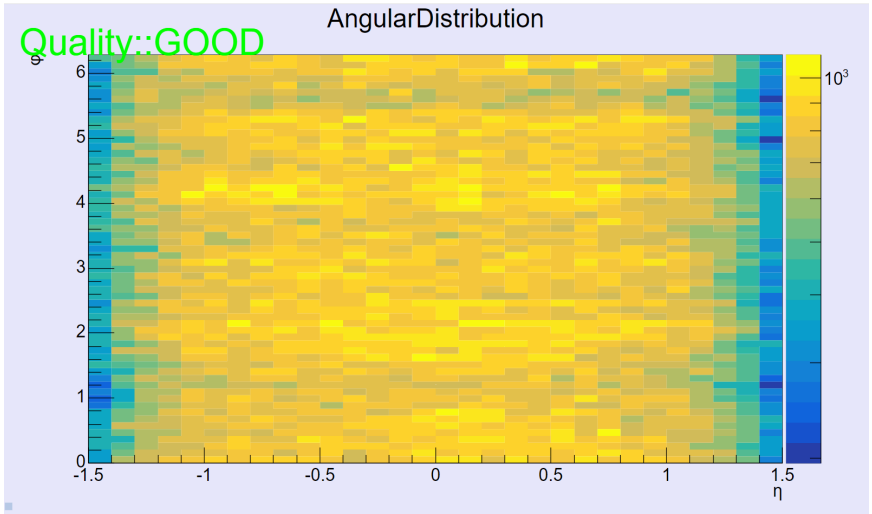
L4_22

- Issue identified to be in the PP2 region (behind FIT) using reflection measurements
- Inspection of PP2 confirmed partial connection due to broken retention mechanism
- Retention measurement repaired in-place and verified
- Resistance measurement correct
- CTRL communication and data taking working



L3_16

- No obvious connection issue at PP2
- Installed additional cable between PP1 and PP2
- No issues since the replacement
- Extraction of problematic cable currently not possible



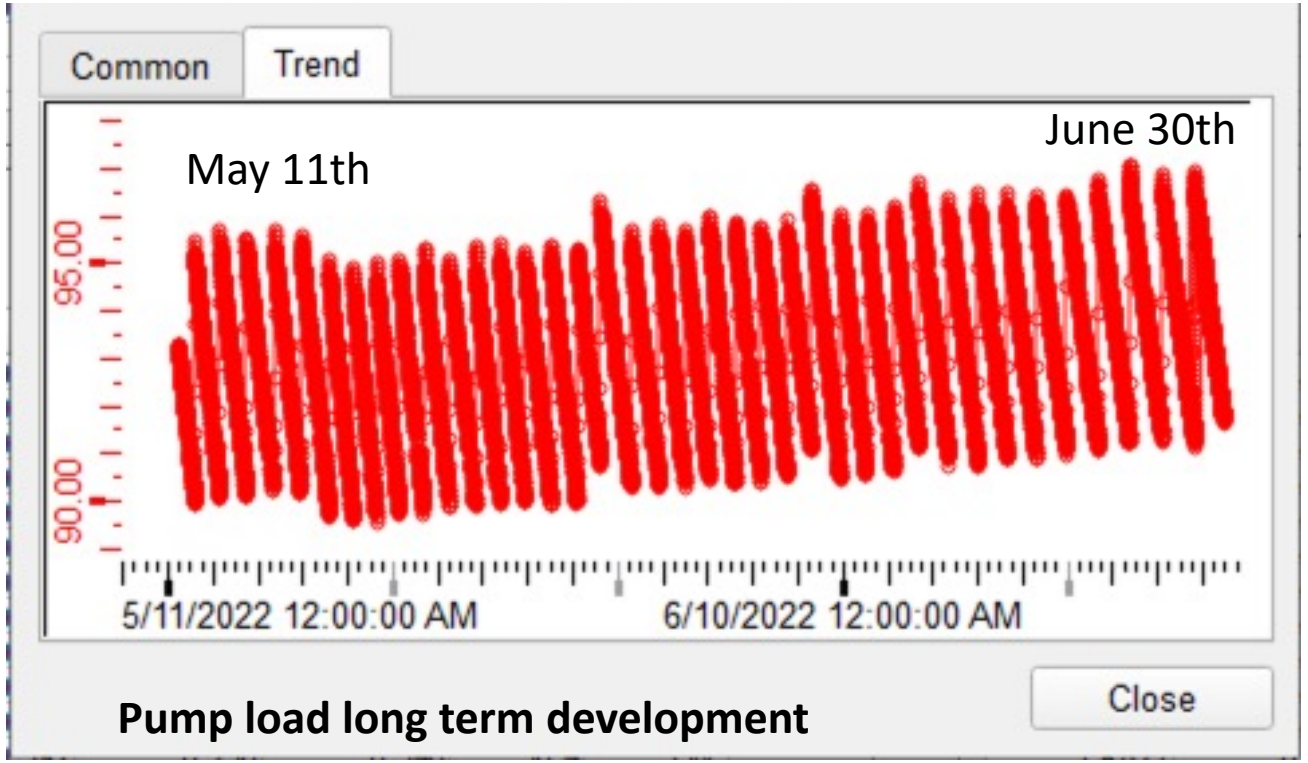
eta-phi tracks distribution: OK after intervention

Cooling plant

Issues: instabilities and pump inefficiency

KEY CHANGES:

- Upgrade main circulation pump
- Connection to chilled water to improve cooling capacity (6 instead of 14.5°C of the mixed water)
- Install valves in the return lines to equilibrate the pressure drops across line



Pump load long term development

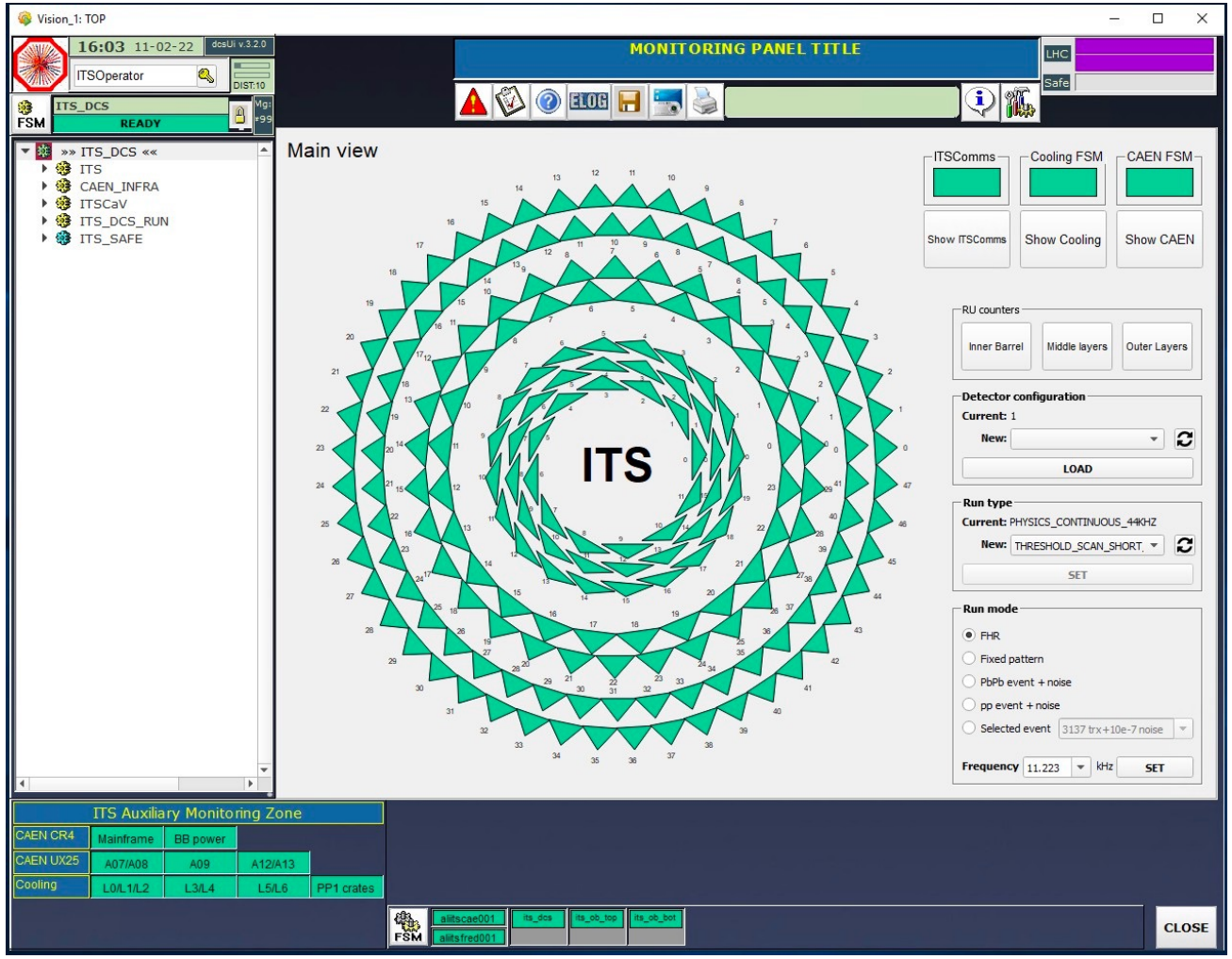
Staged approach due to component availability

- Stage 1: flow pump, connection to chilled water, flow meter recalibration DONE
- Stage 2: installation of valves in the return lines: 2022 YETS

Preparation for data taking

Detector Control System

- DCS ready to control detector in all phases of operation:
  - Controls and configures pixel chips and entire infrastructure
  - Error recovery during a run to continue running with minimal data loss
  - Detector functionality implemented in C++ library (pixel chips, readout cards, regulator boards)
  - GUI, FSM and alarms in Siemens WinCC OA
  - fully integrated into ALICE DCS
- Routinely used during commissioning and Pilot Beams



Calibration

The Challenge:

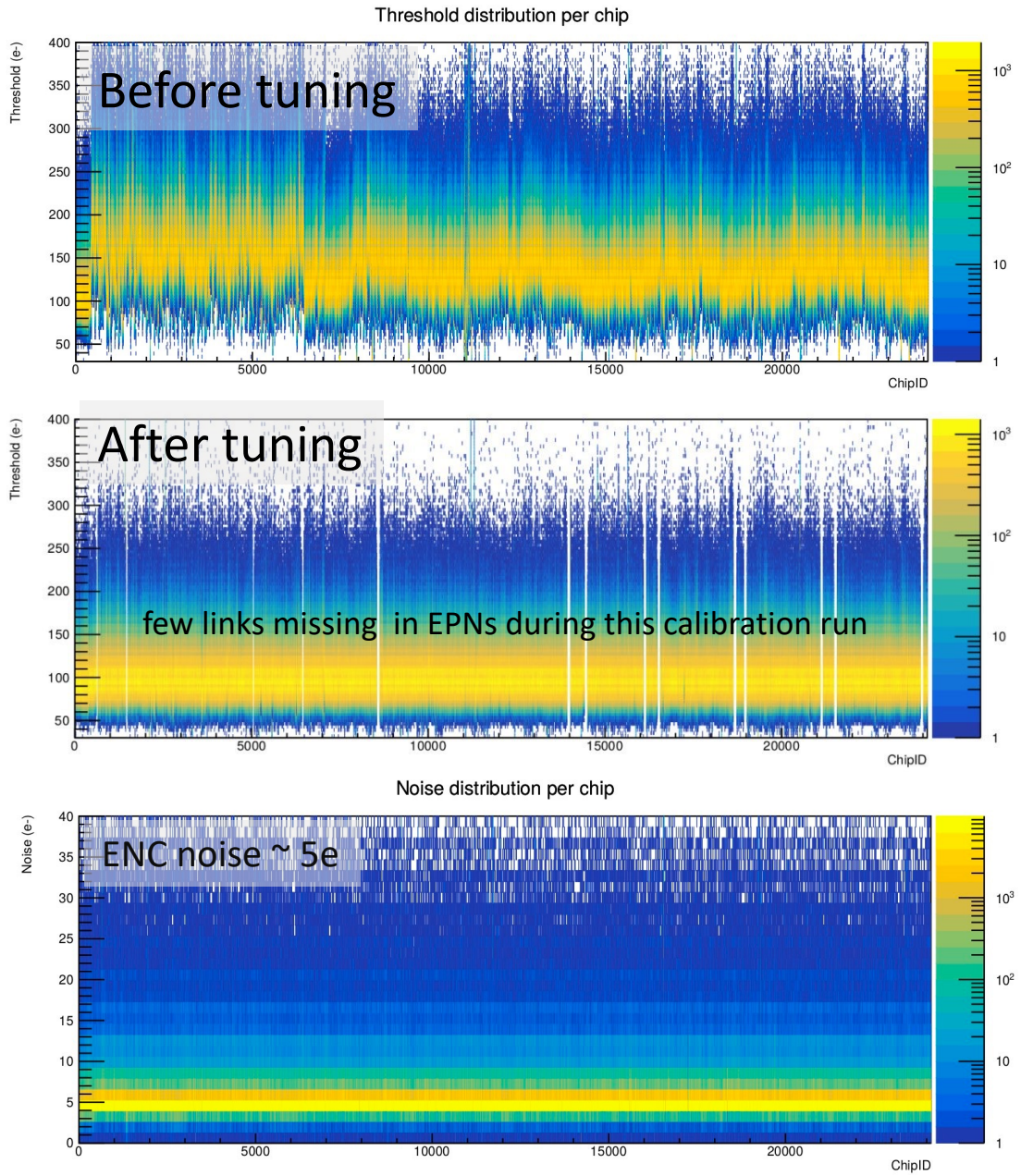
- Online calibration of 12.5 billion channels
- Threshold scan of full detector: > 50 TB of event data
- Several scans to be run sequentially
  - Threshold tuning (adjust thresholds to target)
  - Threshold scan (measure actual thresholds)

Procedure:

- DCS performs actual scans: configure and trigger test injections
- Scan runs in parallel but independently on all staves
- Distributed analysis on event processing nodes
- full procedure takes **less than 30 minutes**

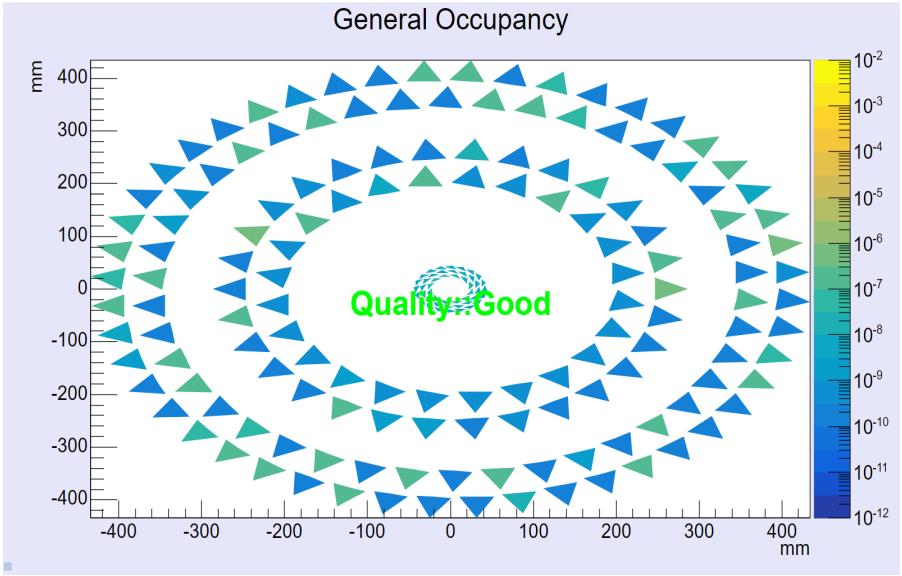
Results:

- Scan with online analysis successfully run on full detector
- before tuning: settings used in surface commissioning: detector already fully efficient
- After tuning:
  - Thresholds very stable on all the chips: RMS of threshold distribution per chip <23 e^- (compatible with what we had during production)
- ENC noise ~ $5e^-$



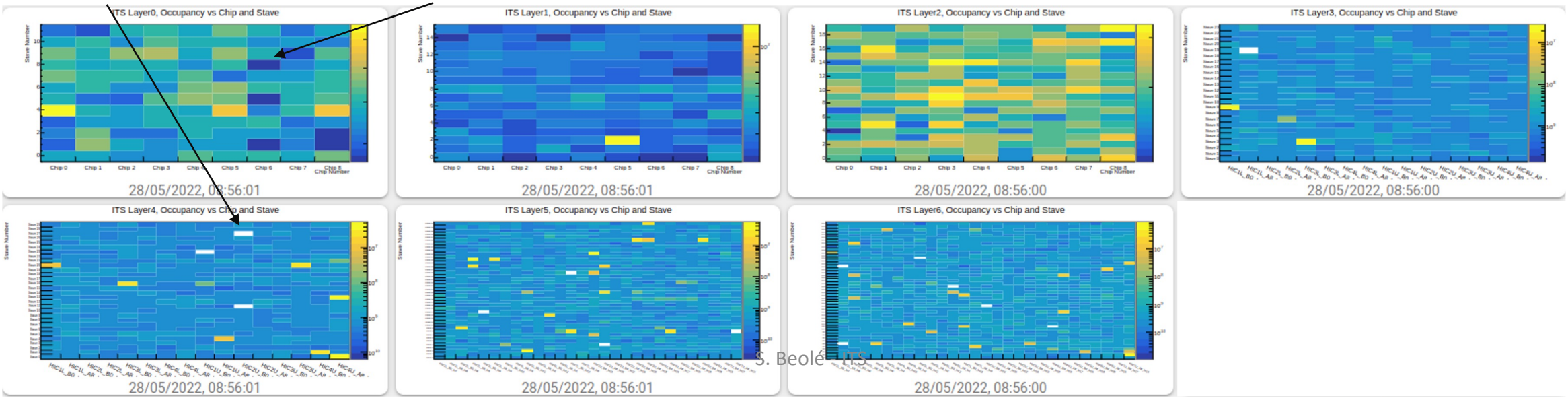
Data Quality Control (QC)

- Comprehensive online QC to check data quality and spot problems early
- 6 QC online tasks to monitor DATA/MC quality: FHR, FEE, Cluster, Track, Noisy Pix, Monte Carlo
  - *Front-end electronics:* data integrity check with payload decoding of all events
  - *Occupancy:* monitoring of detector occupancy
  - *Cluster:* monitoring cluster size, topology etc.
  - *Tracks:* monitoring of track multiplicity, angular distribution, clusters etc.
  - *Noisy pixels:* extraction of noisy pixels for offline noise masks
  - *Threshold:* monitoring during calibration scans (threshold, ENC, dead pixels)
- Offline version of track and cluster task
- QC post-processing online and offline: FHR, FEE, Tracks, Clusters, Thresholds
  - Analysis and trending of QC online plots (run by run)

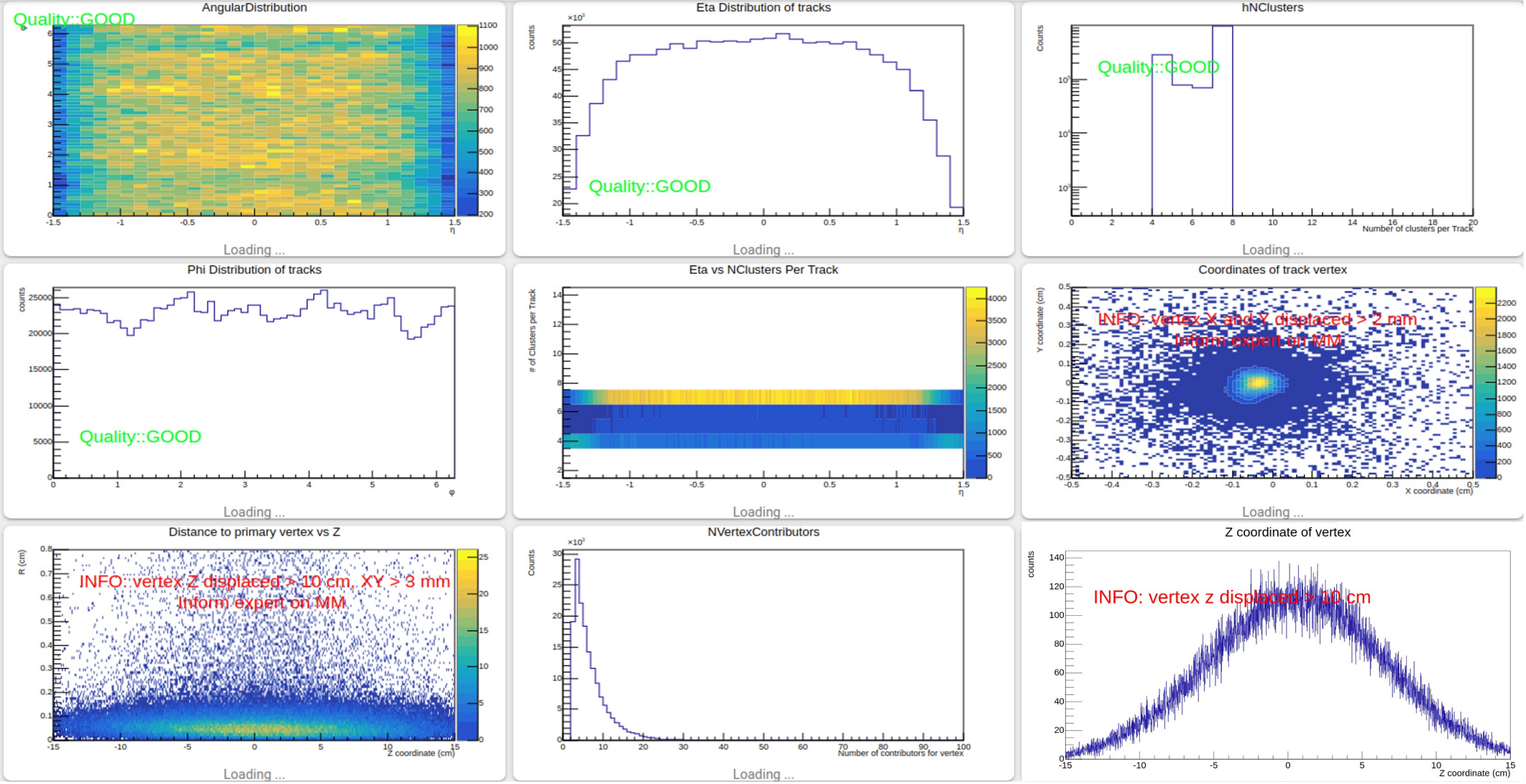


Empty lane (entire run)

Lane stopped sending data during run



Plots from collisions (pp @900 GeV)

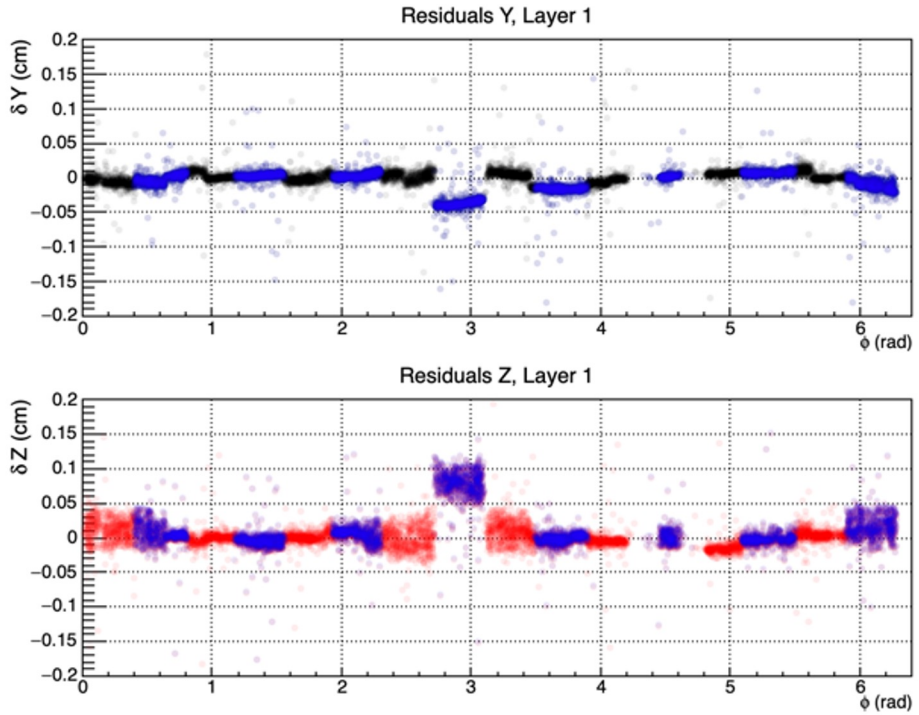


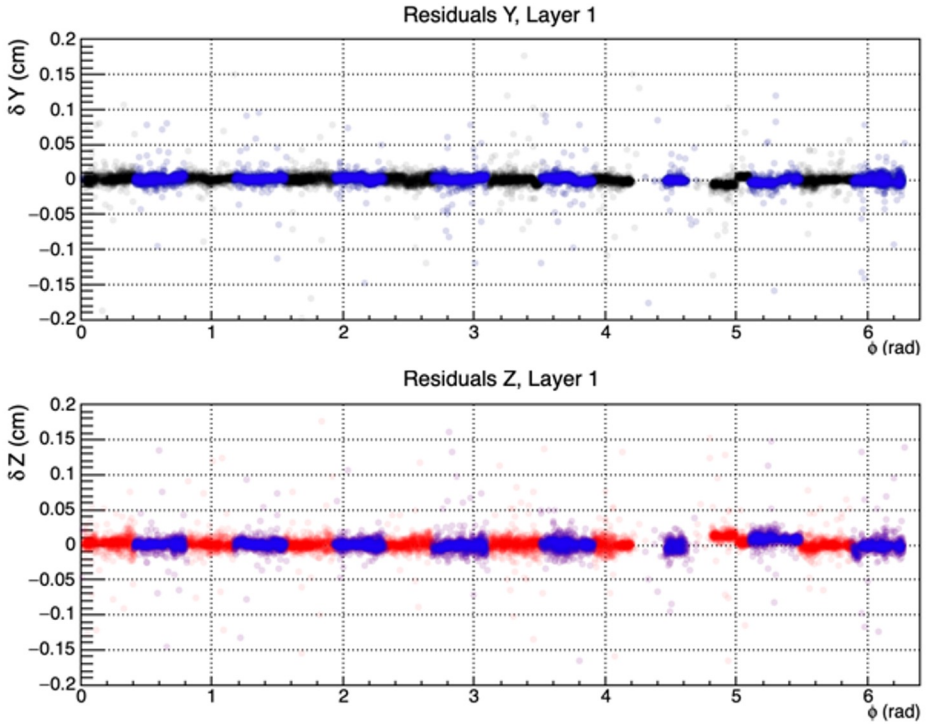
Data Preparation: alignment

Milestone: calibrazione e allineamento sensori
- allineamento 50% a giugno 2022: ritardi nel porting del framework Millepede da AliRoot a O2

- Manual pre-alignment concluded with precision of O(100 µm)
- Ongoing: pre-alignment in R, Rϕ and Z using Millepede
  - currently at O(10 µm) for Inner Barrel and O(30µm) for Outer Barrel)
- Next step: fine alignment targeting a precision of a few µm (using Millepede, or AI approaches)

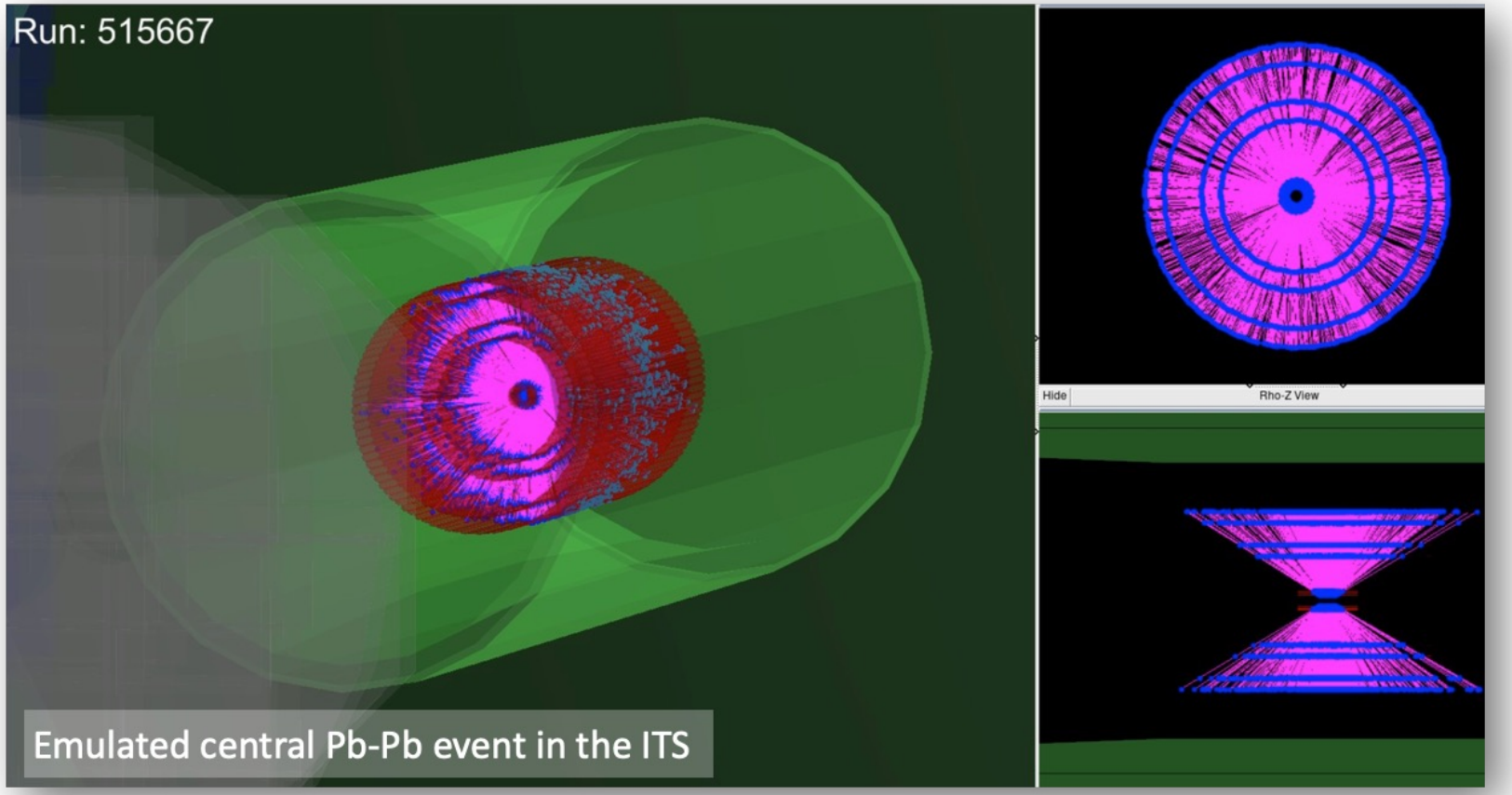
Below: example, Y and Z residuals in L1, before and after alignment with Millepede



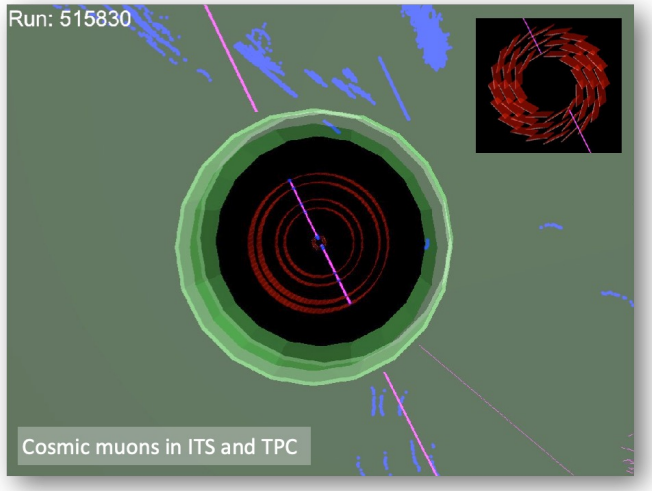


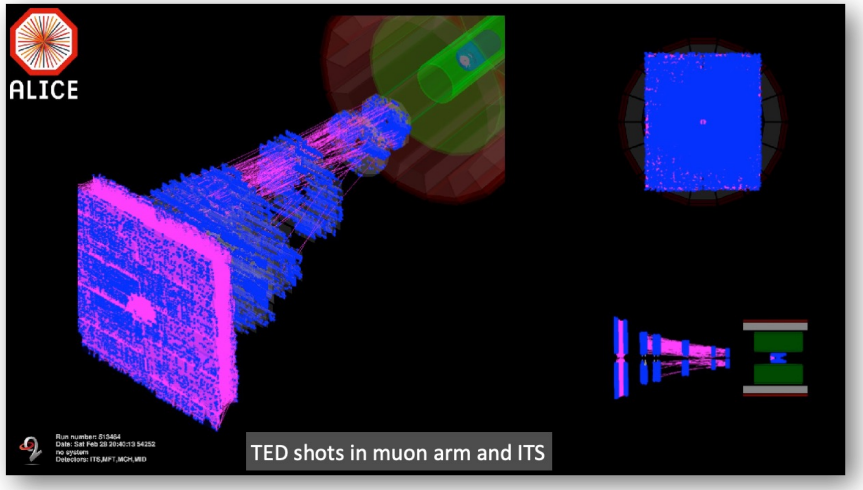
Data Taking Preparation

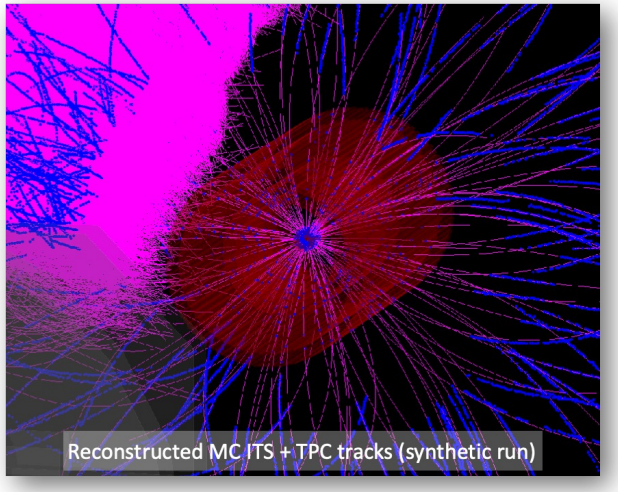
- Last part of commissioning phase devoted to prepare and test settings optimized for pp with 200 kHz framing rate (instead of 45 kHz: default for Pb-Pb) to achieve better time resolution reducing pile-up
  - successfully tested tested in pp Pilot Beam (2022)
- Extensive test runs with emulated Pb-Pb and pp events (injected into the detector front-end) to test detector, processing chain under realistic load

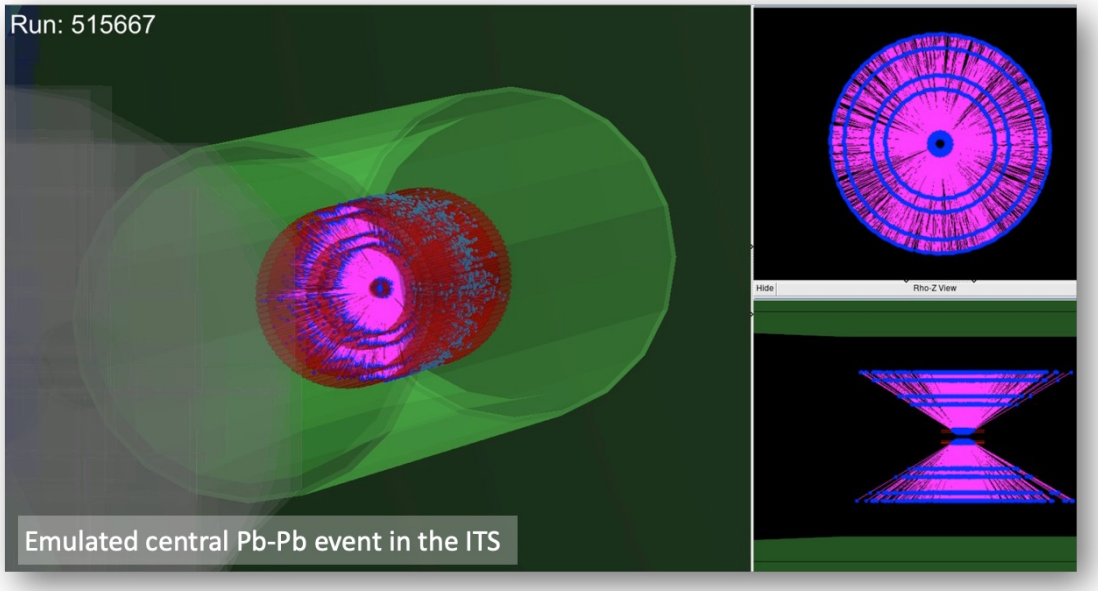


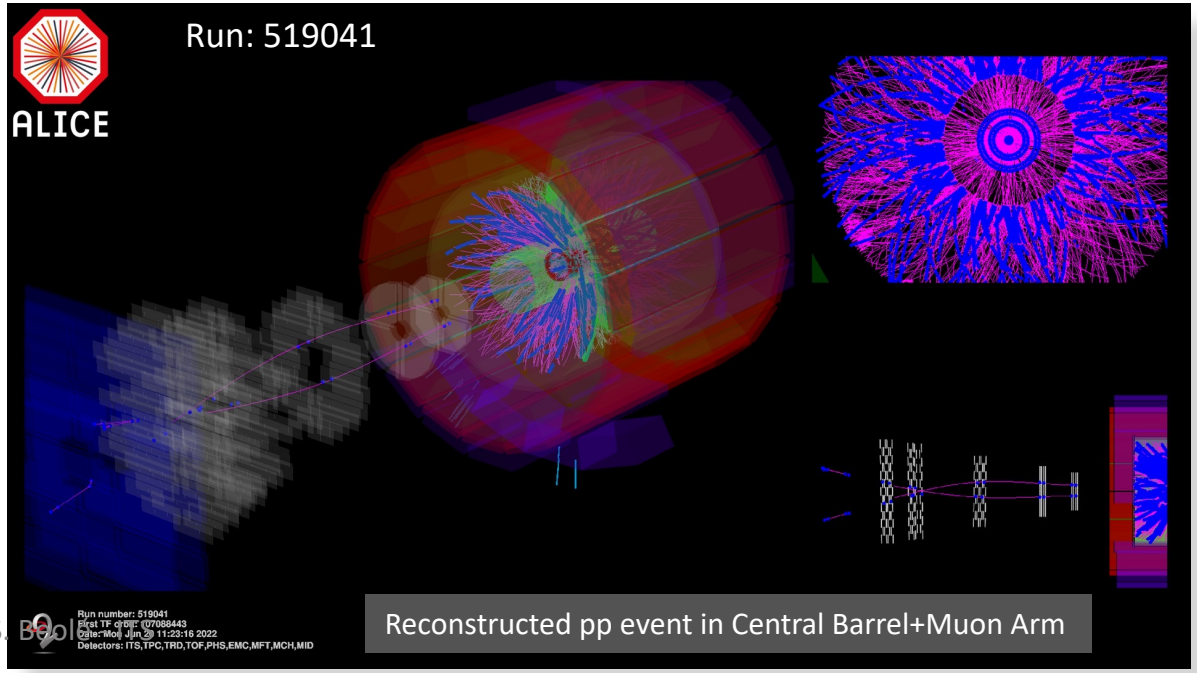
RUN 3 readiness





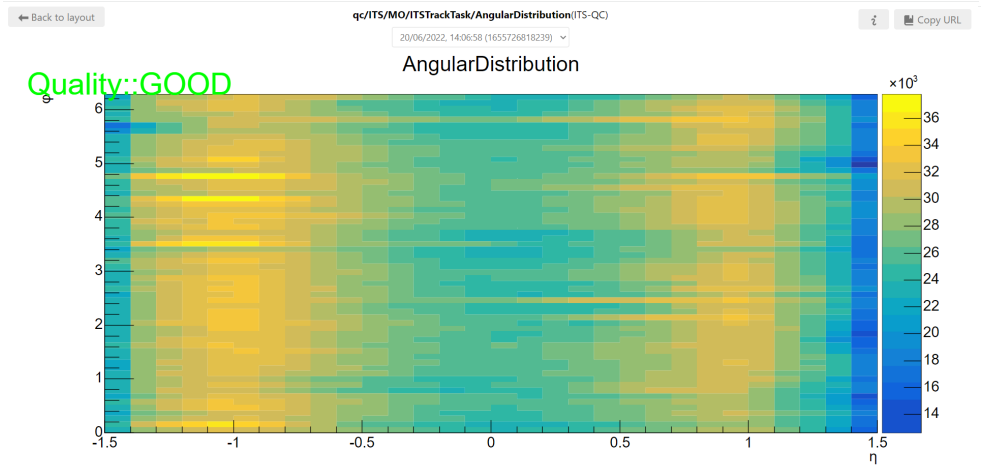


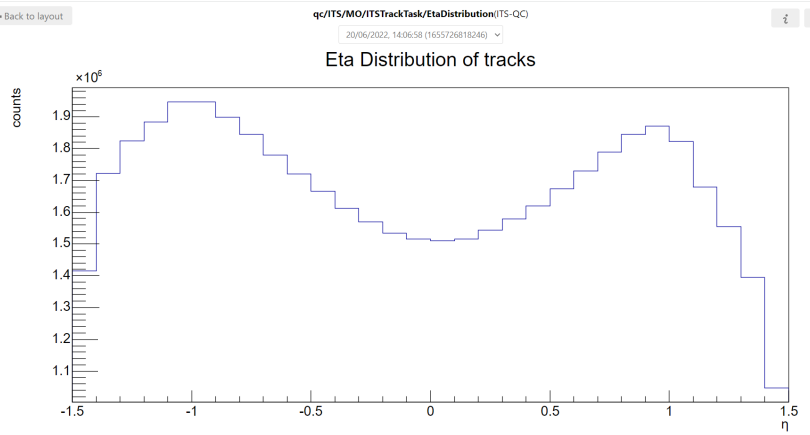


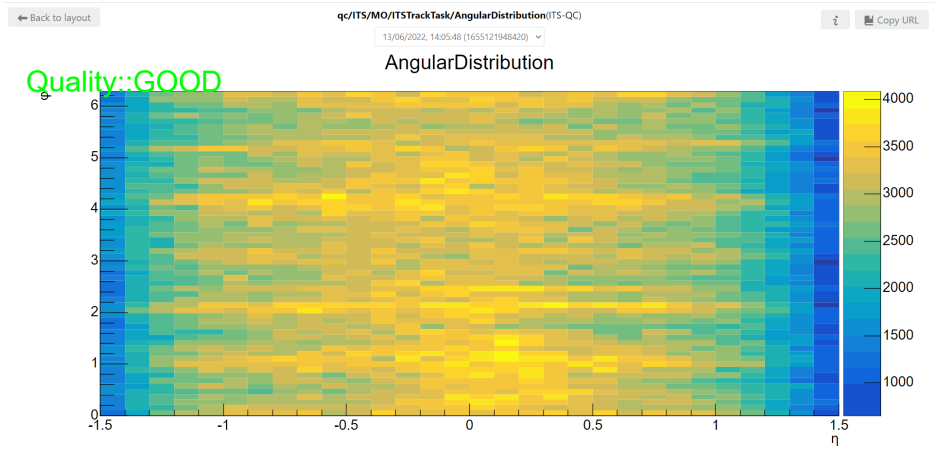


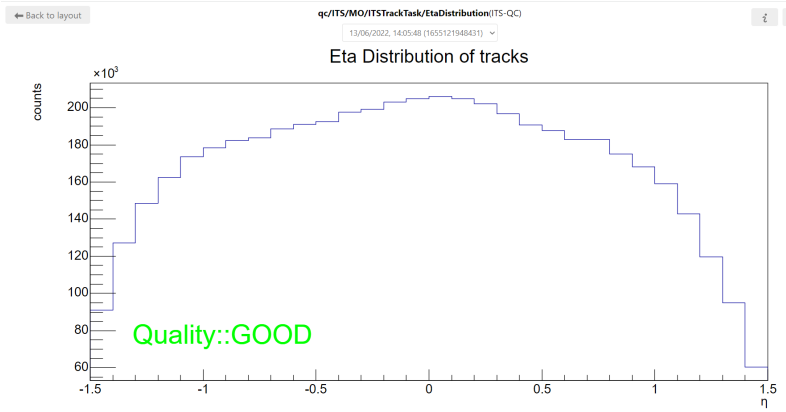
First results at high intensity (up to 300kHz interaction rate)

- Framing Rate 202kHz
- Seeing asymmetric eta distribution with 8 collisions during the stable beams at injection energy. filling scheme Single_16b_8_8_8_noLR2
- No asymmetry for 2 collisions Single_4b_2_2_2_noLR





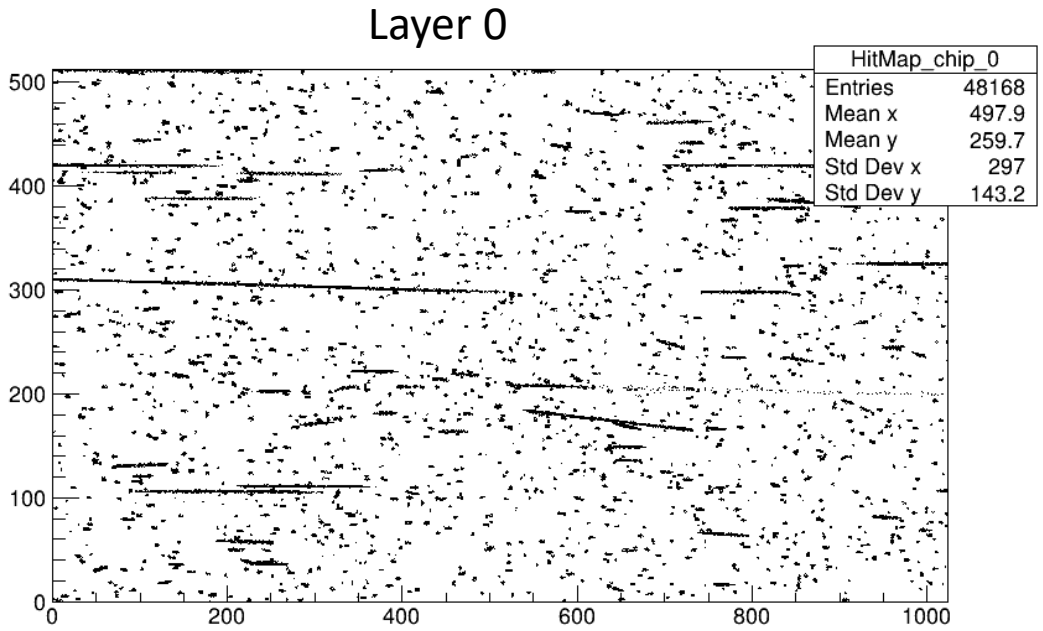


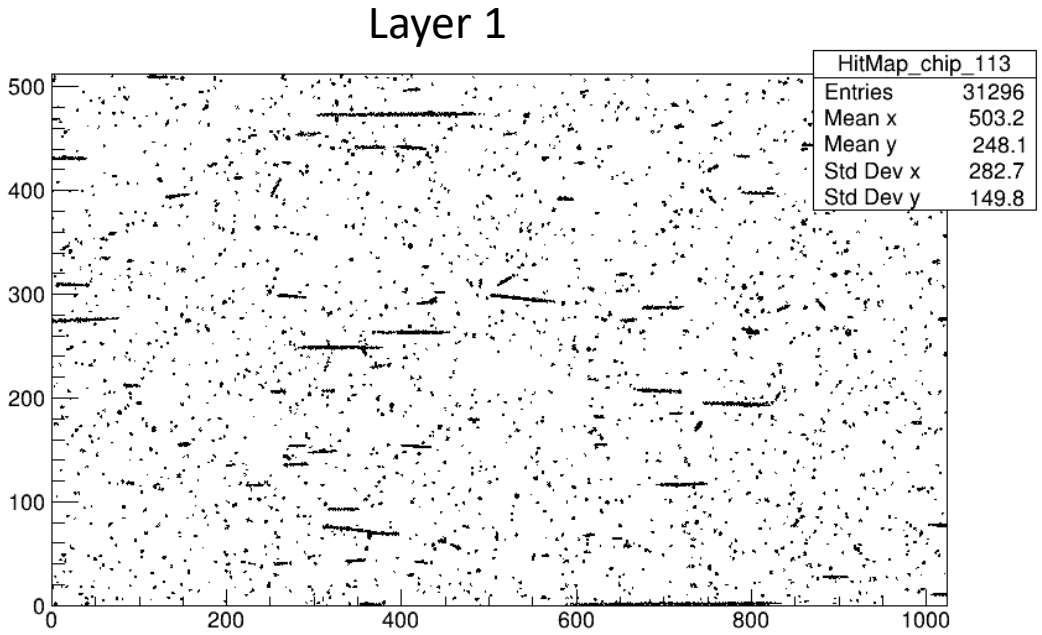


Possible reason: tracks pile-up in adjacent frames. Being investigated, masking of clusters removed, merging of clusters in adjacent readout frames considered as a viable solution

First results at high intensity (up to 300kHz interaction rate)

- Huge clusters (cluster size > 50)
- Consequence: chips in busy (mostly in inner layers)
- Solution: tuning of RU time out values

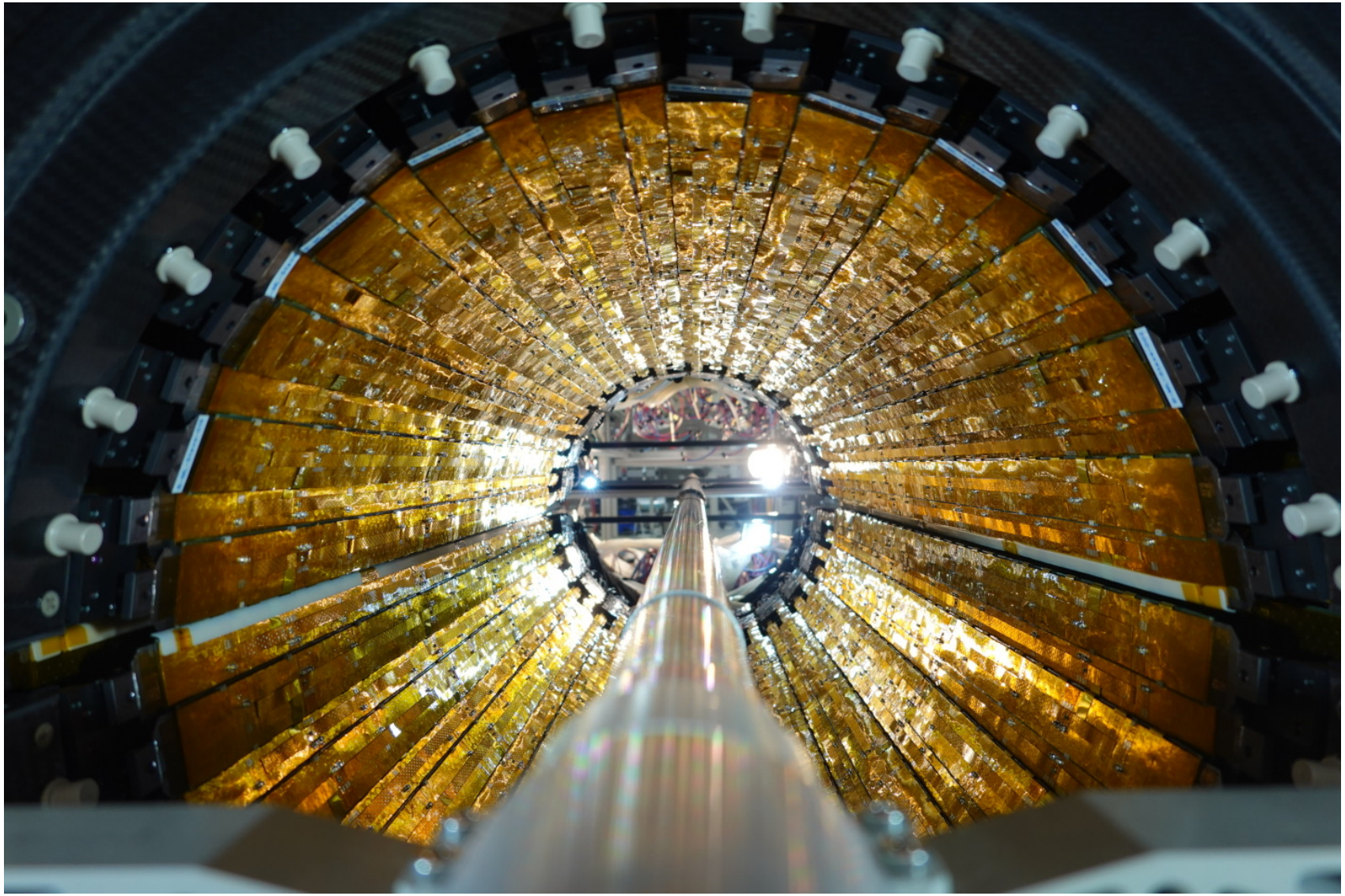




Conclusions

- ITS2 successfully installed and commissioned for LHC RUN3
- Calibration procedure established and tested
- DCS and QC tools ready for data taking
- Detector settings optimized both for pp and PbPb collisions

- ITS2 is ready for RUN3



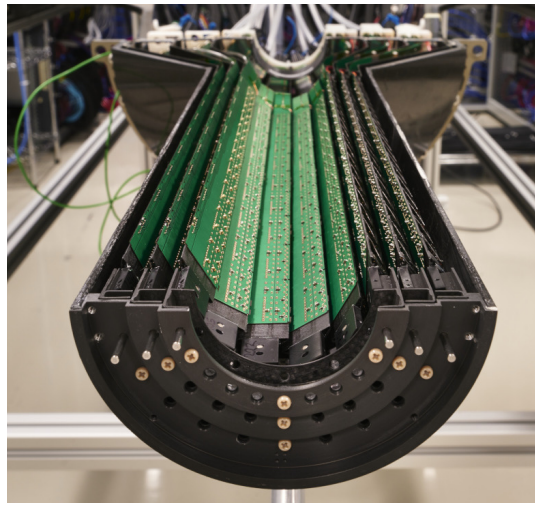
ALICE ITS2 Outer Barrel during insertion tests

ITS3

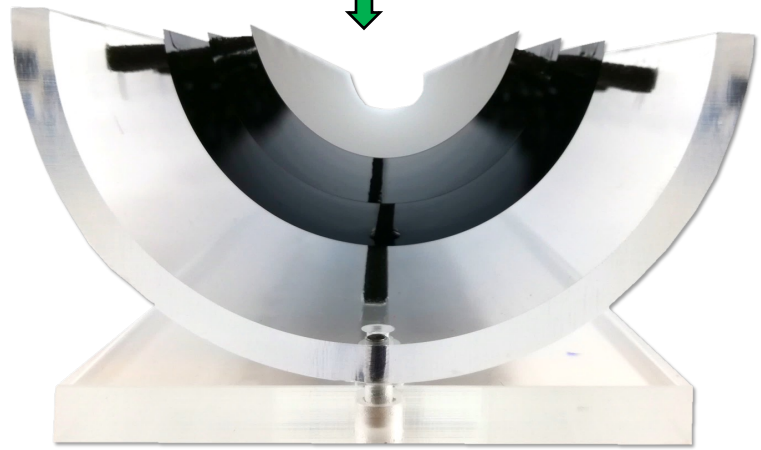
ITS3: all silicon new vertexer

LOI: CERN-LHCC-2019-018

- New detector technology:
  - three truly cylindrical Si pixel layers based on ultra-thin wafer-sized curved sensors (65 nm CIS technology)
  - no external connections nor cooling
  - new beam pipe
  - new concept for future detectors
- Performance:
  - Pointing resolution improves by a factor 2 compared to ITS2 in the full p_T range
  - Tracking efficiency increases by a factor 1.2-2 compared to ITS2 in p_T < 100 MeV/c



inner layers	ITS1	ITS2	ITS3
X/X_0	1.14%	0.36%	0.05%
innermost radius	39 mm	22 mm	18 mm
pixel size	50x425 μm^2	30x30 μm^2	O(15x15 μm^2)



Sensor Development Roadmap

Technology

TPSCo ISC 65 nm CMOS Imaging
300 mm wafers + Stitching

Silicon submissions

MLR1 (Q4 2020)

ER1 (Q2 2022)

- prototypes delivered Sep 2021
- characterization ongoing

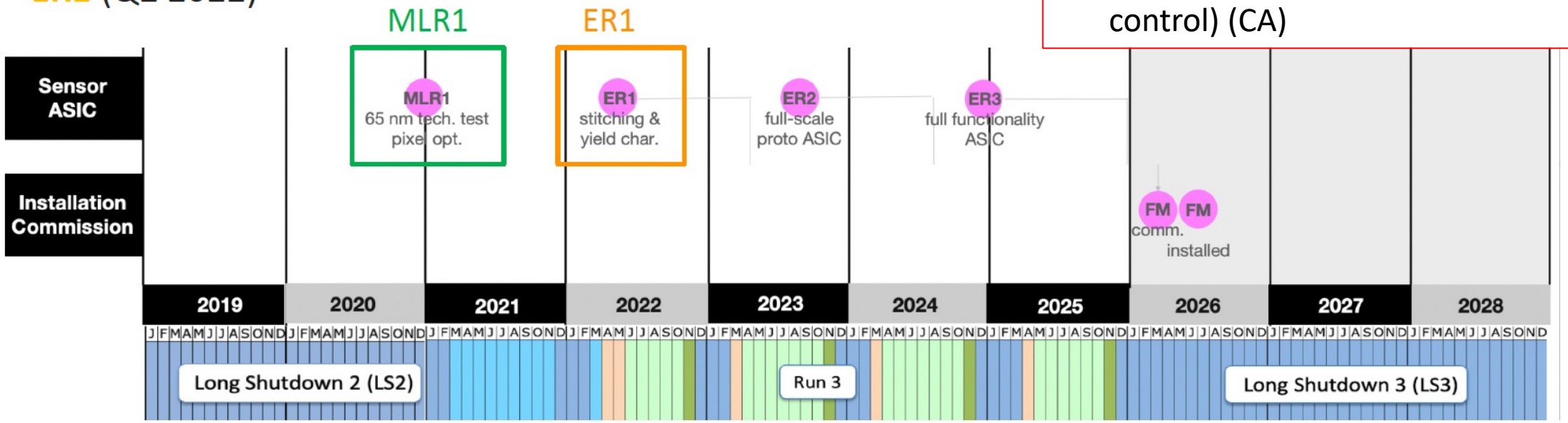
- **submission delayed to summer 2022 (165k€ from INFN)**

Design teams coinvolti nel progetto oltre al CERN:

- IPHC Strasbourg
- NIKHEF Amsterdam
- RAL, Univ. Birmingham

INFN contributions:

- Digital chip for seu and latchup tests (BA)
- Design of digital periphery (readout and control) (CA)



ITS3 road map

- large area
- stitched
- bent

Can we test each feature independently?

bend existing chips (ALPIDE)

caveat: ALPIDE technology 180nm CIS -> need to test bending on 65nm

large area wafers: 65 nm CIS

port charged particle CIS from 180 to 65nm -> MLR1

stitching in CIS for charged particles sensors (widely used for imaging sensors) -> ER1+ER2

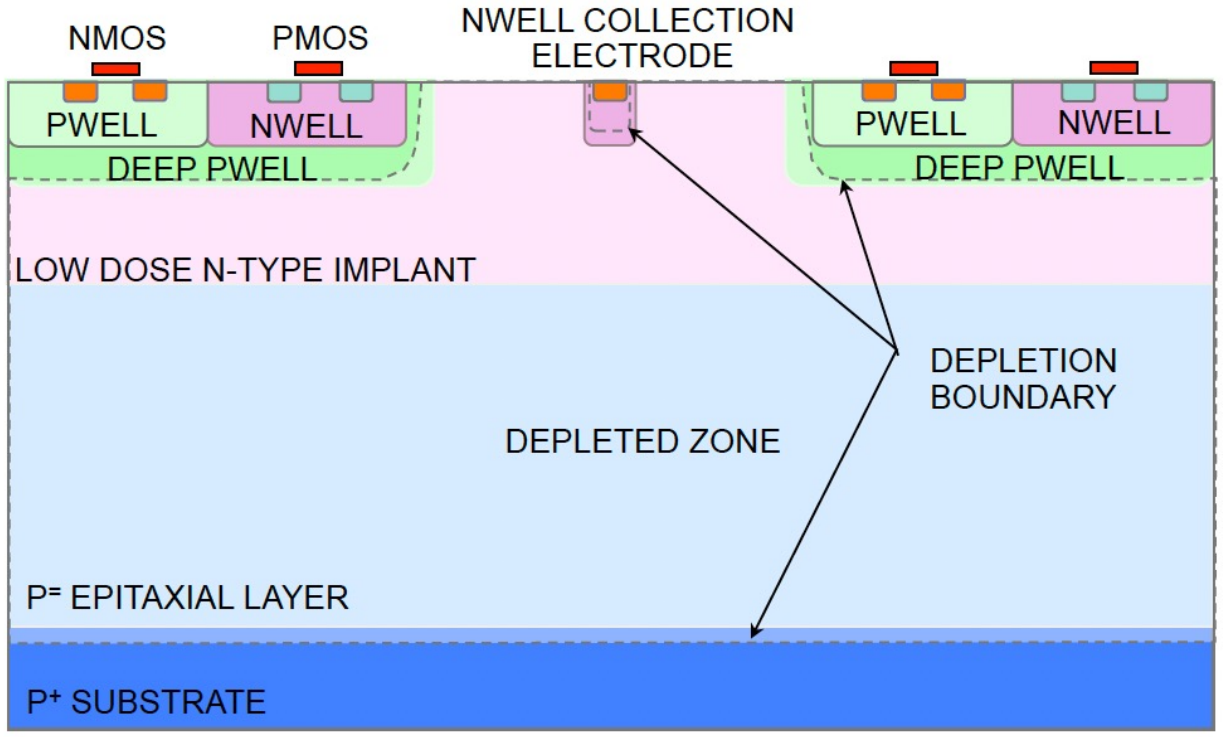
WP2+3: CHIP DESIGN AND CHARACTERIZATION

Sensor optimization

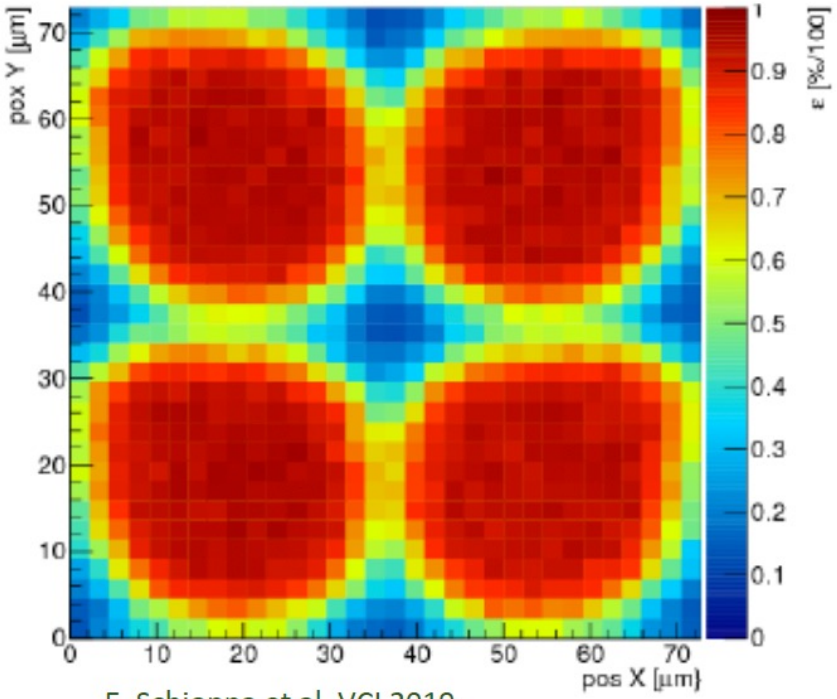
TowerJazz 180nm imaging CMOS technology

From 180nm to 65nm CIS

EP R&D



https://doi.org/10.1016/j.nima.2017.07.046 (180nm)



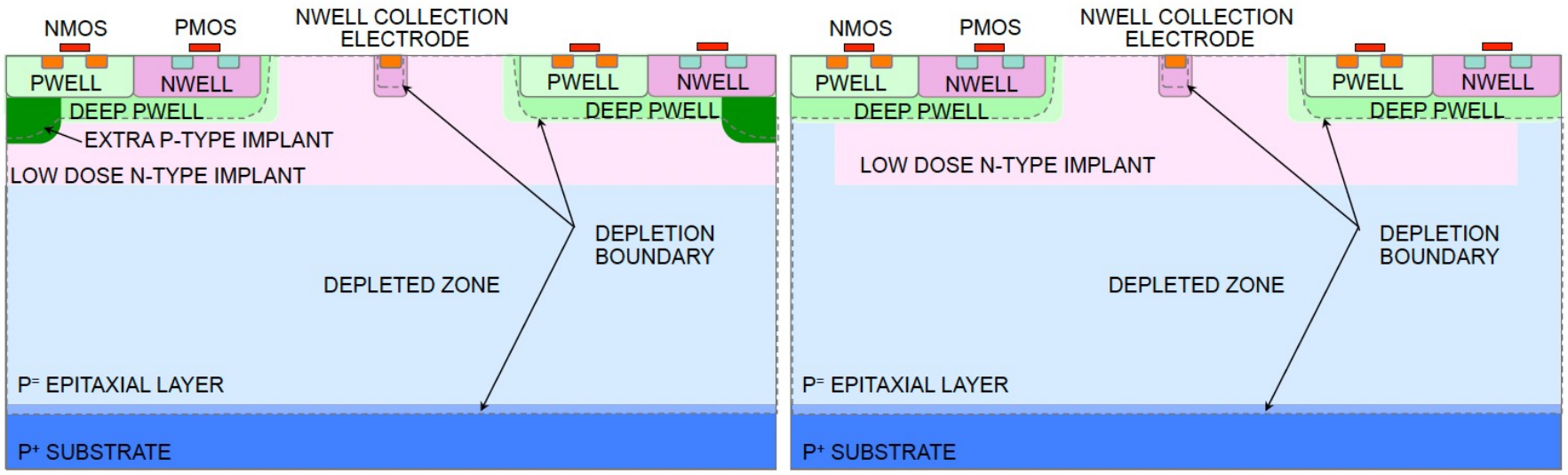
E. Schioppa et al, VCI 2019

- Side development in ALICE: move junction away from the collection electrode to deplete epitaxial layer
  - add deep low dose n-type implant -> radiation tolerance improved by an order of magnitude.
- After interest from ATLAS: MALTA/TJ MONOPIX development (Bonn, CPPM, IRFU and CERN)
- However, efficiency loss at ~ 10^{15} 1 MeV n_{eq}/cm^2 on the pixel edges and corners due to a too weak lateral field

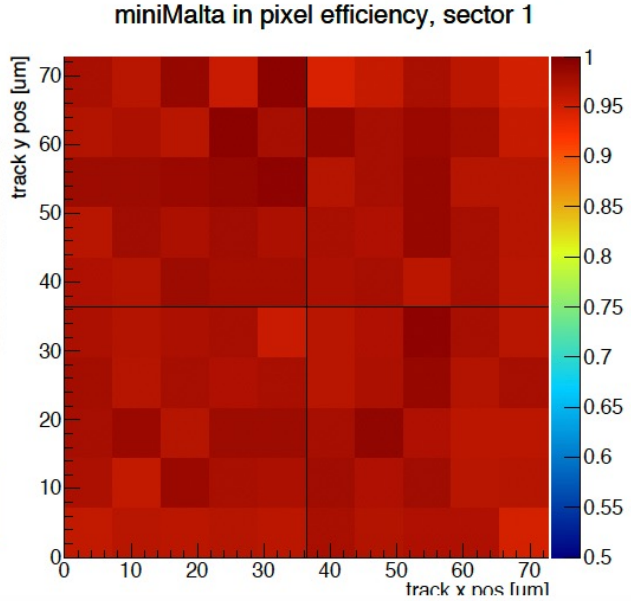
TCAD simulations and sensor optimization

TowerJazz 180 nm imaging CMOS technology

From 180nm to 65nm CIS



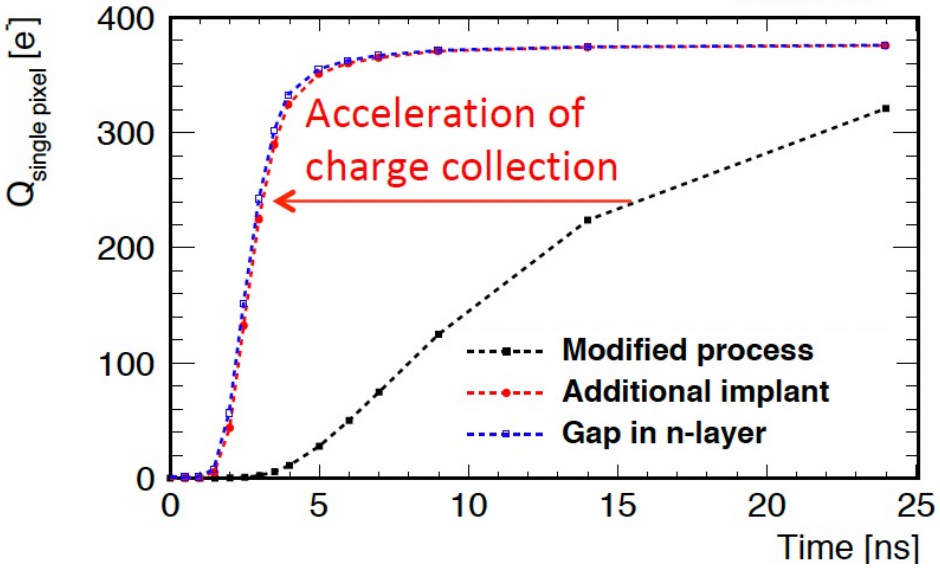
3D TCAD simulation M. Munker et al. PIXEL2018 https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013



Extra deep p-type implant or gap in the low dose n-type implant improves lateral field near the pixel boundary and accelerates the signal charge to the collection electrode. This yields:

- recovered efficiency at 10^{15} n_{eq}/cm^2
  H. Pernegger et al., Hiroshima 2019, M. Dyndal *et al* 2020 *JINST* **15** P0200
- more operating margin even before irradiation
- better sensor timing

- Monte Carlo using Garfield and Allpix² can generate distributions with reduced computation time compared to full TCAD



Moving to deeper submicron CMOS

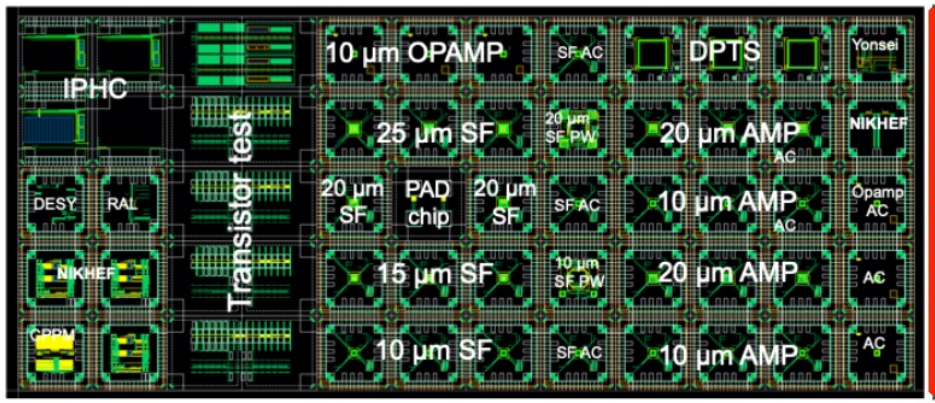
From 180nm to 65nm CIS

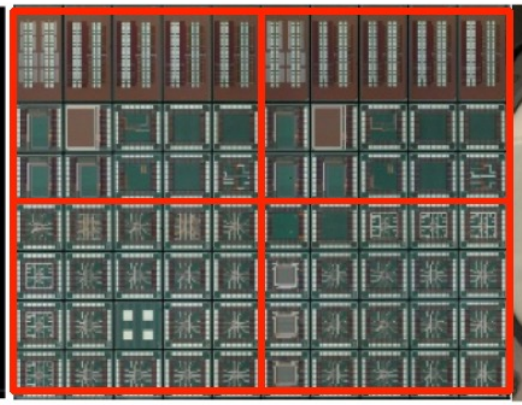
First technology selected: TPSCo 65 nm ISC

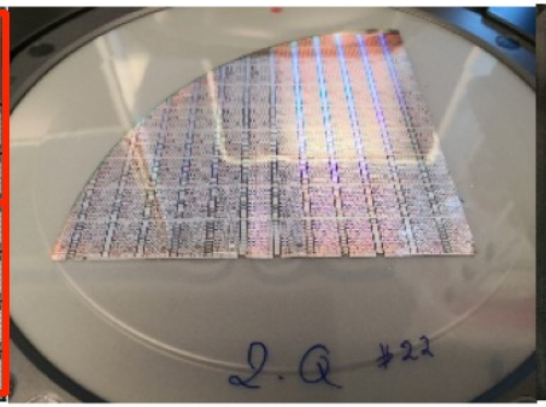
- TPSCo (joint venture TJ & Panasonic): several 65 nm flavors: high density logic, RF, and imaging (ISC)
- ISC preferred: 2D stitching experience, special sensor features, different starting materials, lower defect densities, etc
- Initially 5 metal layers, now 7 metals
- NDA (M. Campbell, L. Pocha & M. Ayass) for participating groups
- Finance Committee approval for stitched runs

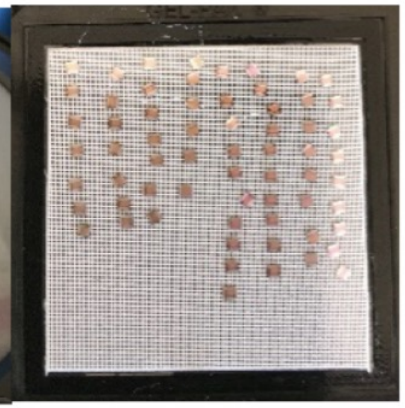
First submission: Multi Layer per Reticle MLR1 details in Gianluca's presentation

- Significant contribution from outside groups (from ALICE but not only) to design and test (!), also financially
- Many test chips of 1.5 x 1.5 cm^2 or twice that size.
- GDS submitted Dec 1, 2020, chips ready to test, Sept, 2021







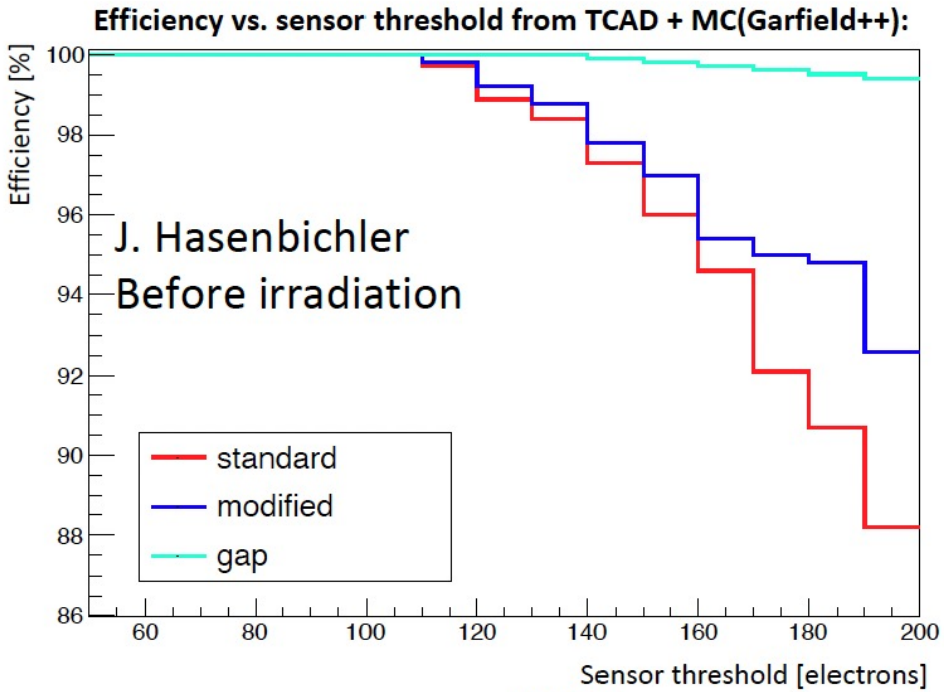


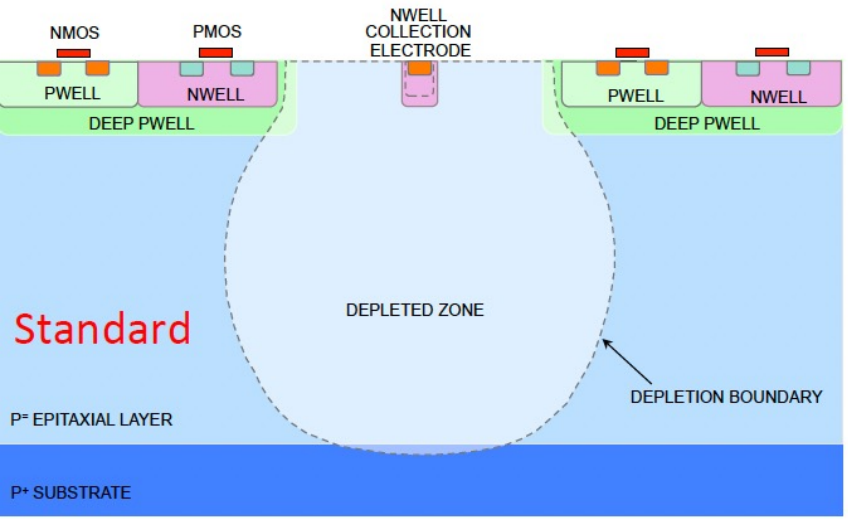
SPLITS for Multi Layer per Reticle MLR1

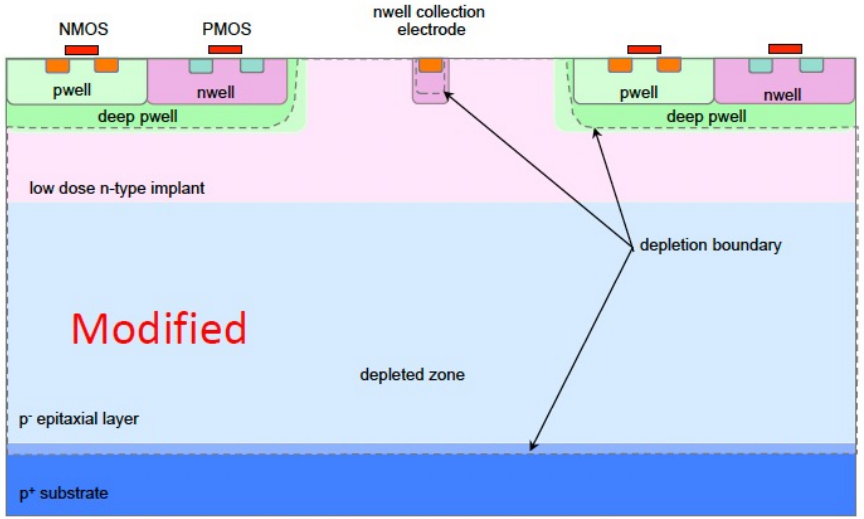
applying same optimization principles to 65 nm as in 180 nm

- 4 process splits, 3 wafers each
  - **Split 1: default process**
  - Split 2: first intermediate process
  - Split 3: second intermediate process
  - **Split 4: optimized process**
- 3 main pixel designs implemented in all splits
  - Standard similar in all splits, Modified, Gap

modifications more needed in 65 nm for good charge collection.







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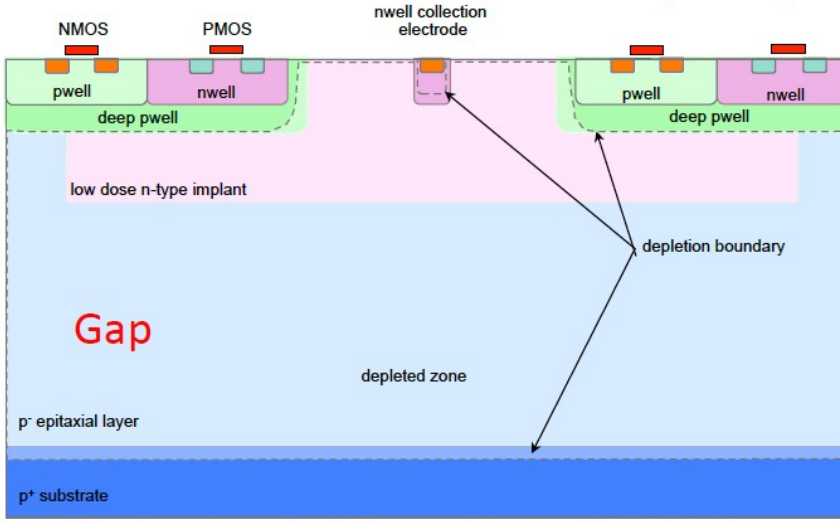


https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

Charge collection speed

Charge sharing

MLR1 Submission

EP R&D

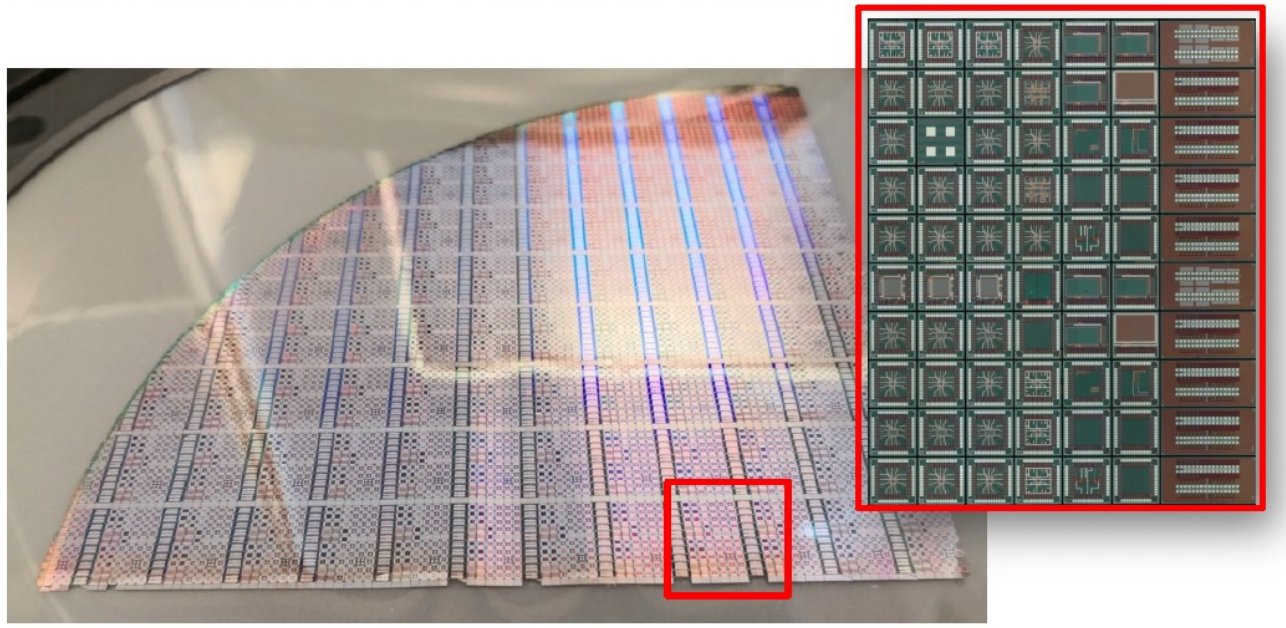
First submission in 65 nm CMOS Imaging, December 2020

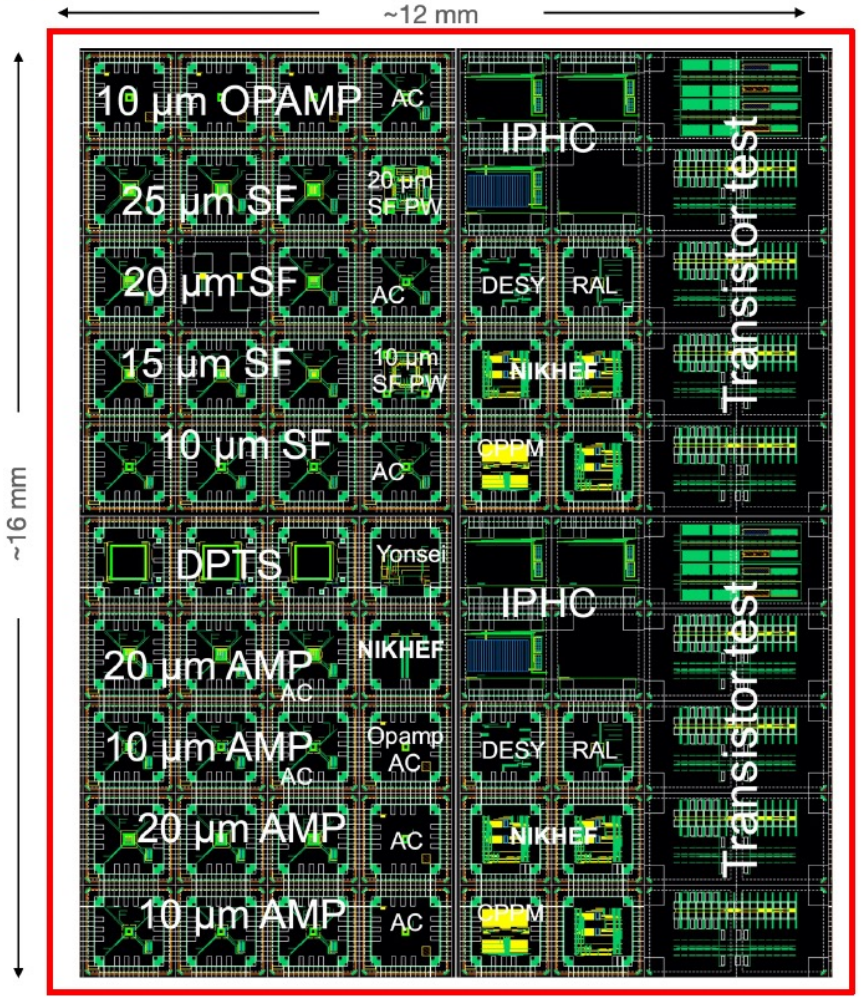
Learn technology features

Characterize devices

Prototype circuits, blocks and pixel structures

1.5 × 1.5 mm^2 or 3 × 1.5 mm^2 test chips



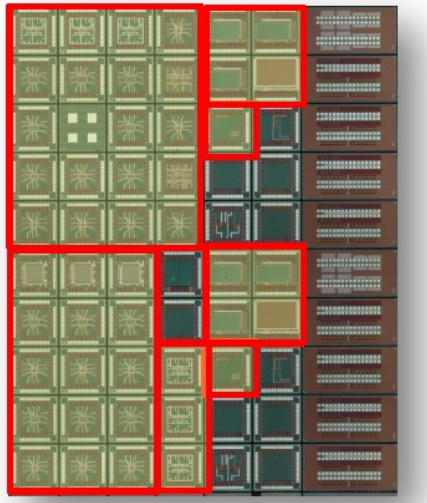


Pixel Prototype Chips

APTS, DPTS, CE65

Variants of collection diodes

Variants of Front-End



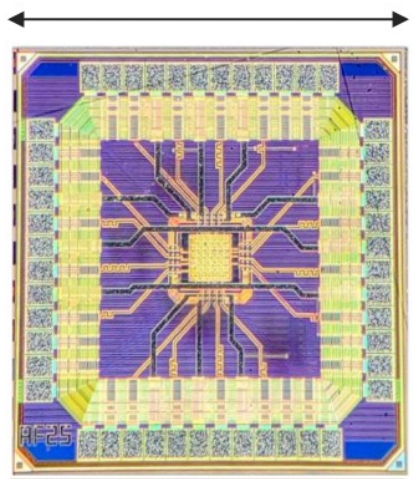
Front-End prototype

Charge Shaping Amplifier

Process Optimisation

Increase margins on sensing performance

Silicon proven pixels and DPTS front-end used as basis for stitched chip sensors in ER1



EP R&D

APTS

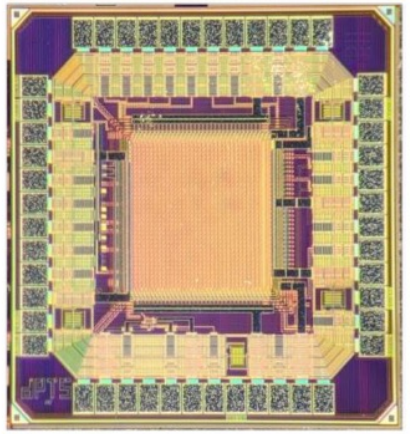
4x4 pixel matrix

10, 15, 20, 25 µm pitches

Pixel variants

Direct analogue readout

tested @ INFN



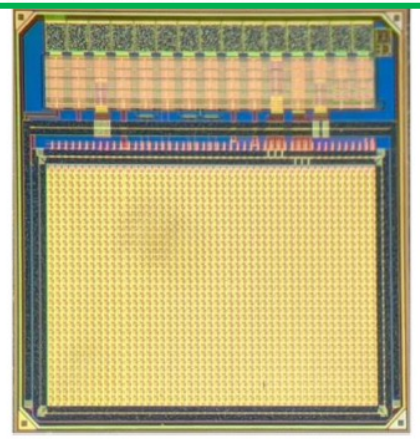
DPTS

32 × 32 pixels

15 µm pitch

Asynchronous digital readout

ToT information



CE65

64 × 32, 15 um pixels

48 × 32, 25 um pixels

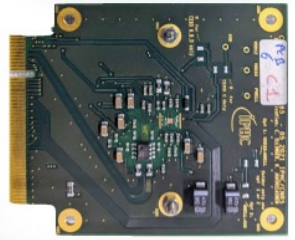
Rolling shutter analog readout

3 pixel front-end architectures

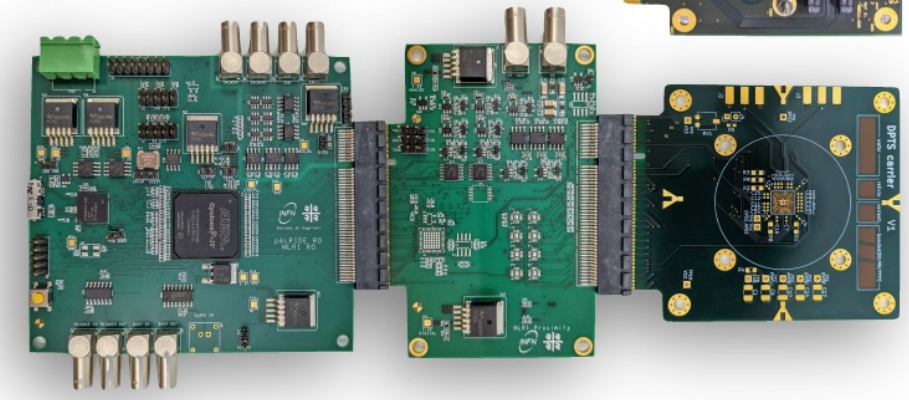
Readout system

ITS3 development

developed @ INFN CA-TO-TS (85k€ in 2021)



- Adaptation of existing readout system based on the DAQ boards that were used for ITS2 and ALPIDE
  - compatible with existing ALPIDE telescopes
  - affordable
- Newly produced proximity boards allow to set biases and read analog signals
- Uses simple chip carriers that are produced in large quantities (few hundreds)
  - essential to study large parameter space
- Distributed to a number of institutes



CERN + INFN (CA, CT, TO, TS) + IHPC (Strasbourg): pilot sites
BA+BO+PD + Nikhef + Liverpool + Birmingham: extensive test sites

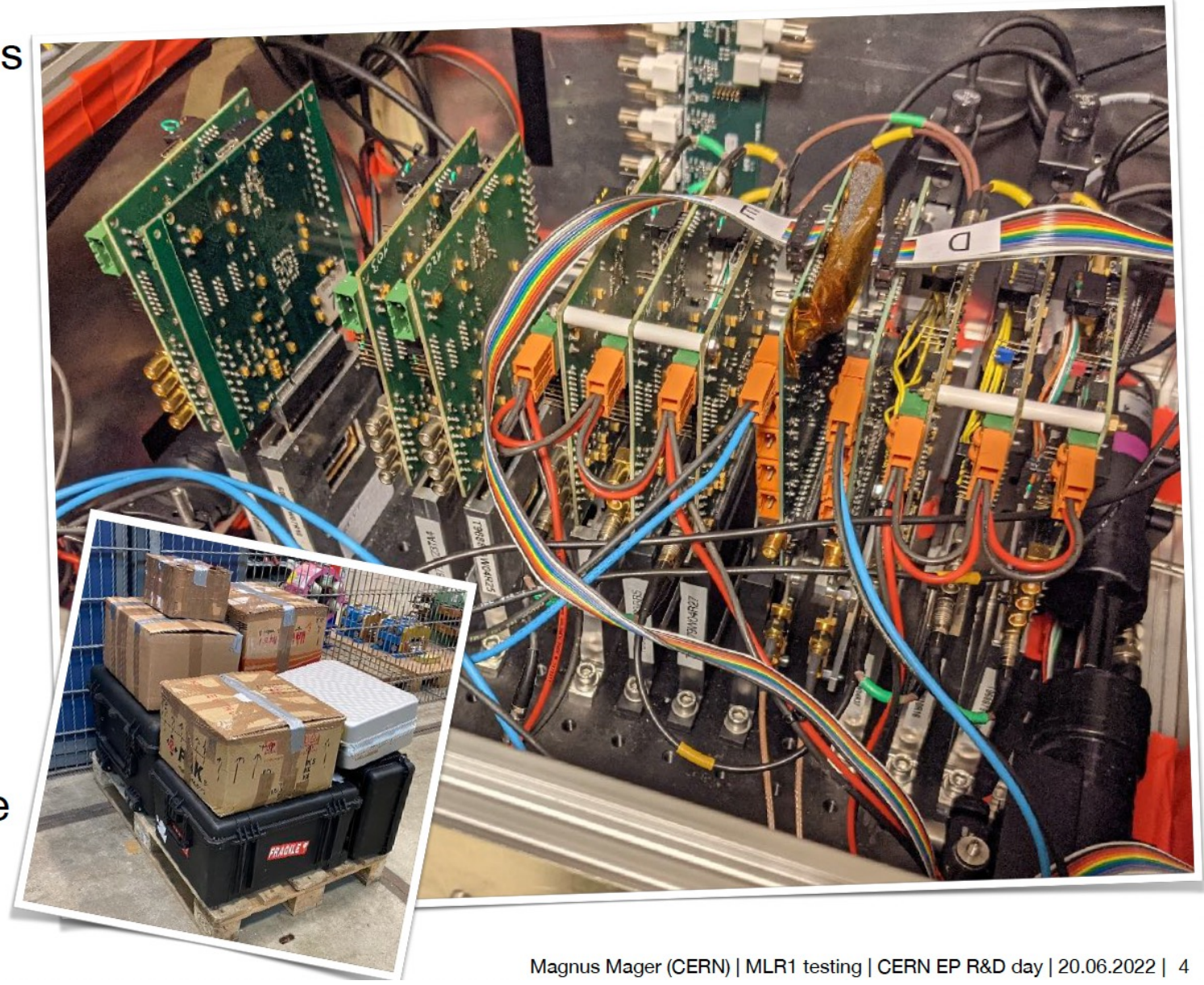
Test beams

ITS3 ALPIDE telescopes

- A large number of beam tests at various facilities (non-comprehensive list):
  - Sep 2021: DESY
  - Oct 2021: PS
  - Nov 2021: SPS
  - Dec 2021: DESY
  - Mar 2022: DESY
  - Apr 2022: MAMI
  - May 2022: PS
  - Jun 2022: PS
  - Jun 2022: SPS
- This is planned to continue at the same cadence

INFN participation

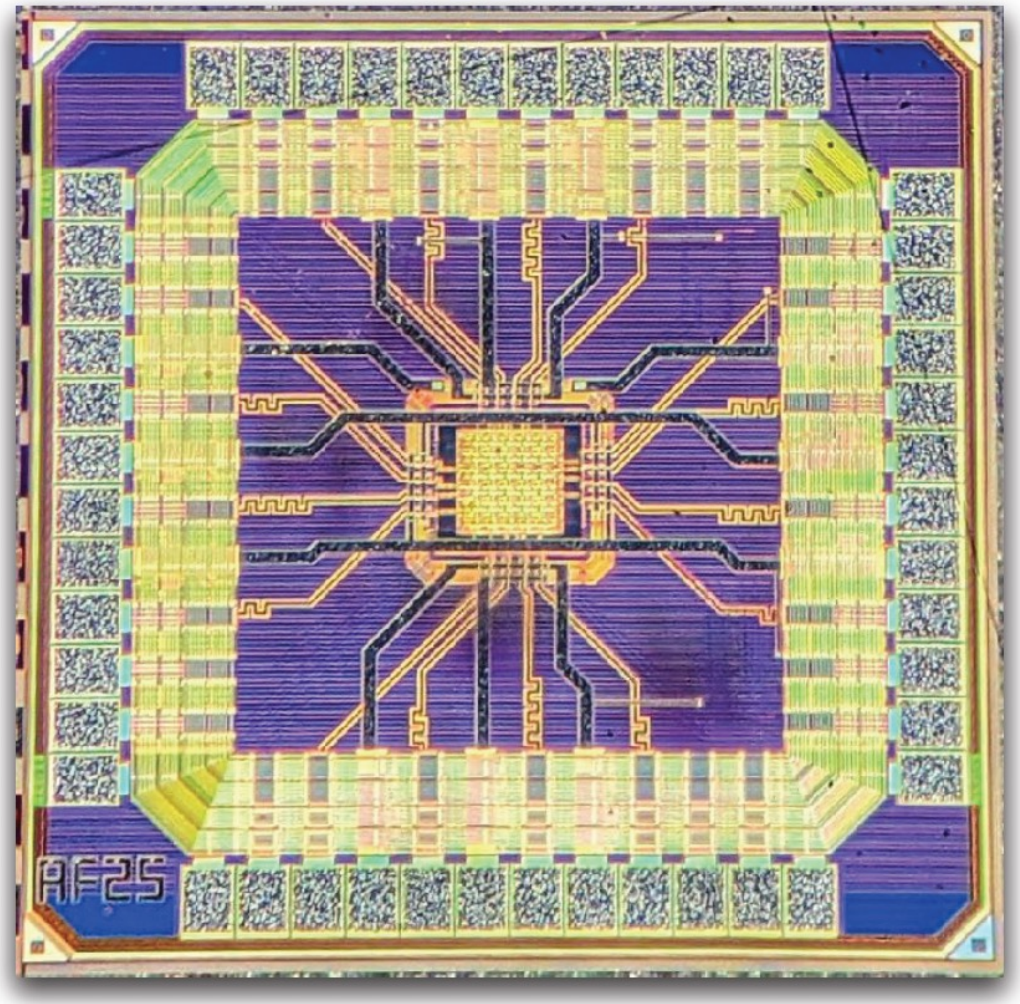
INFN participation



Analog Pixel Test Structure (APTS)

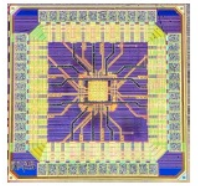
overview

- The analog pixel test structure (APTS)
  - 6x6 pixels (central 4x4 read out)
  - different pitches: **10, 15, 20, 25 µm**
  - different implant geometries
  - different output drivers:
    - OpAmp: very fast, driving 50 Ohm
    - source follower (SF): more classical
- Allows for very detailed mapping of parameters space
  - important e.g. in view of larger pixels
  - also key to verify and tune simulation models



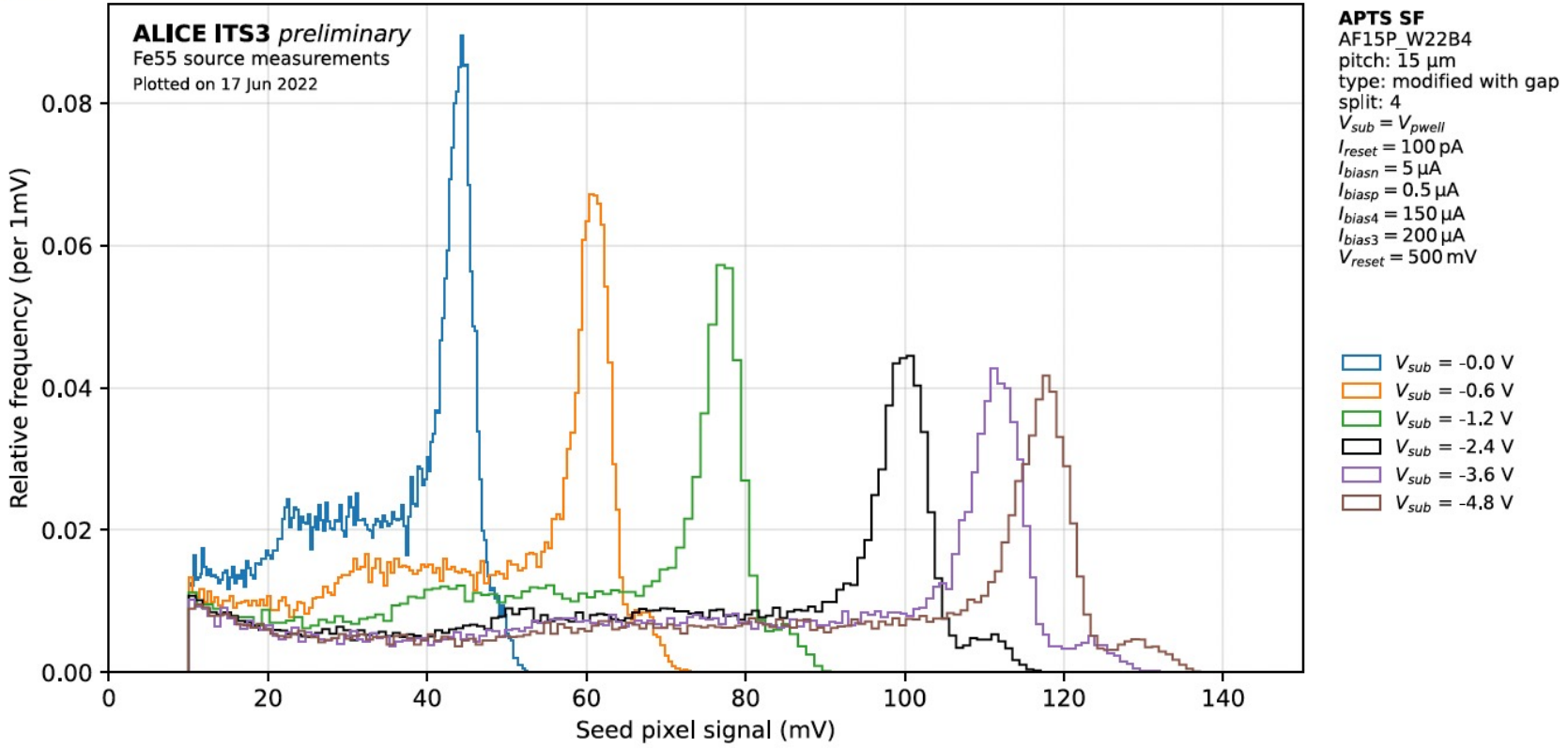
APTS SF – Fe-55 lab tests

comparison reverse bias voltages



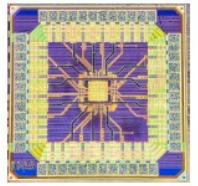
- The capacitance of the sensor can be lowered by increasing the substrate bias
- Values down to 2.2 fF are observed

Source follower tested in CT+CERN

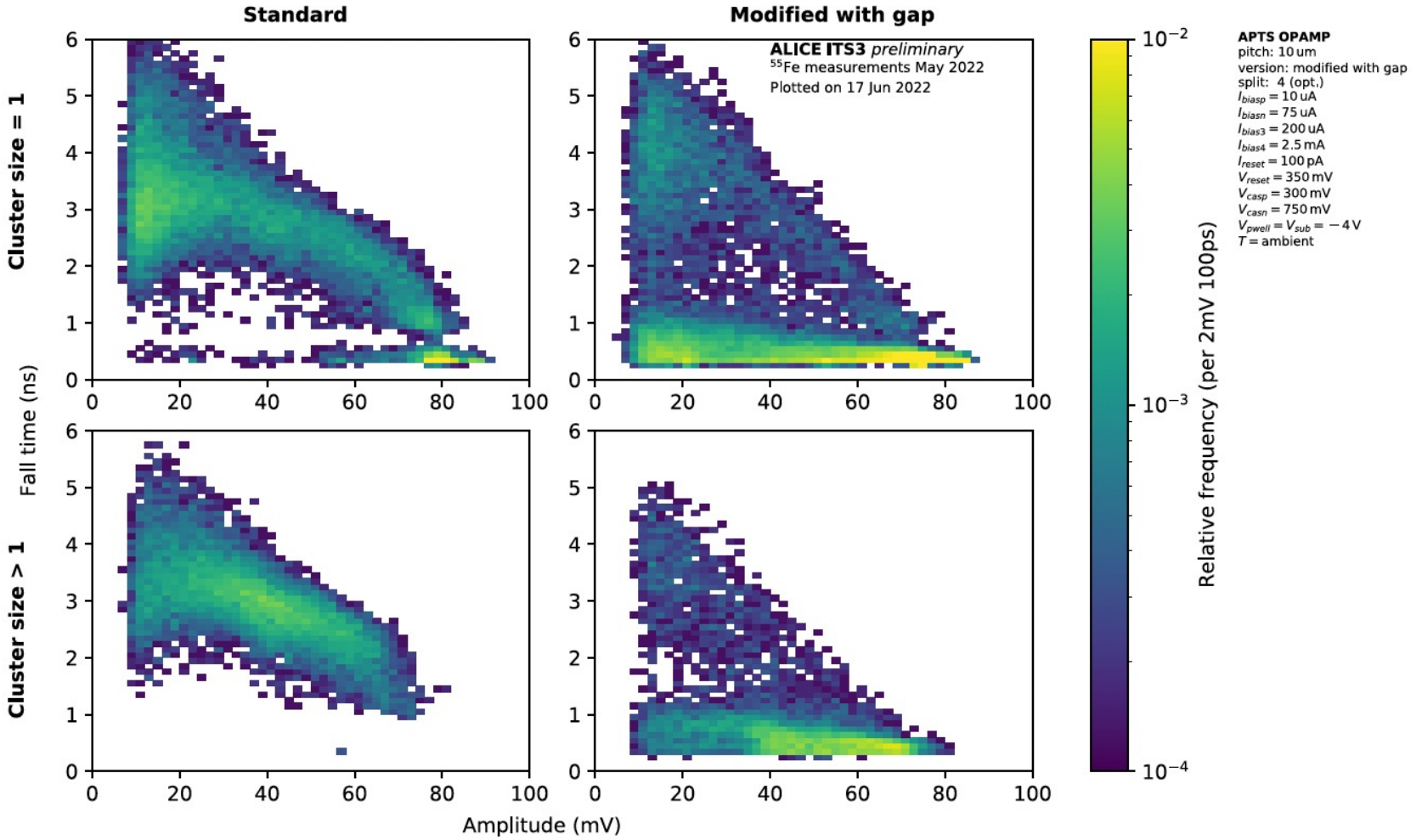


APTS OpAmp – Fe-55 lab tests

comparison of process modifications



- Clusters of different sizes show distinct fall time and amplitude distributions
- Nice demonstration of the change in charge collection
- Test beam is underway to measure the timing performance

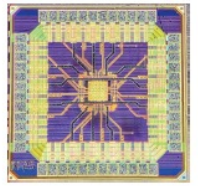


OPAMP tested in Torino

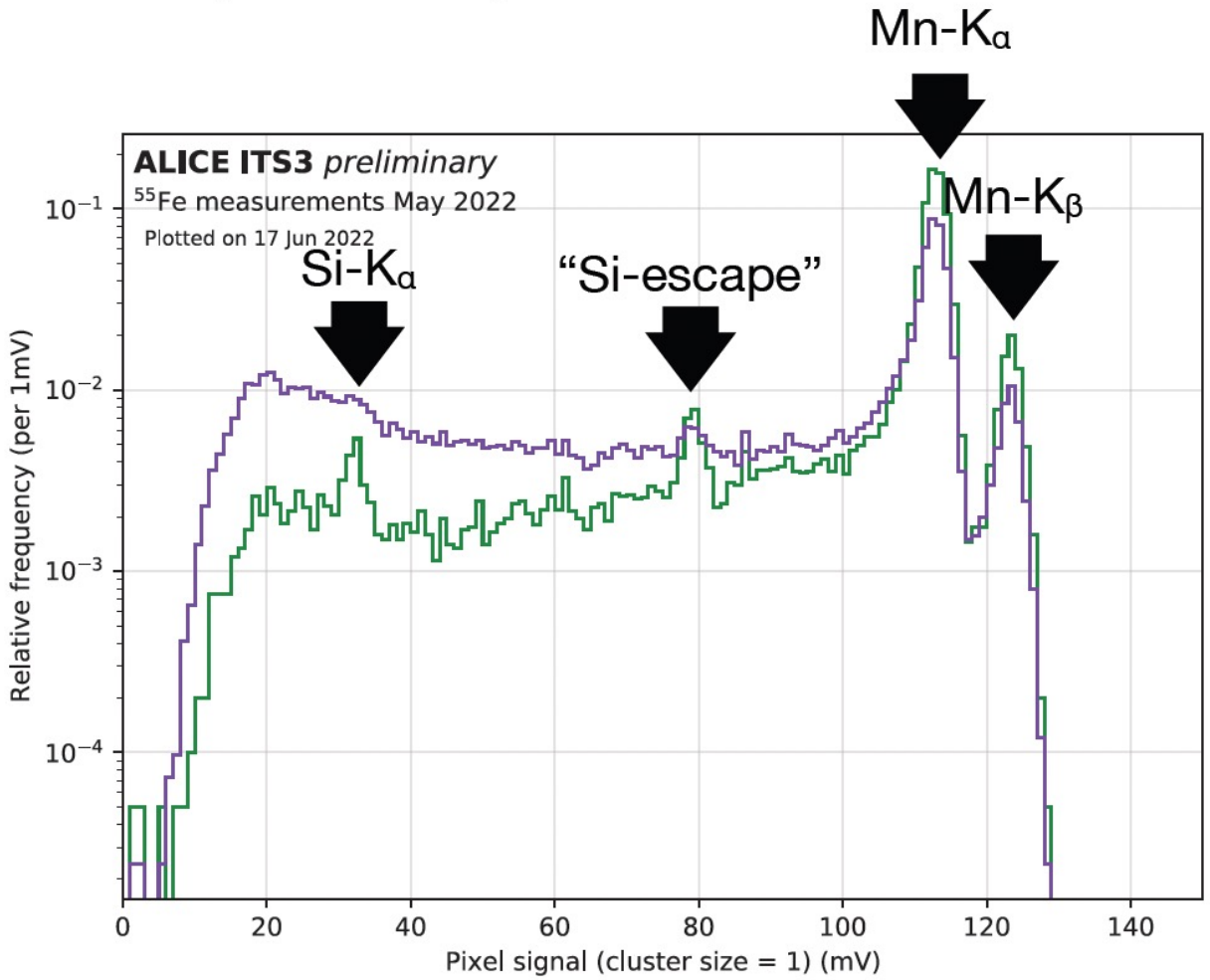
It can be nicely seen how the charge collection is accelerated with the process modification!

APTS OpAmp – Fe-55 lab tests

comparison of pitches (modified process)



- By applying a timing cut on the charge collection, spectra can be enhanced
  - selection of events where charge is collected quickly
  - likely because the conversion happens close the electrode



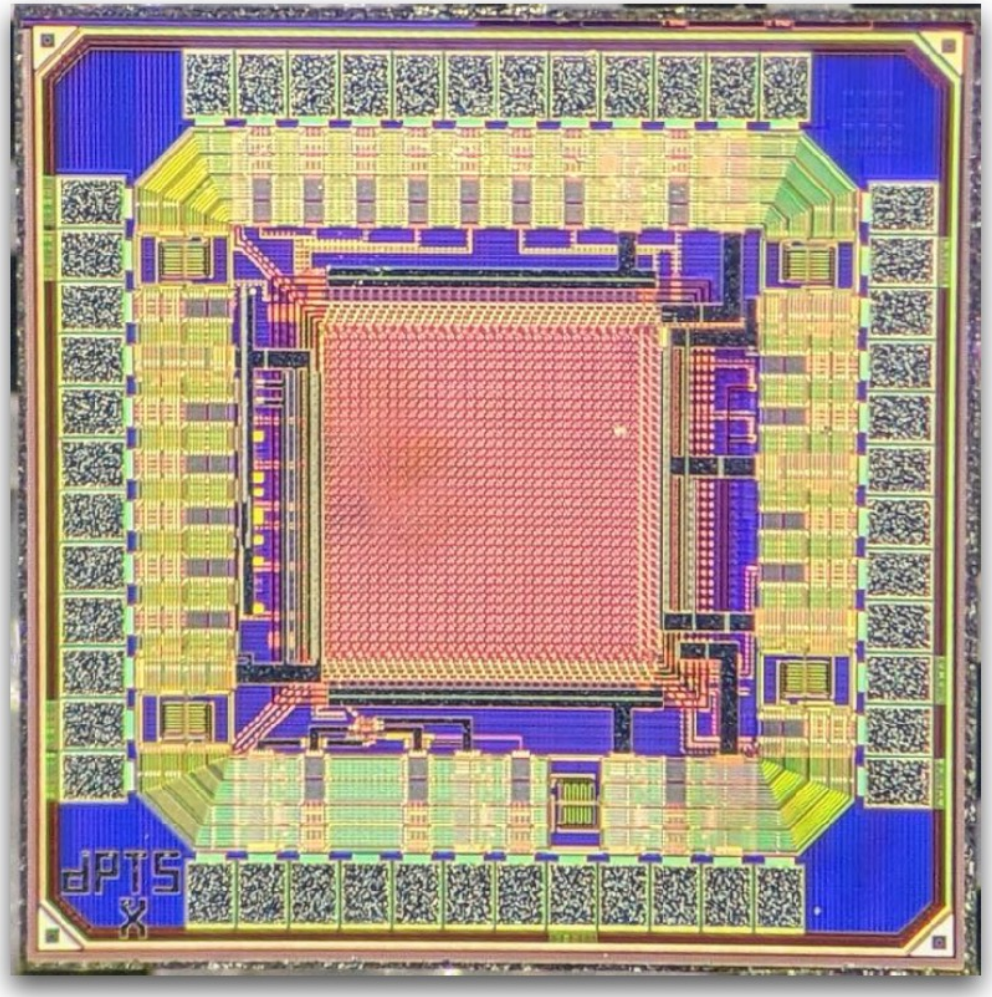
OPAMP tested in Torino

Digital Pixel Test Structure (DPTS)

overview

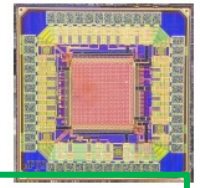
- The digital pixel test structure (DPTS)
  - 32x32 pixels
  - pitch: 15 µm
  - using most-optimised geometry (“P” variant)
  - 3 different readout circuit variants
- Includes a full digital front-end within each pixel
  - asynchronous digital readout
  - time-over-threshold information

DPTS tested in TS + CERN

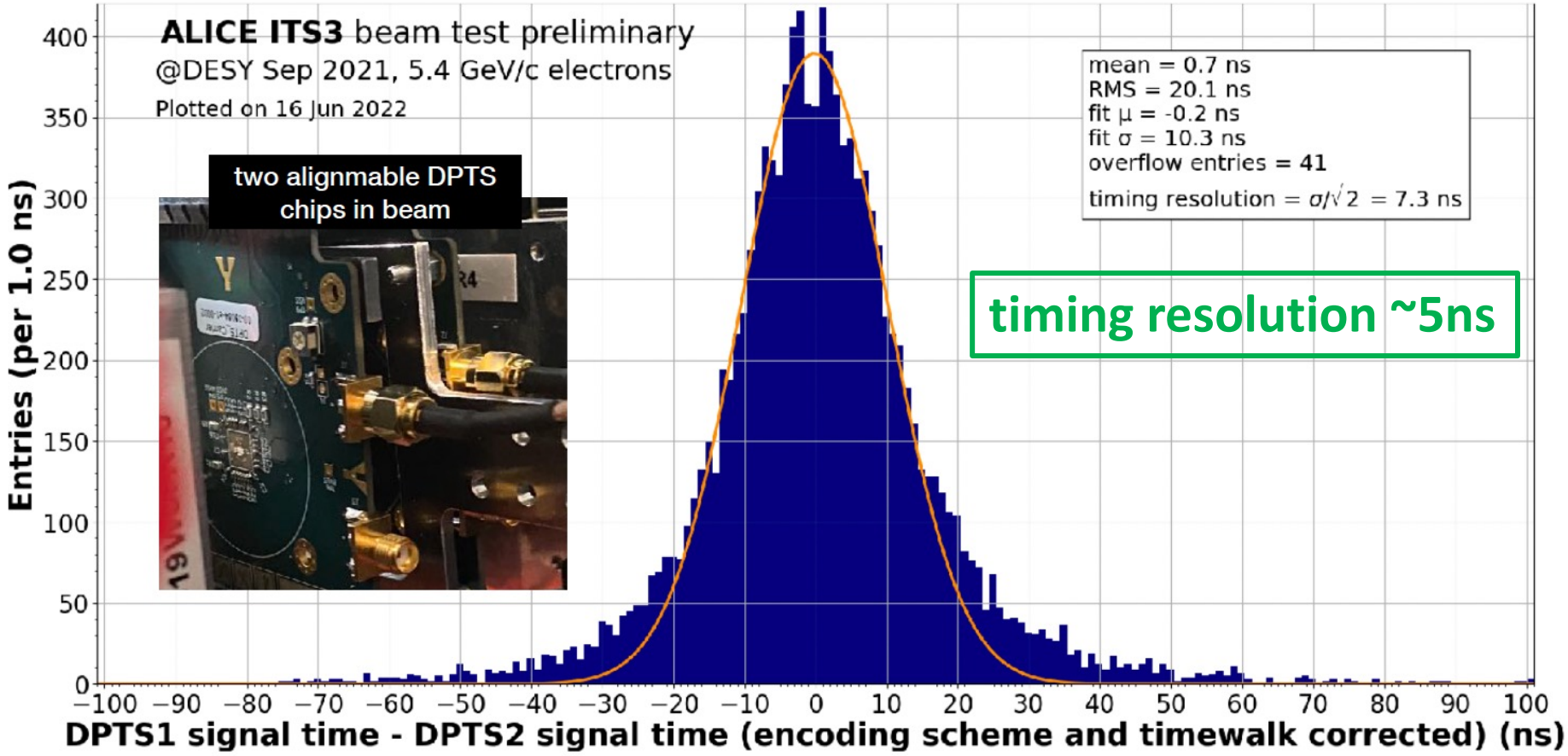


DTPS – time resolutions

coincidence between two chips



DPTS tested in TS + CERN



timing resolution ~5ns

DPTSOW22B3 (not irradiated)
version: O
split: 4 (opt.)
I_{reset} = 10 pA
I_{bias} = 100 nA
I_{biasn} = 10 nA
I_{db} = 100 nA
V_{casn} = 300 mV
V_{casb} = 250 mV
$V_{pwell} = V_{sub} = -1.2$V

DPTSXW22B1 (not irradiated)
version: X
split: 4 (opt.)
I_{reset} = 10 pA
I_{bias} = 100 nA
I_{biasn} = 10 nA
I_{db} = 100 nA
V_{casn} = 300 mV
V_{casb} = 280 mV
$V_{pwell} = V_{sub} = -1.2$V

Even at moderate front-end currents, very good (sub-LHC BC) resolutions are obtained

MAIN RESULTS MLR1 65 nm

Milestone: completamento caratterizzazione MLR1 - 20% a giugno 2022. Ritardo dovuto a difficoltà di reperimento componenti per test set-up v2. Milestone spostanta a giugno 2023

Functionality

- Fully efficient sensor, analog front end, digital readout chain in 15 x 15 μm^2 pixel (DPTS) including sensor optimization
- Sensor optimization clearly accelerates charge collection
- Frontend tunable from 10 nA to 1 µA (power – time resolution tradeoff)
- Measurements at 100 nA, time resolution ~7.5 ns

Radiation effects

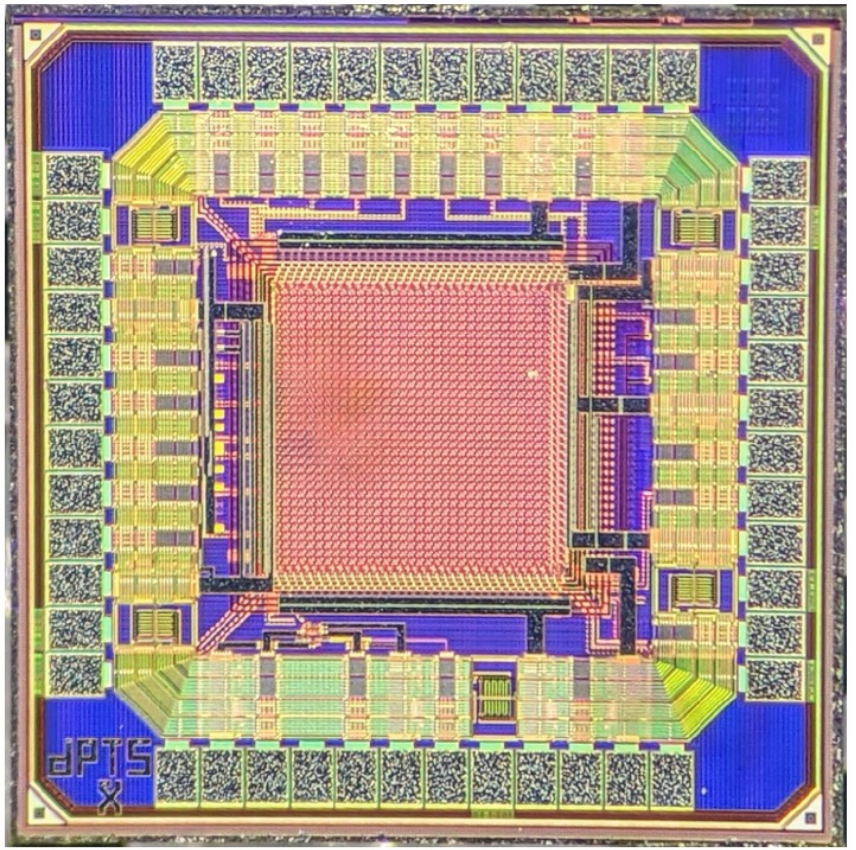
- Single event upset cross-section according to expectations
- Circuit radiation tolerance TID in line with other 65 nm technologies
- Sensor radiation tolerance NIEL: analysis in progress:
  - ~ 99% efficiency after 1e15 n_{eq}/cm^2 at room temperature
  - higher fluencies to be investigated, also at lower temperature

Building knowledge about this technology for general interest

- Very significant contribution from the ALICE experiment
- Towards full technology validation for our applications

Next submission Stitched Engineering Run ER1

- Learning about stitching and continue learning about the technology



these results allow the stitched chip designers to fix parameters for pixel size and FEE

ER1 Submission

August 2022

EP R&D

Aim: learn and prove **stitching**

Two large *stitched* sensor chips (MOSS, MOST)

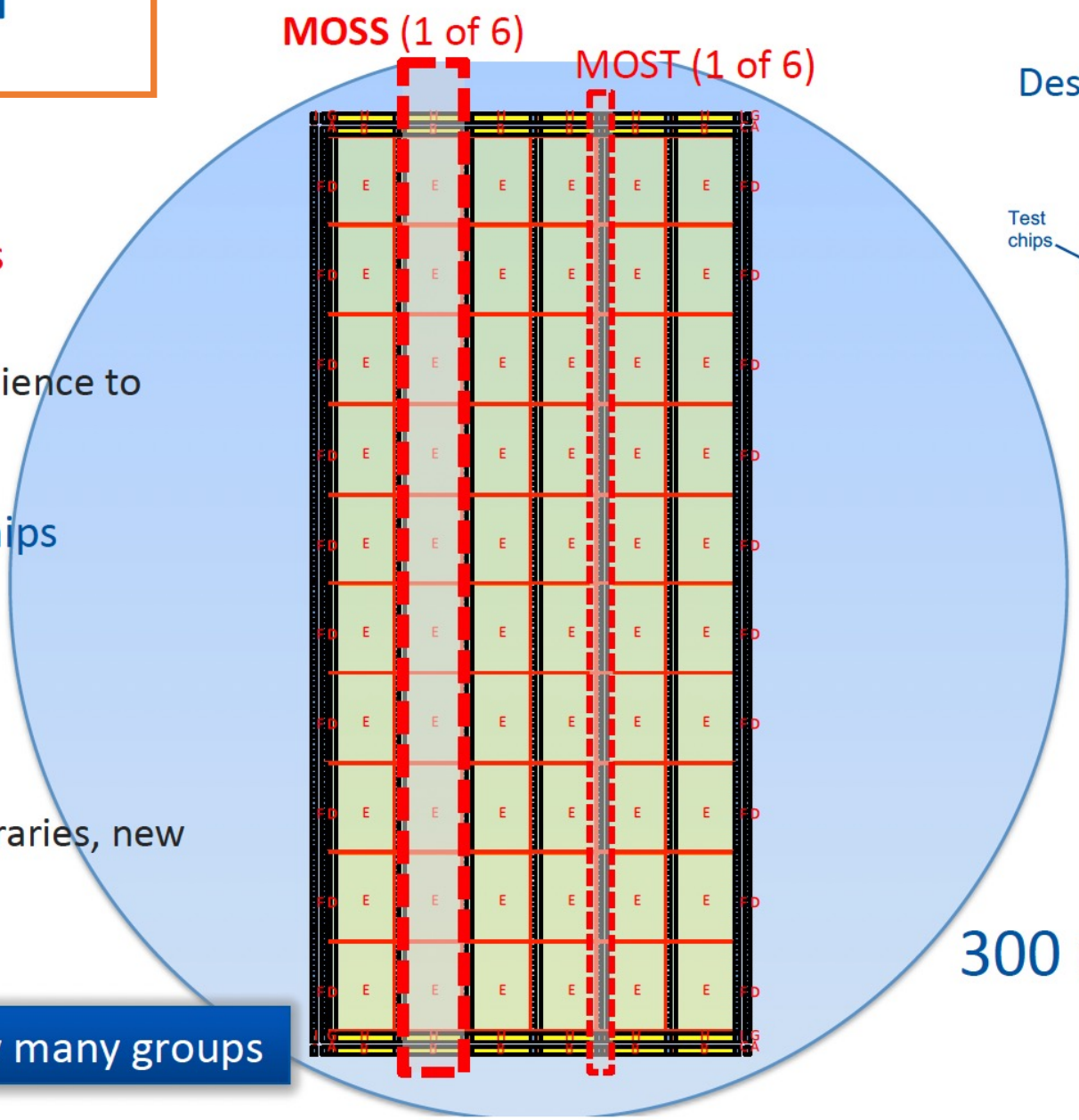
- Different approaches for resilience to manufacturing faults

Small test and development chips

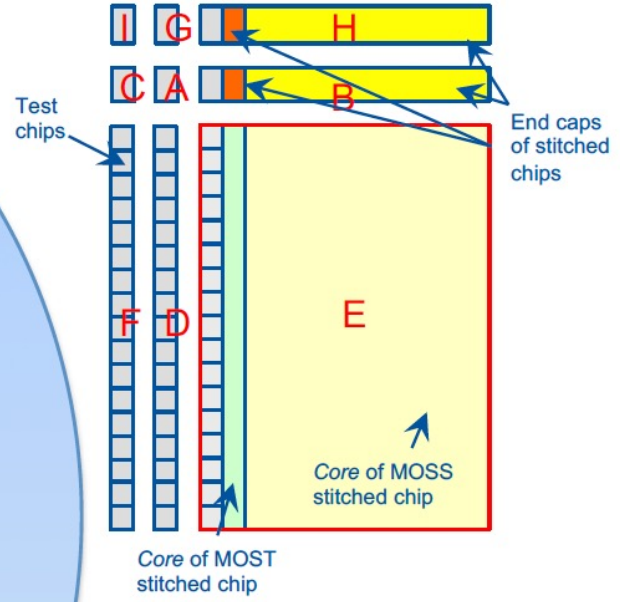
- Pixel Prototypes
- Fast Serial Links

Technology and Support

- New metal stack, new I/O libraries, new PDKs



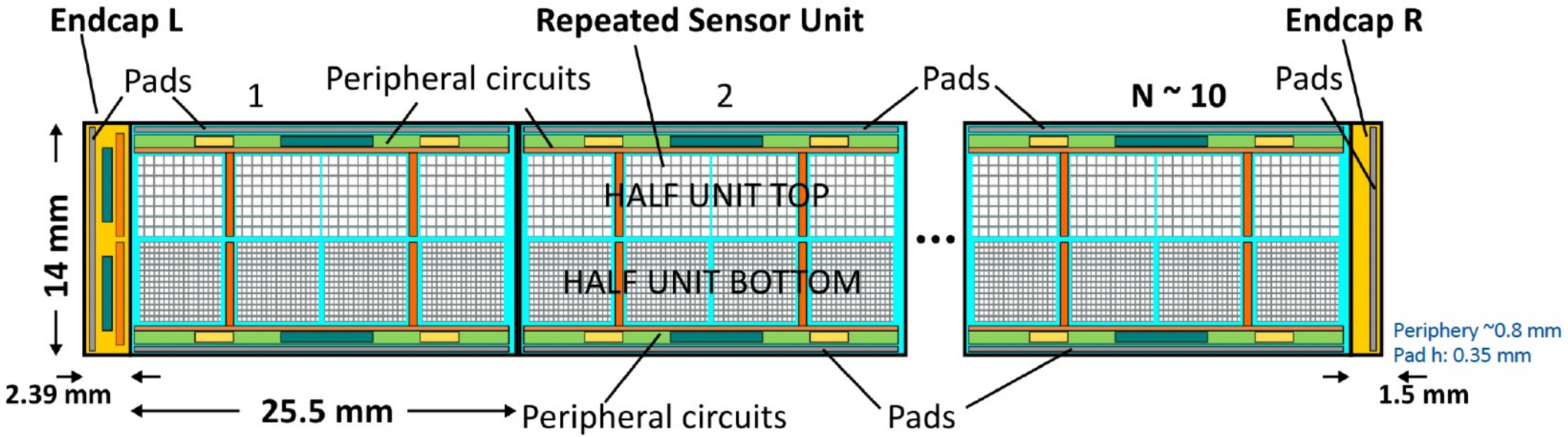
Design Reticle



300 mm wafer

Intense design effort shared by many groups

MOSS Monolithic Stitched Sensor Prototype



Primary Goals
Learn Stitching technique to make a particle detector
Interconnect power and signals on wafer scale chip
Learn about yield and DFM
Study power, leakage, spread, noise, speed

Repeated units abutting on short edges

- Functionally independent
- Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**

MOST chip

EP R&D

Investigate yield when local density is preserved

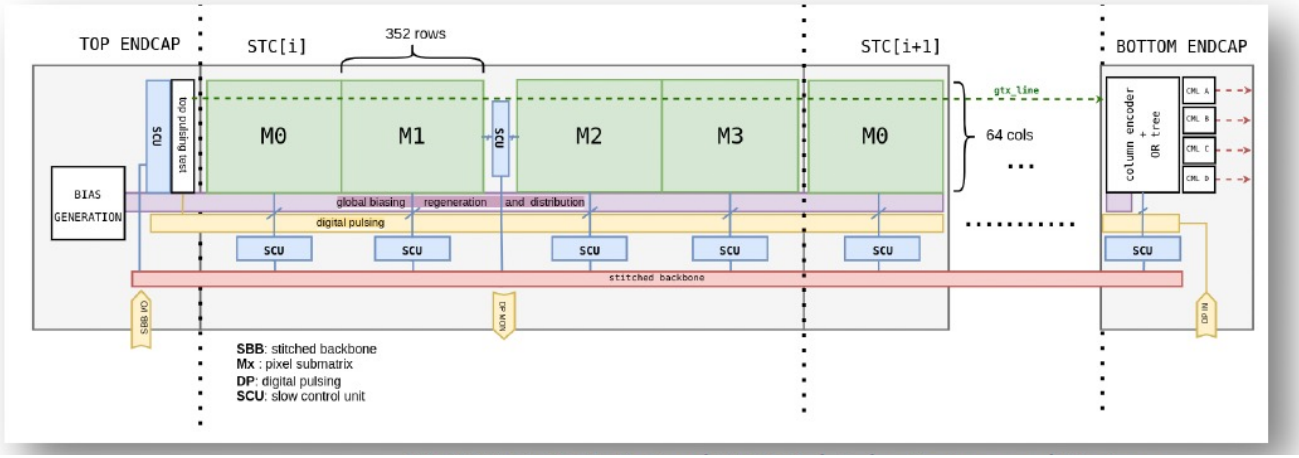
- Global power domains over full chip (Digital/Analog)
- Power gating with high granularity to mitigate defects

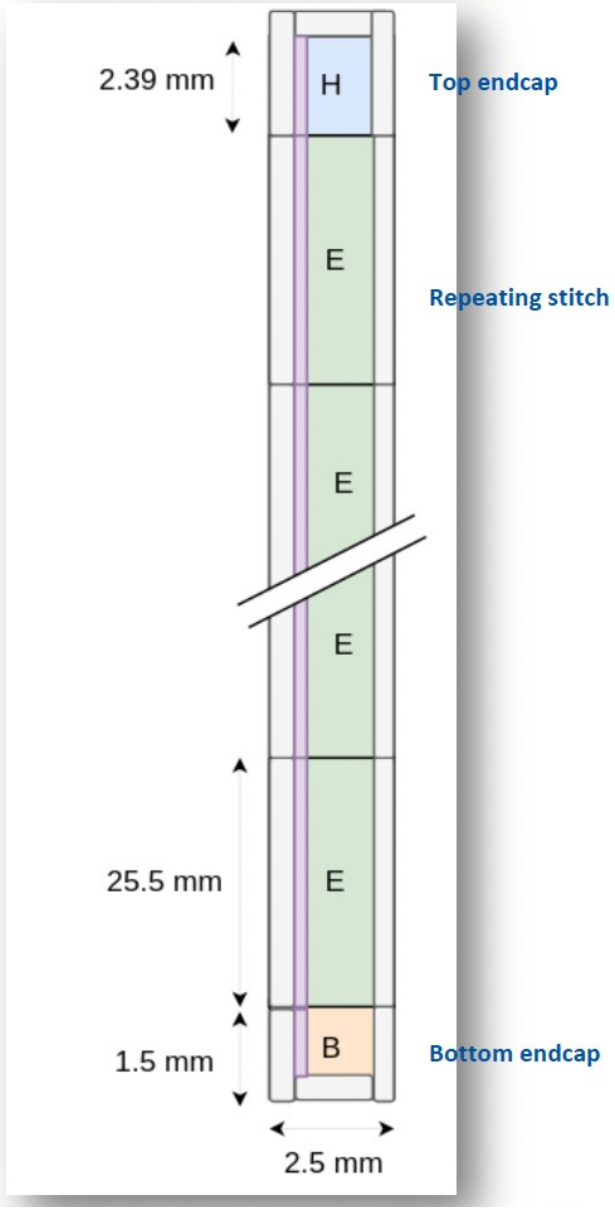
Larger sensor bias achieved by higher power supply

- PWELL tied to ground

Event-driven asynchronous readout

- No global shutter/strobe
- Immediate transmission of hit data over long distance to the periphery
- 4 CML outputs in the bottom endcap





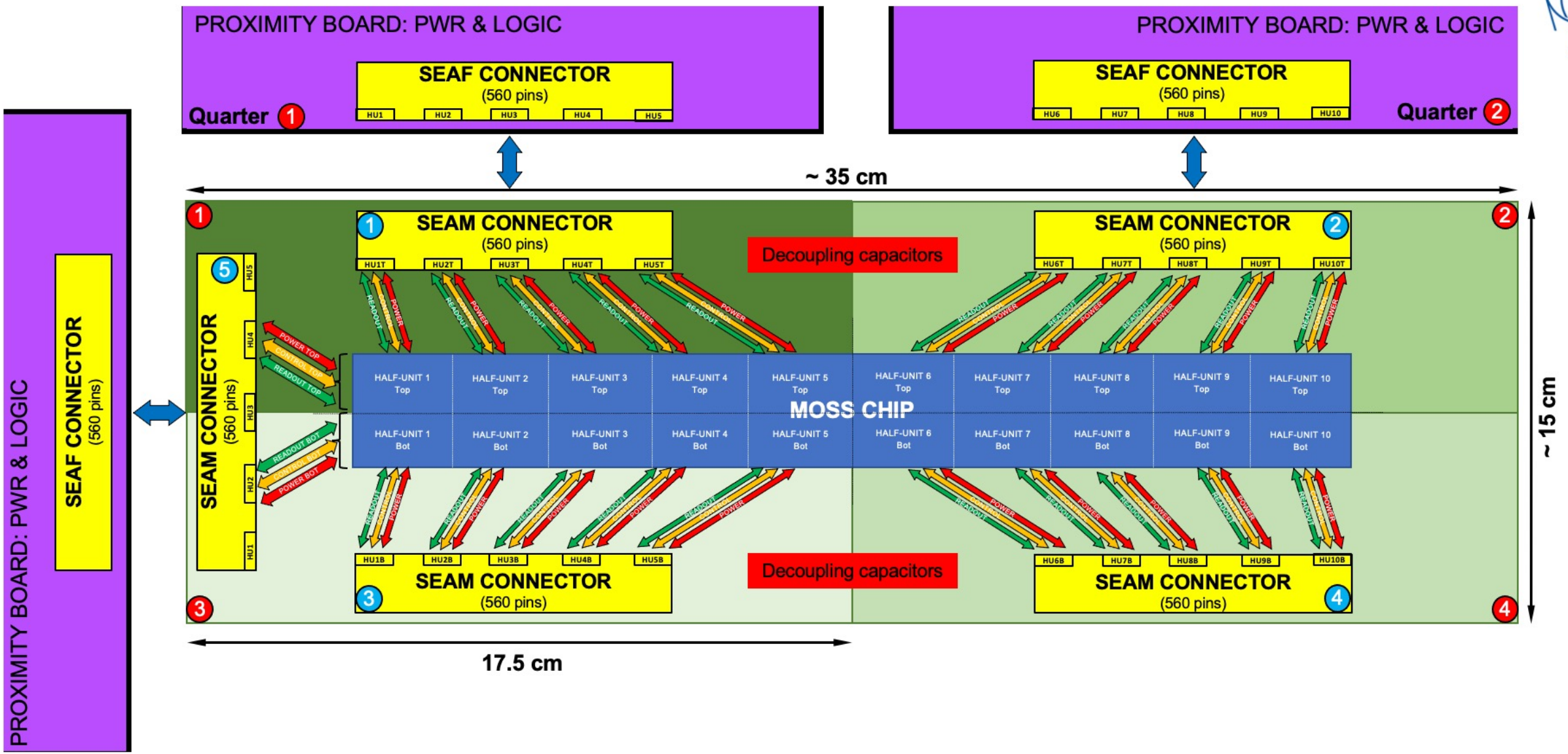
MOSS test system

- Aim: power and read out independently each sensor unit

Consists of:

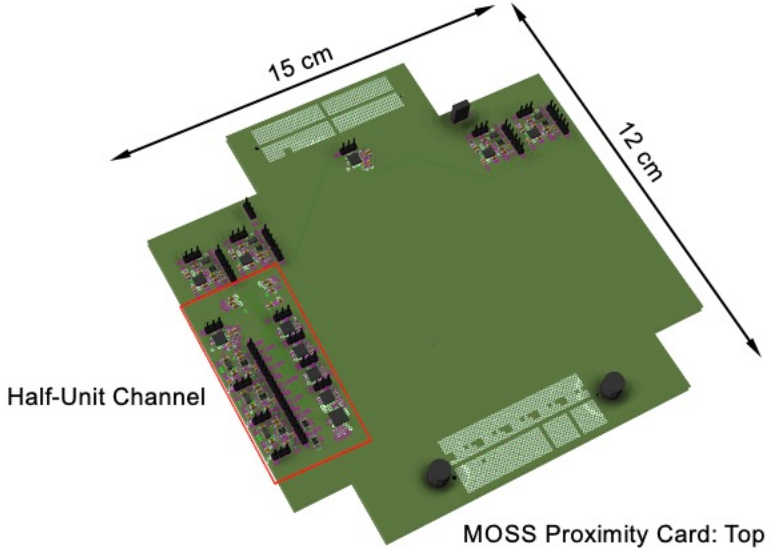
- Fully passive carrier card
- 5 proximity boards + 5 readout cards
- read-out card: control and automate testing.

FULLY PASSIVE CARRIER CARD

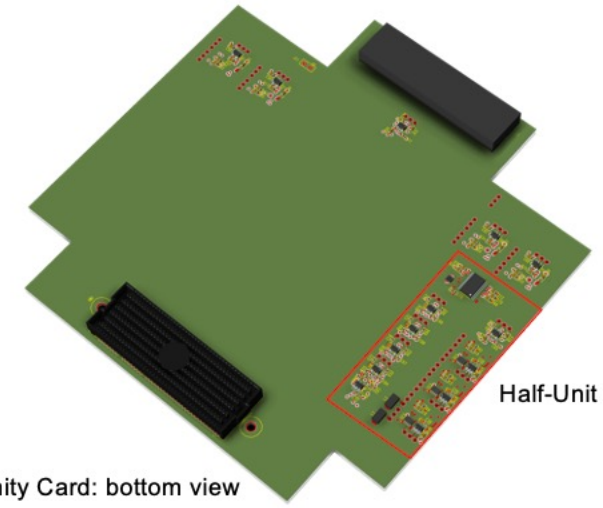


PROXIMITY BOARD STATUS

- Schematic achieved for one of the 5 Half-Unit
- The layout is in progress, the routing of one Half-Unit has been done
- All the active components have been ordered and received
- SEAF SAMTEC connectors have been ordered and are expected end of July



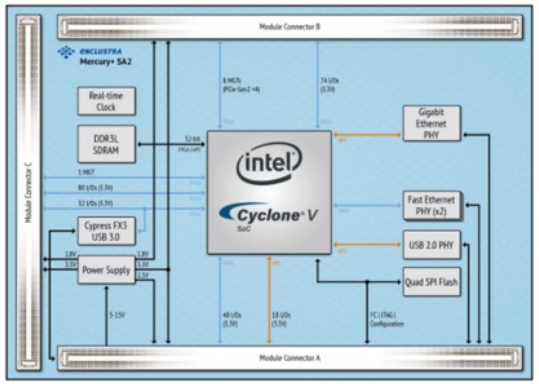
MOSS Proximity Card: Top view



MOSS Proximity Card: bottom view

READ OUT CARD

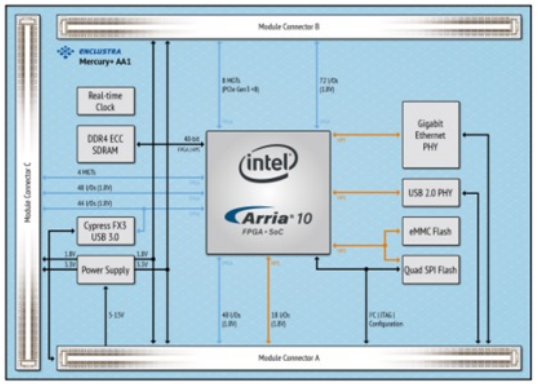
PROCURED: 1 unit of PE1-300 and 1 unit of Mercury UX8, prototyping
ORDER PLACED and ACCEPTED: for 12 boards. 2 end of May, 10 November.



Mercury+ SA2

Mercury+ SA2 Features:

- Intel Cyclone® V ARM® Processor-based SoC FPGA
  - ARM® dual-core Cortex™-A9
  - (32 bit, up to 800 MHz)
  - Intel Cyclone V 28nm FPGA fabric
- Small form factor (74 × 54 mm)
- 294 user I/Os
  - 18 ARM peripheral I/Os (2 × CAN, SPI, SDIO, 2 × I2C, 2 × UART)
  - 234 FPGA I/Os (single-ended or differential))
    - 202 FPGA I/Os
    - 32 FPGA I/Os shared with USB 3.0
  - 42 MGT signals (clock and data)
- 9 × 6.144 Gbps MGTs
- Up to 2 GByte DDR3L SDRAM
- 64 MB QSPI flash
- PCIe® Gen1/Gen2 x4
- Gigabit Ethernet
- Dual Fast Ethernet
- USB 3.0 device controller
- USB 2.0 device controller
- 2 × CAN, 2 × UART, SPI, 2 × I2C, SDIO/MMC

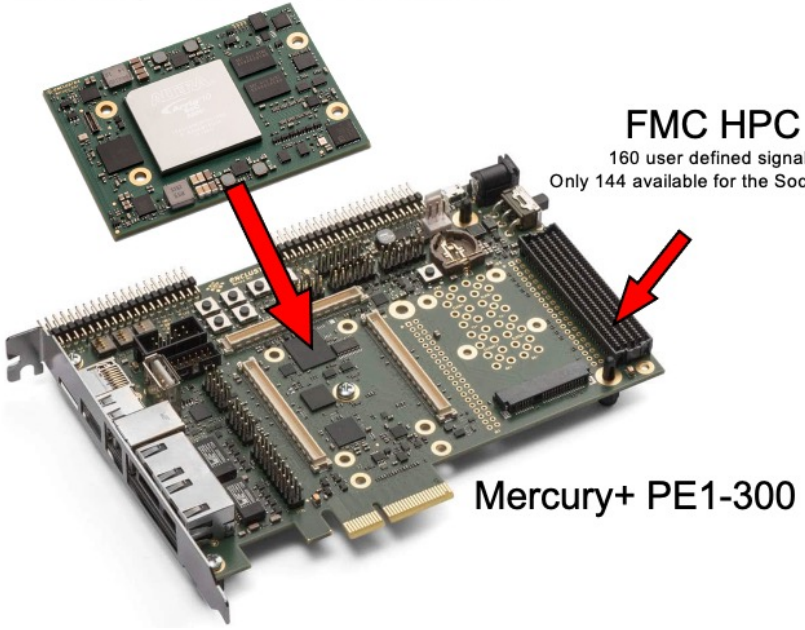


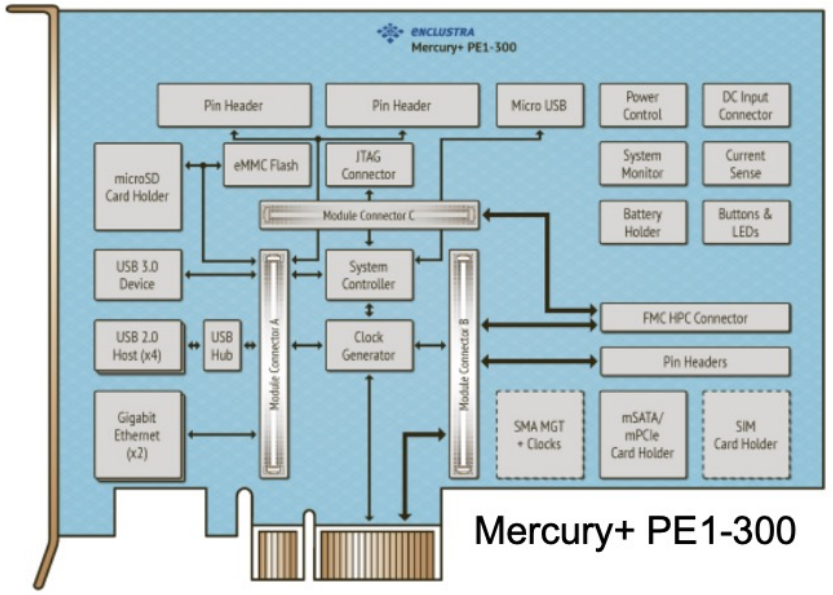
Mercury+ AA1 SX270

Mercury+ AA1 Features:

- Intel Arria® 10 ARM® Processor-based SoC FPGA
  - ARM® dual-core Cortex™-A9
  - (32 bit, up to 1.5 GHz)
  - Intel Arria 10 20 nm FPGA fabric
- Small form factor (74 × 54 mm)
- 286 user I/Os
  - 18 ARM peripheral I/Os (SPI, SDIO, I2C, UART)
  - 212 FPGA I/Os (single-ended or differential)
    - 168 FPGA I/Os
    - 44 FPGA I/Os shared with USB 3.0
    - 56 MGT signals (clock and data)
- Up to 4 GByte DDR4 ECC SDRAM
- 16 GByte eMMC flash
- 64 MByte quad SPI flash
- PCIe® Gen3 x8
- 12 × 10.3125/12.5 Gbit/sec MGTs
- Gigabit Ethernet
- USB 3.0 device controller
- USB 2.0 host/device
- 5 to 15 V supply voltage

Mercury+ SA2 or AA1 SX270





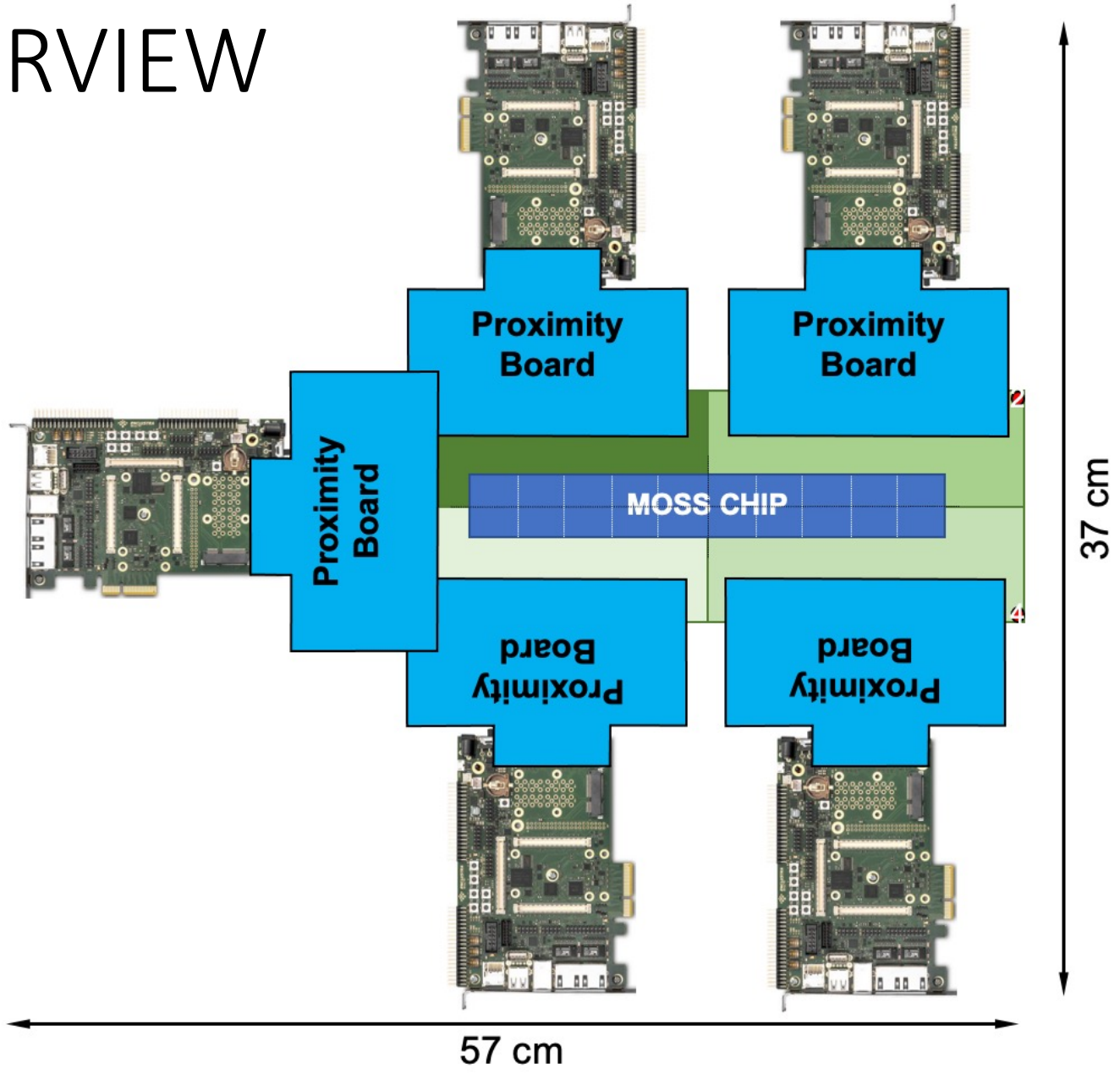
Mercury+ PE1-300

Mercury+ PE1-300 Features:

- Hirose FX10 connectors for Mercury/Mercury+ modules
- Low-jitter clock generator
- System monitor
- System controller
- Power control
- Current sense
- microSD card holder
- eMMC Managed NAND flash
- PCIe Gen2 ×4 interface
- USB 3.0 device interface
- 4 × USB 2.0 host interface
- Micro USB 2.0 device (UART, SPI, I2C, JTAG) interface
- 2 × RJ45 Gigabit Ethernet
- mPCIe/mSATA card holder (USB only)
- SIM card holder (optional)
- MGT and SMAclock in/out (optional)
- 1 × FMC HPC connector (PE1-300)
- 2 × 40-pin Anios pin header
- 3 × 12-pin Pmod™ pin header
- 5 to 12V DC supply voltage
- USB bus power (with restrictions)

TEST SET-UP OVERVIEW

Milestone 3 ITS3: verifica funzionalità large area non-bent sensor stitched



WP4+5: BENDING INTERCONNECTIONS AND MECHANICS

WP4: bending & interconnections

1st paper doi:10.1016/j.nima.2021.166280

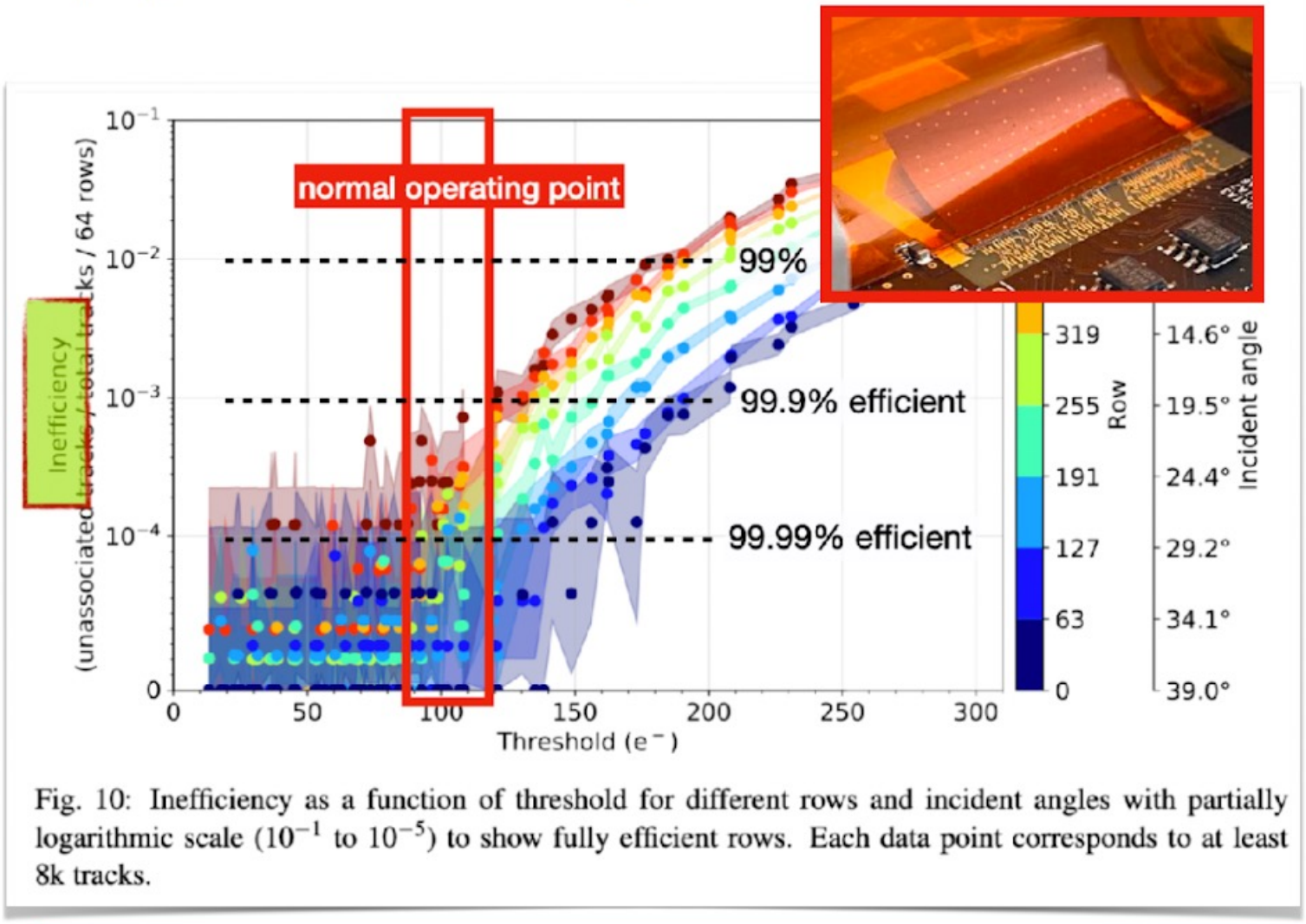


Fig. 10: Inefficiency as a function of threshold for different rows and incident angles with partially logarithmic scale (10^{-1} to 10^{-5}) to show fully efficient rows. Each data point corresponds to at least 8k tracks.

Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment

Available online 10 January 2022, 166280

In Press, Journal Pre-proof

First demonstration of in-beam performance of bent Monolithic Active Pixel Sensors

ALICE ITS project [1]

Show more

Share Cite

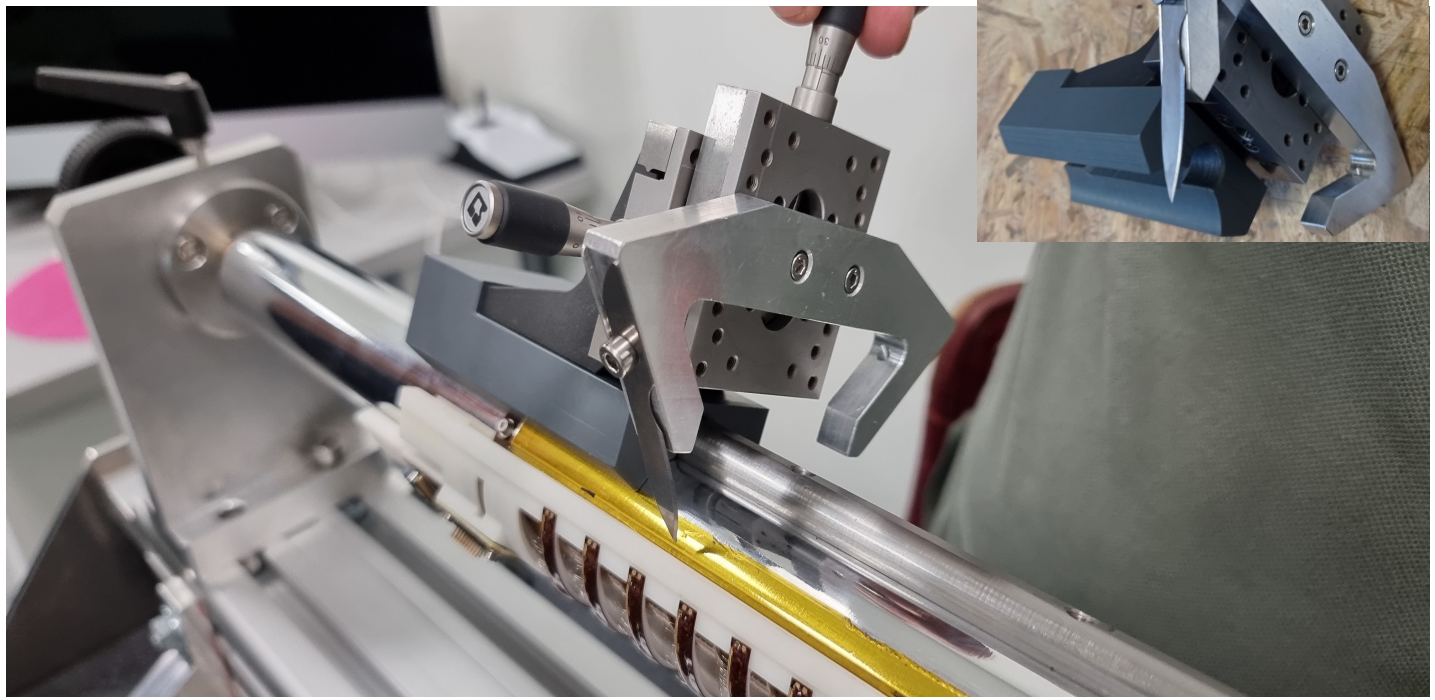
https://doi.org/10.1016/j.nima.2021.166280

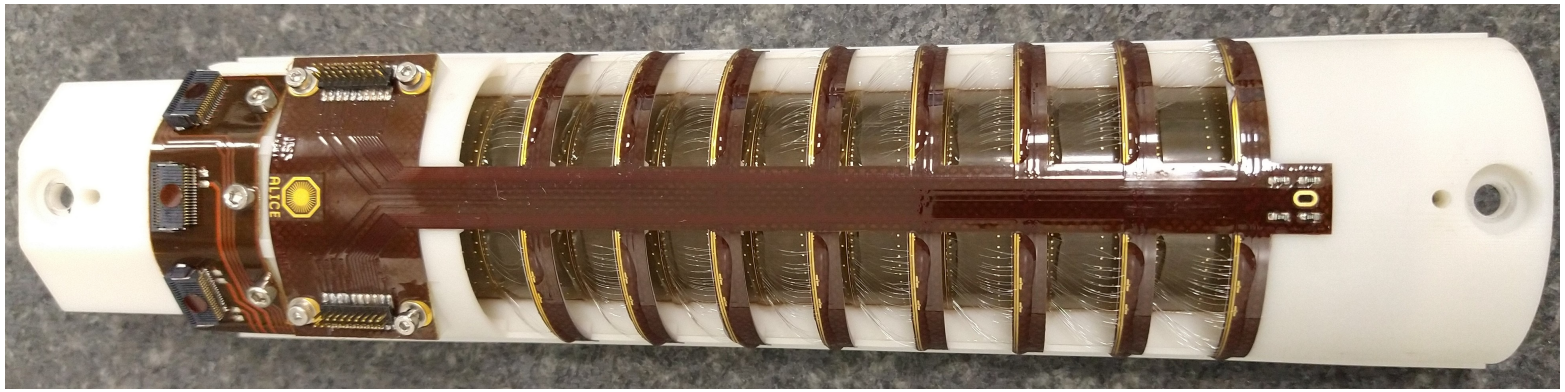
Get rights and content

Clearly proving that bent MAPS are working!

WP4: bending & interconnections

- Resp: D. Colella – G. Contin
- Goal:
  1. tecniche di bending di sensori di grande area
  2. tecniche di interconnessione flex-bent silicon (wire bond – spTAB bond)

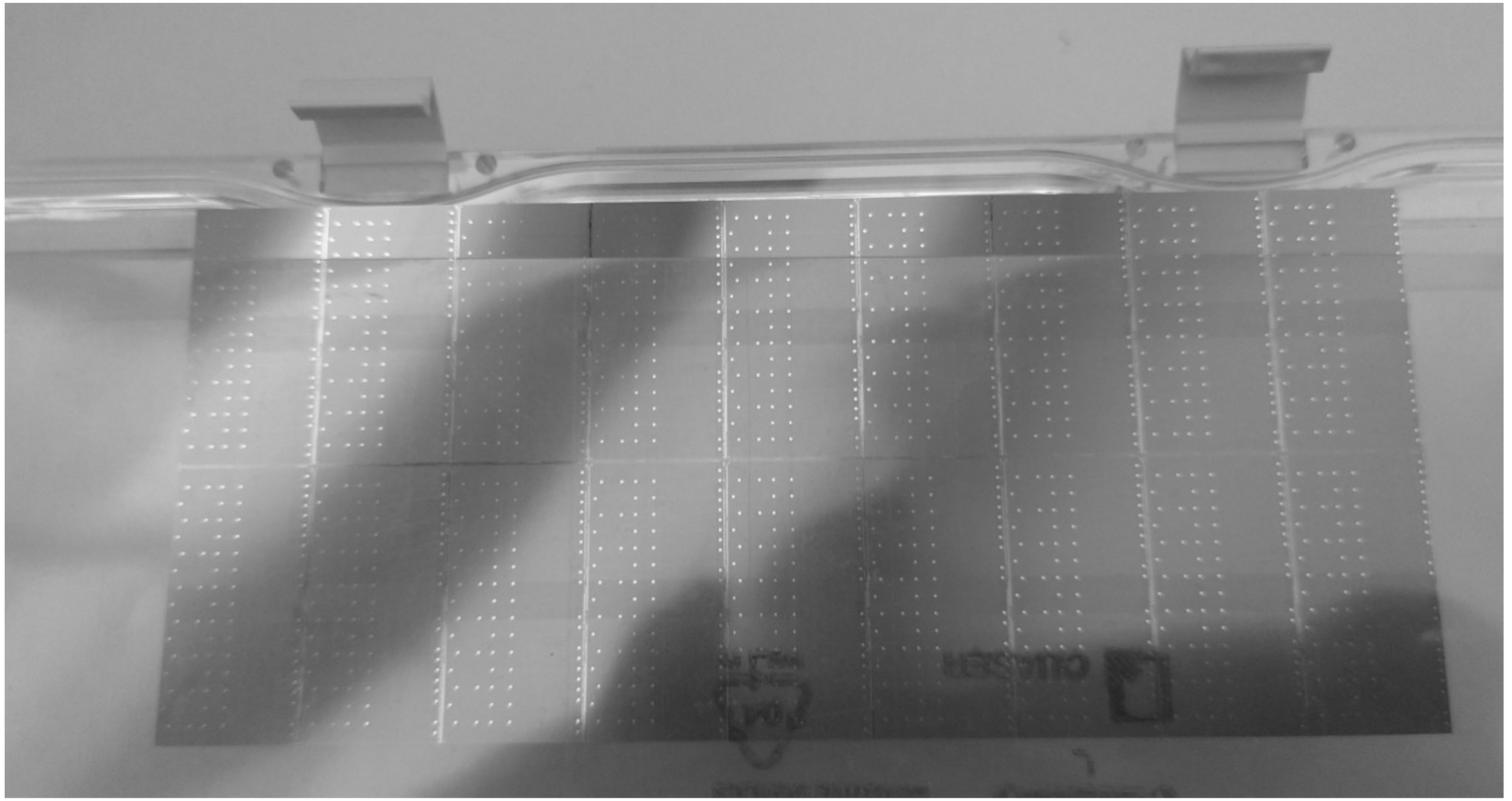




- Stato dell'arte:
- jig per bending di superAlpide pronto, risultati attesi per Settembre (beam test)
- primi prototipi di FPC bondati su superALPIDE mock-up

WP4: bending & interconnections

- Super ALPIDE chip: 9 ALPIDE chips to simulate 1 large area sensor



Milestone 2 ITS3: verifica funzionalità large area bent sensor non-stitched

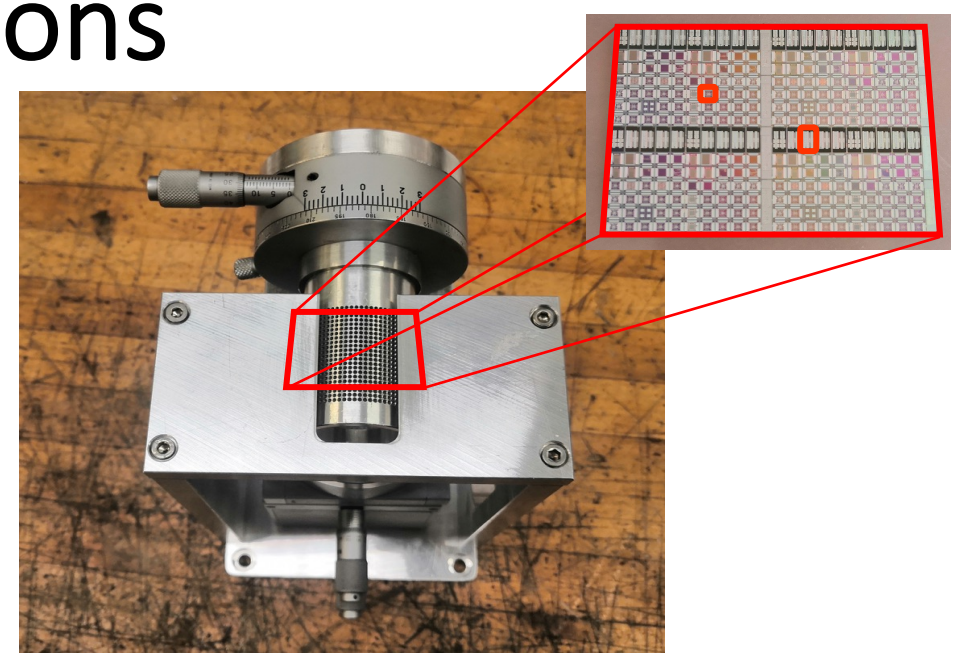
- Stato dell'arte:
- jig per bending di superAlpide pronto, risultati attesi per Settembre (beam test)
- primi prototipi di FPC bondati su superALPIDE mock-up

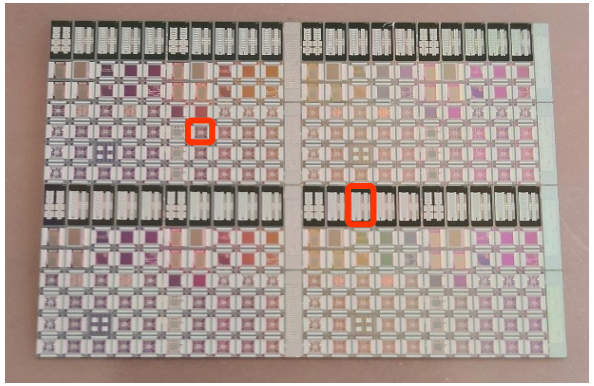
WP4: bending & interconnections

- Next steps:
  1. bending di strutture APTS
  2. verifica della funzionalità di bent chip in tecnologia 65 nm

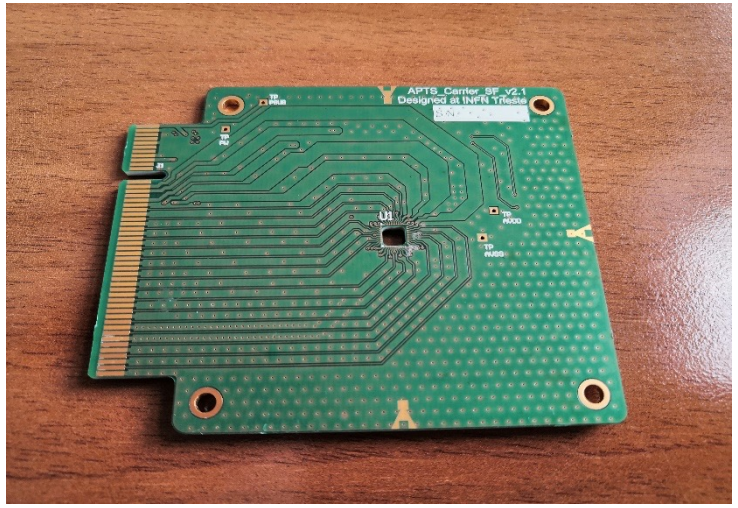
Attualmente l'attività si concentra sullo sviluppo di jig per il bending e di PCB per il test delle strutture bent

- Wire bonding being tested on dummy silicon
- New jig with chip-cylinder alignment reference and micro positioning stages ready
- Carrier jig being adapted to telescope setup

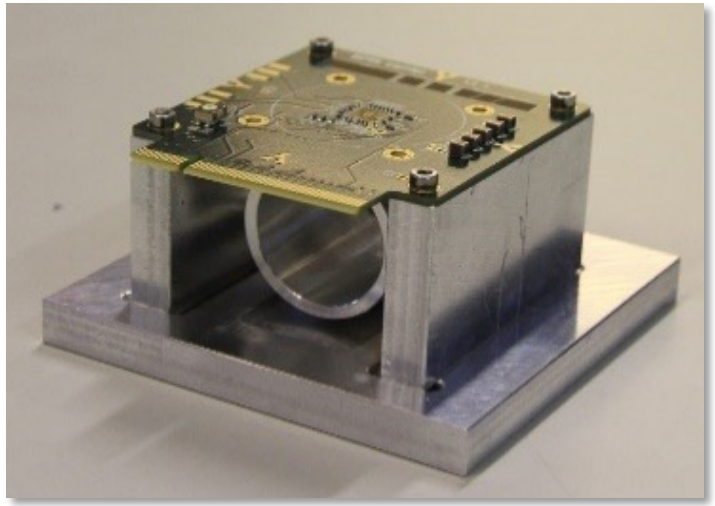




4x MLR1 reticles = 3.2x2.4 cm^2 chip



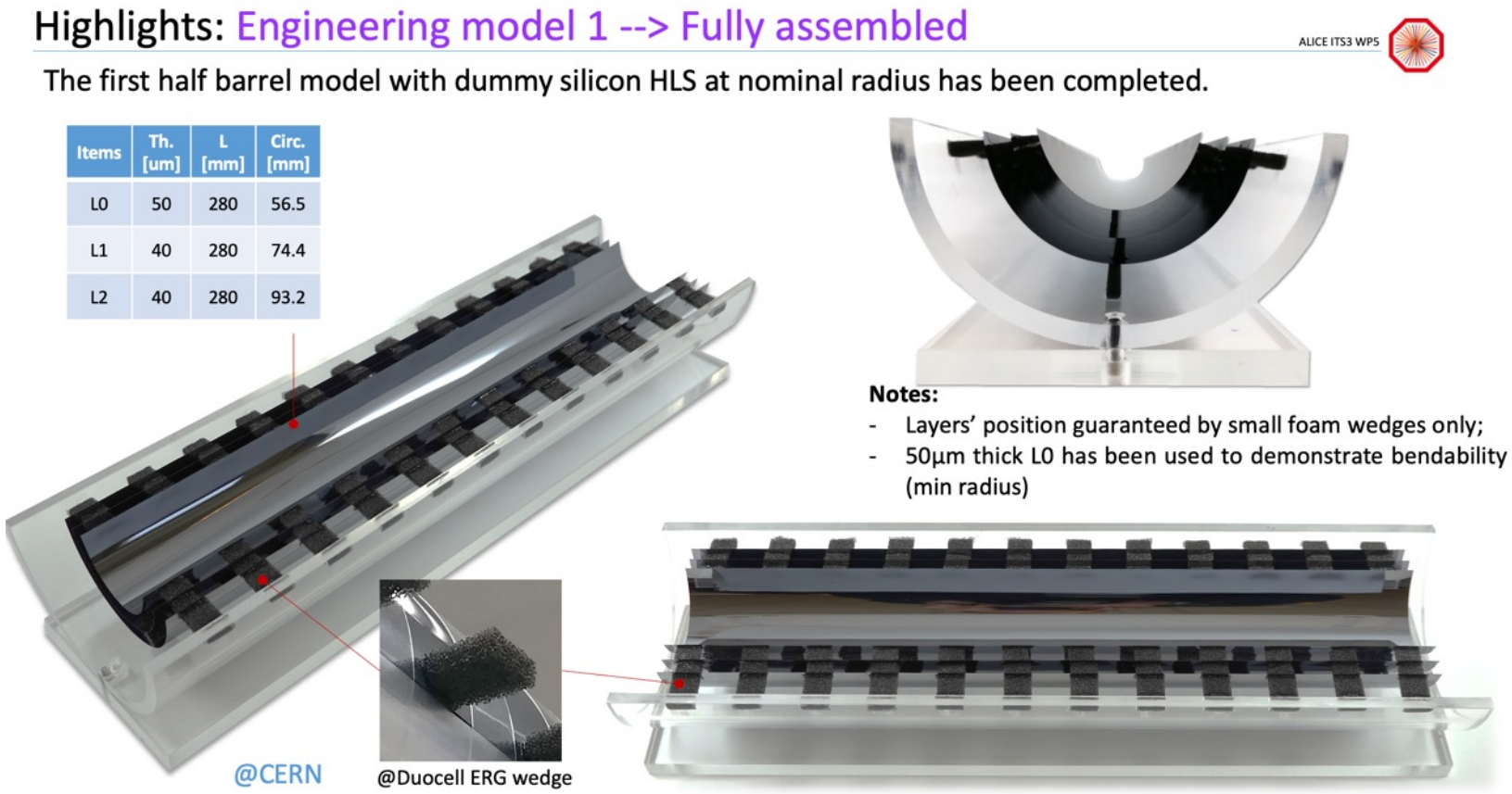
APTS_SF modified board



ITS3-WP5: mechanics

convener: C. Gargiulo

- attività principali:
  - studi strutturali dei sensori curvati
  - scelta materiali per supporti in carbon foam
  - studi su cooling della periferia del sensore
  - progettazione struttura e supporti
- contributo INFN:
  - **Bari**



ITS3 test structure characterization campaign

Responsabilità INFN: chip design, test system e organizzazione campagna di caratterizzazione, bending & interconnections

2021:

- progettazione e messa a punto test system per small pixel matrices
  - DAQ board + Proximity board
  - Carrier board APTS OPAMP
  - Carrier board APTS Source Follower

produced and tested 2 versions so far

- Test di caratterizzazione APTS in 5 sedi INFN, collaborazione per CE65 (IPHC)
- Partecipazione a beam tests come da programma 2020

2022:

- Sottomissione ER1 (contributo INFN 165k€)
- progettazione e messa a punto test system per MOSS
  - DAQ board (CA) + Proximity board (CERN)
- Partecipazione a beam tests (circa 8 settimane)
- caratterizzazione di massa di TS MLR1

ITS3 test structure characterization campaign

Responsabilità INFN: chip design, test system e organizzazione campagna di caratterizzazione, bending & interconnections

2023:

- WP2: Design e sottomissione ER2 (contributo INFN previsto 250k€)
- WP3: Test di strutture bent + large area (sviluppo di nuovo test system per MOSS chip); caratterizzazione di strutture irraggiate
- WP4: continuazione attività bending e bonding su strutture bent di piccola e grande area
- WP5: studio di materiali per supporti e cooling

(contributo INFN previsto 150k€)

ITS3: Conclusions

- Le responsabilità INFN in ITS3 sono consolidate per ruoli di coordinamento di Work Package (WP1-3) e di attività specifiche (chip design – test system design and production – chip characterization)
- La sottomissione di ER1 è prevista per Agosto 2022
- Il sistema di test MLR1 è completato e in fase di distribuzione per il test di massa delle TS MLR1
- Il sistema di test per ER1 è in fase di progetto

- Eccellenti risultati ottenuti nella fase preliminare di caratterizzazione dei chip APTS e DPTS (contributo sostanziale INFN a test di laboratorio e su fascio)
- Progressi continui per bending e bonding: next step il bending di sensori di grande area (superALPIDE) e di TS di piccola area (MLR1)

OVERVIEW RICHIESTE ITS3 2021-2025

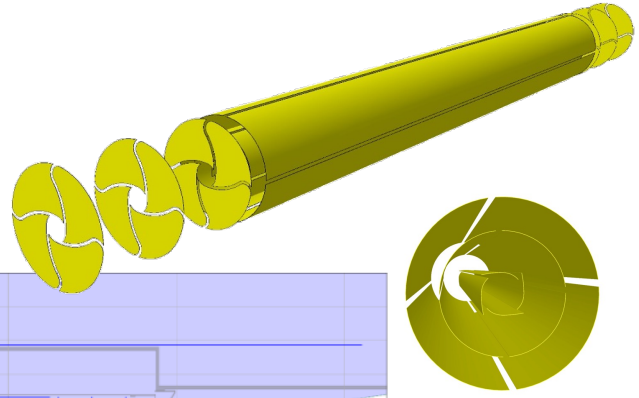
tipo attività	2021 (k€)	2022 (k€)	2023 (k€)	2024 (k€)	2025 (k€)	2026 (*)?	totale richiesta INFN (k€)	totale ITS3 (k€)
R&D	200	300	150 WP3=100 WP4+5=50				700 (**)	2500
Costruzione			ER2: 250	400	400	100	1100	3500
totale	200	300	400	400	400	100	1800	6000
viaggi			50					

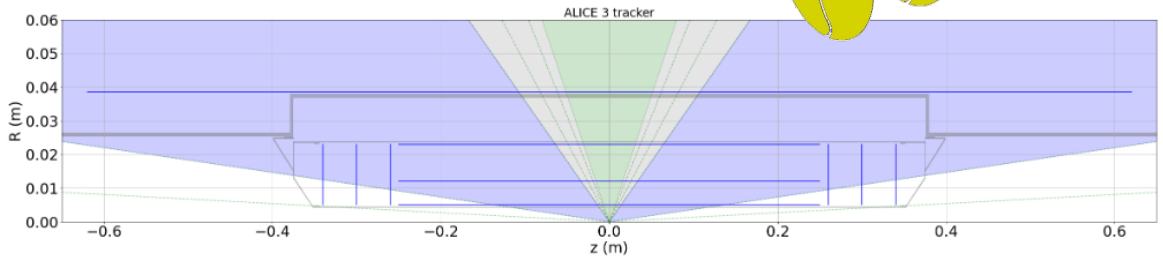
ALICE3 tracker

ALICE 3 Tracker layout

Vertex detector

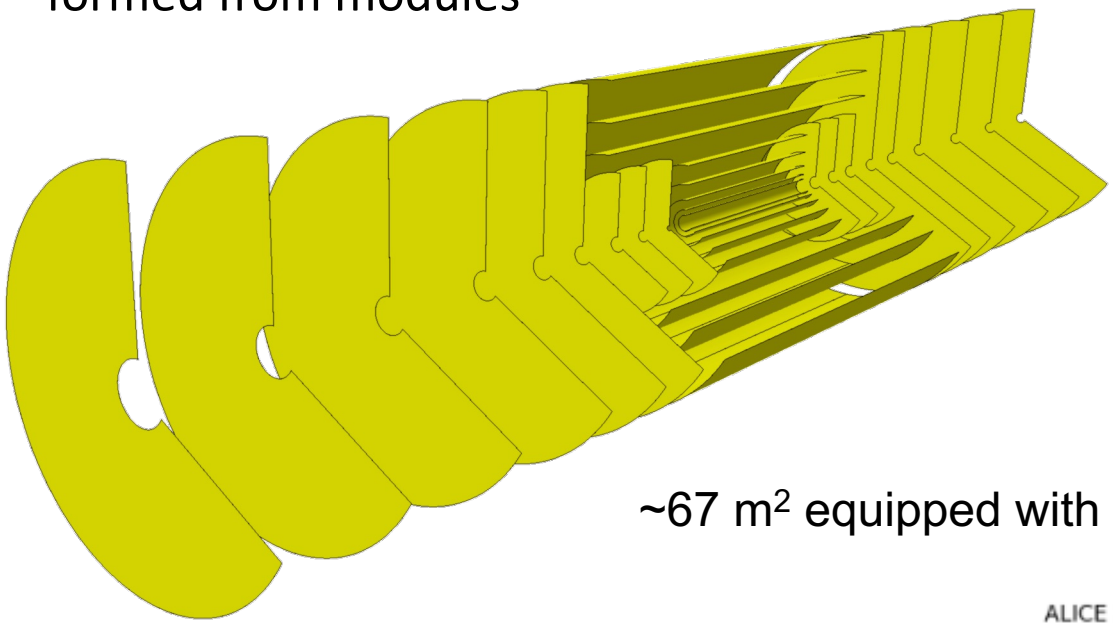
Retractable bent silicon inside the beampipe





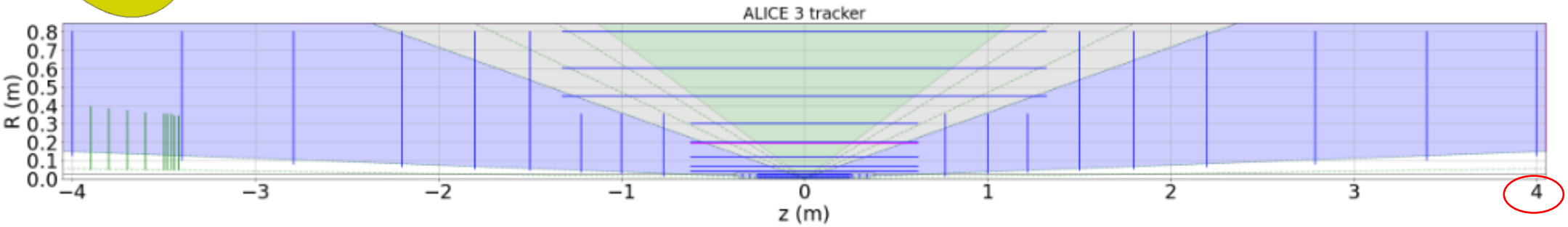
Outer tracker

Traditional disks/staves formed from modules



~67 m^2 equipped with MAPS

Layer	Material thickness ($\%X_0$)	Intrinsic resolution (μm)	Barrel layers Length ($\pm z$) (cm)	Barrel layers Radius (r) (cm)	Forward discs Position ($\lvert z \rvert$) (cm)	Forward discs R_{in} (cm)	Forward discs R_{out} (cm)
0	0.1	2.5	50	0.50	26	0.005	3
1	0.1	2.5	50	1.20	30	0.005	3
2	0.1	2.5	50	2.50	34	0.005	3
3	1	10	124	3.75	77	0.05	35
4	1	10	124	7	100	0.05	35
5	1	10	124	12	122	0.05	35
6	1	10	124	20	150	0.05	80
7	1	10	124	30	180	0.05	80
8	1	10	264	45	220	0.05	80
9	1	10	264	60	279	0.05	80
10	1	10	264	80	340	0.05	80
11	1				400	0.05	80



Requirements for the ALICE 3 Tracker

Different requirements for the two tracker systems:

- **Vertex** detector: sustain high rate and high radiation load
- **Outer tracker**: minimize power, equip a very large area (> 60m^2)

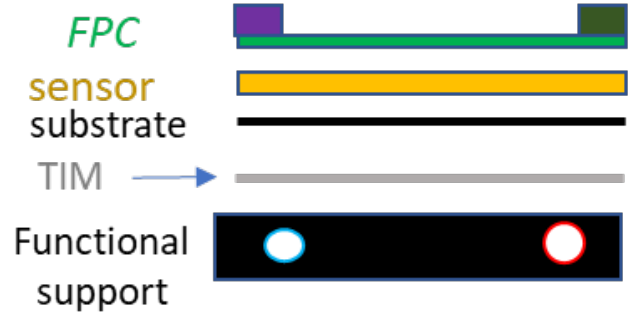
ITS3 sensor technology as a baseline sensor for ALICE 3

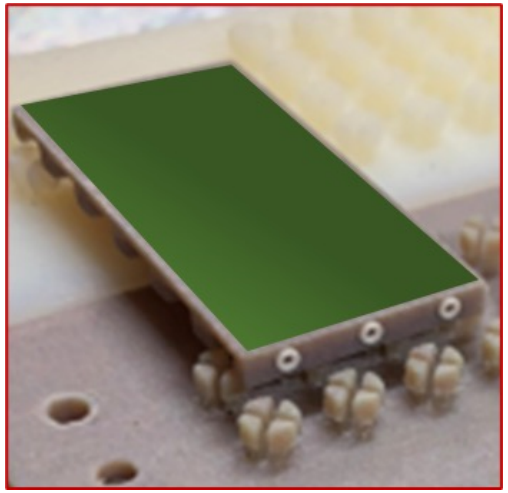
- **Synergies** and **existing expertise** within INFN groups
- Ongoing ITS **studies easily extended to the ALICE 3** requirements

Parameter	Vertex detector	Outer tracker
Spatial resolution	2.5 μm	10 μm
Time resolution	100 ns (RMS)	100 ns (RMS)
Hit rate capability	35 x 10^6 / (s cm^2)	5 x 10^3 / (s cm^2)
Power consumption	70 mW / cm^2	20 mW / cm^2
Radiation hardness	1.5 10^{15} 1 MeV n_{eq} / cm^2 / year	

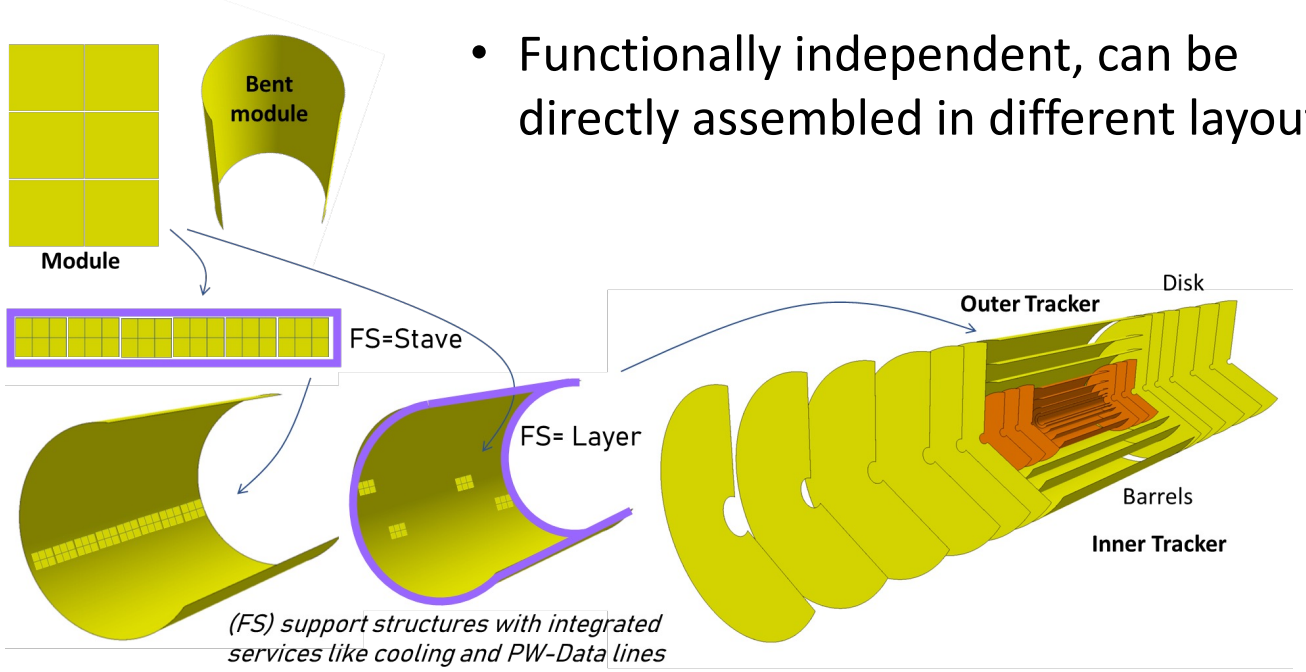
Challenges and R&D topics

- **Sensor** development and validation for ALICE 3 requirements
- **Mechanics and services** for Vertex in secondary vacuum
- Outer Tracker concept: **modularized and industrialized** module
  - Include sensor, signal and power distribution, interconnection bus, supports
  - Easy to replicate and to produce in an industrial environment
  - Supports provide alignment, stability, connectivity, cooling



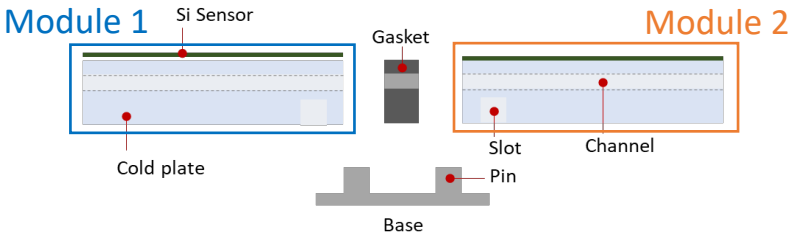


- Functionally independent, can be directly assembled in different layout



(FS) support structures with integrated services like cooling and PW-Data lines

Lego design idea



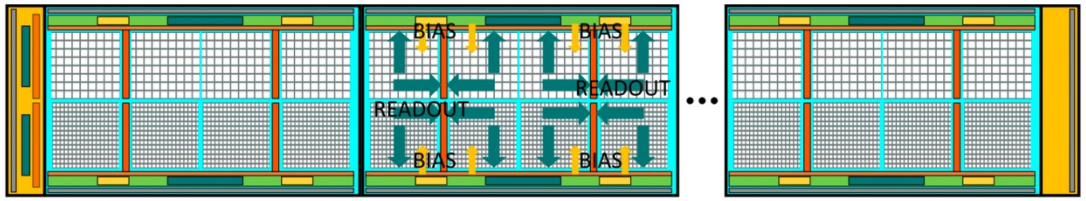
BACKUP SLIDES

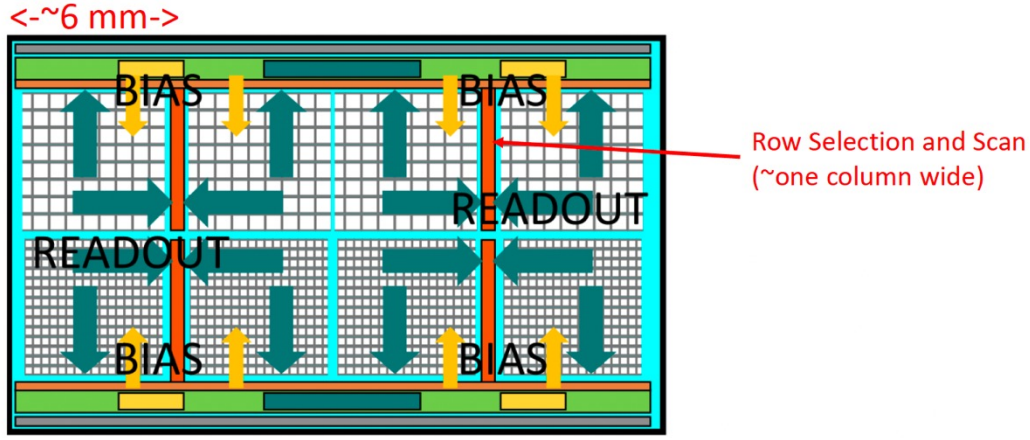
MOSS: Monolithic stitched sensor

First large are sensor designed for high energy particles detection → main goal:

- test basic features of designing with stitching and aspects like yield

DESIGN DI INTERESSE COMUNE A:
ALICE
NA60+
EIC





Basic subsensor unit 25 m long, replicated 10 times through stitching, for an o length of about 25 cm

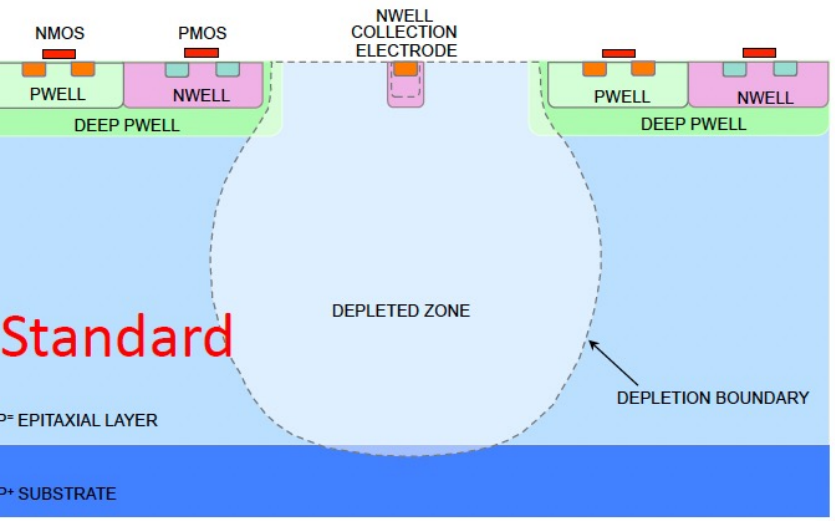
Readout architecture and powering:

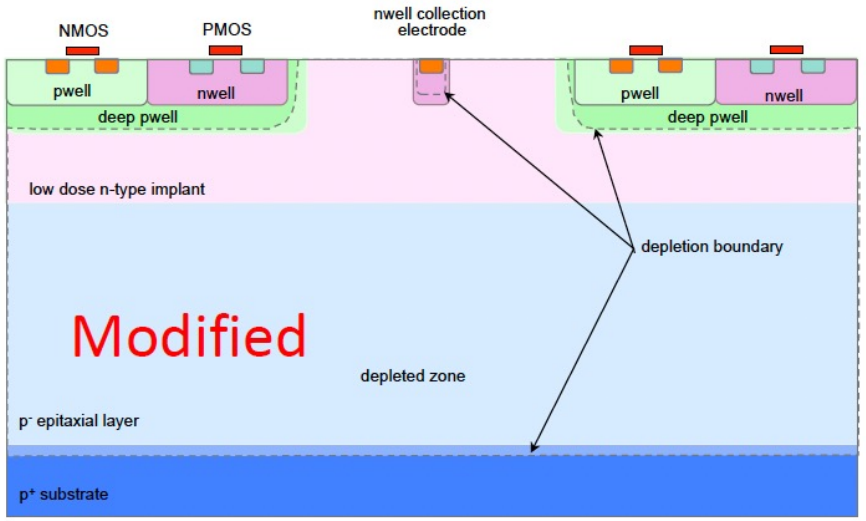
- readout performed locally independently for each subsensor and also from left end as foreseen for ALICE ITS3 (simple parallel ports, no high speed serial links)
- separate powering for each subsensor →minimize shorts affecting the others

Process modifications

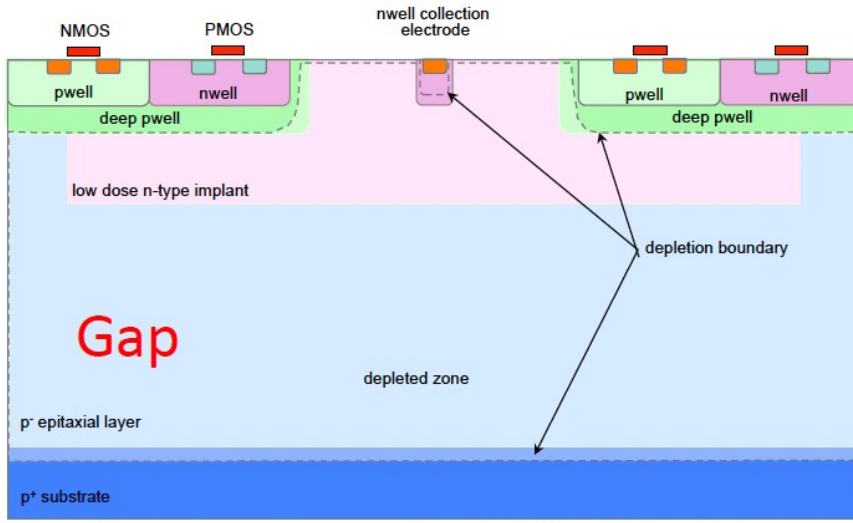
Similar optimization as in 180nm

Implant modifications needed even more in 65 nm for good charge collection





https://doi.org/10.1016/j.nima.2017.07.046 (180nm)



https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013 (180nm)

Charge collection speed

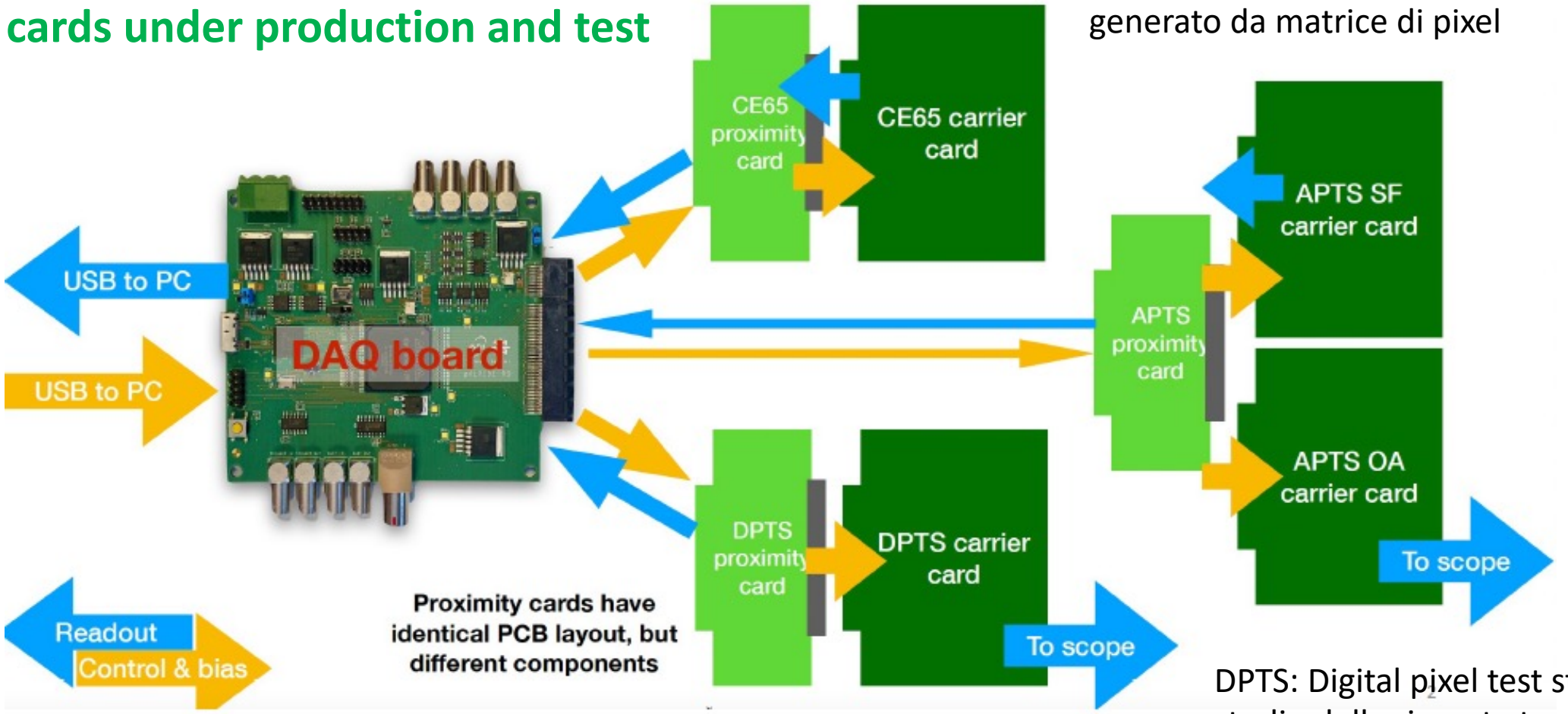
Charge sharing

MLR1 Test system concept

System fully designed

Presently **cards under production and test**

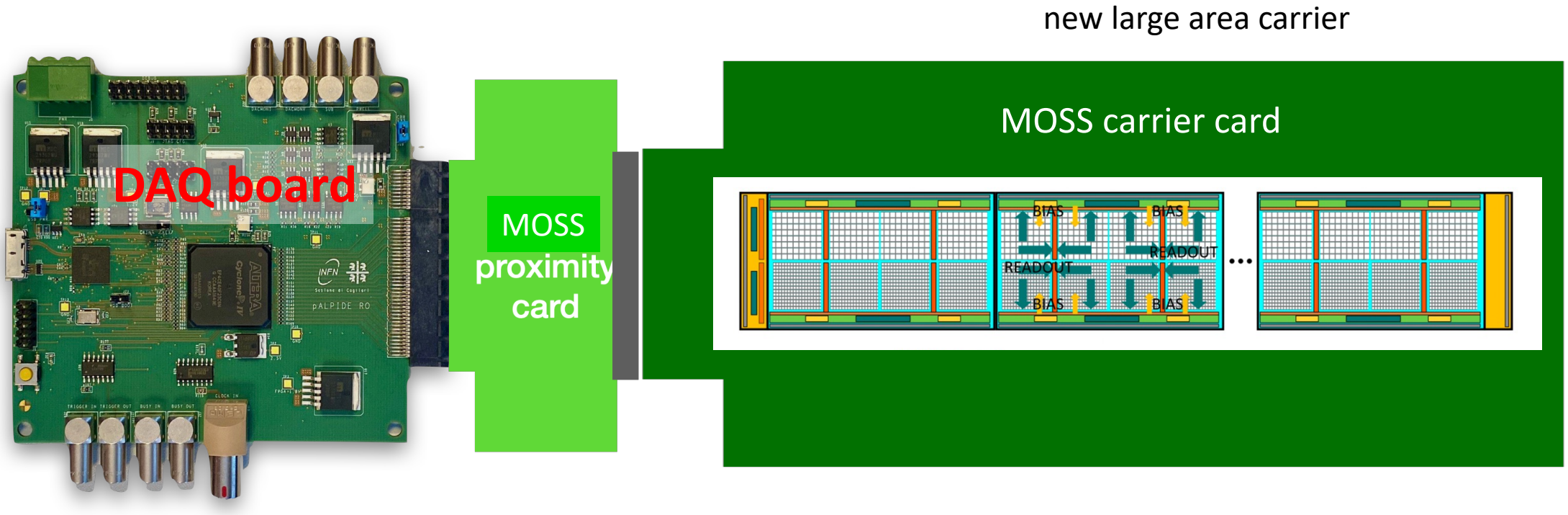
APTS: Analog pixel test structure
studio della forma del segnale generato da matrice di pixel



DPTS: Digital pixel test structure
studio della risposta temporale de pixel

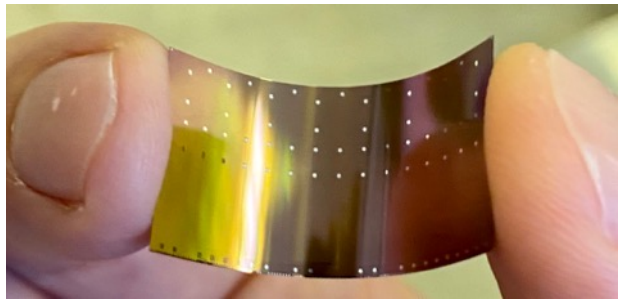
MOSS Test system concept

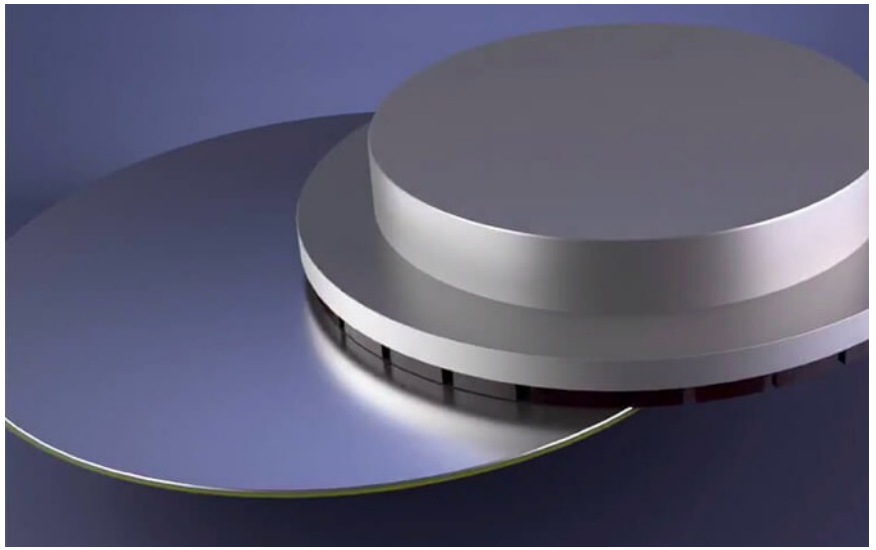
Extension of concept developed for MLR1

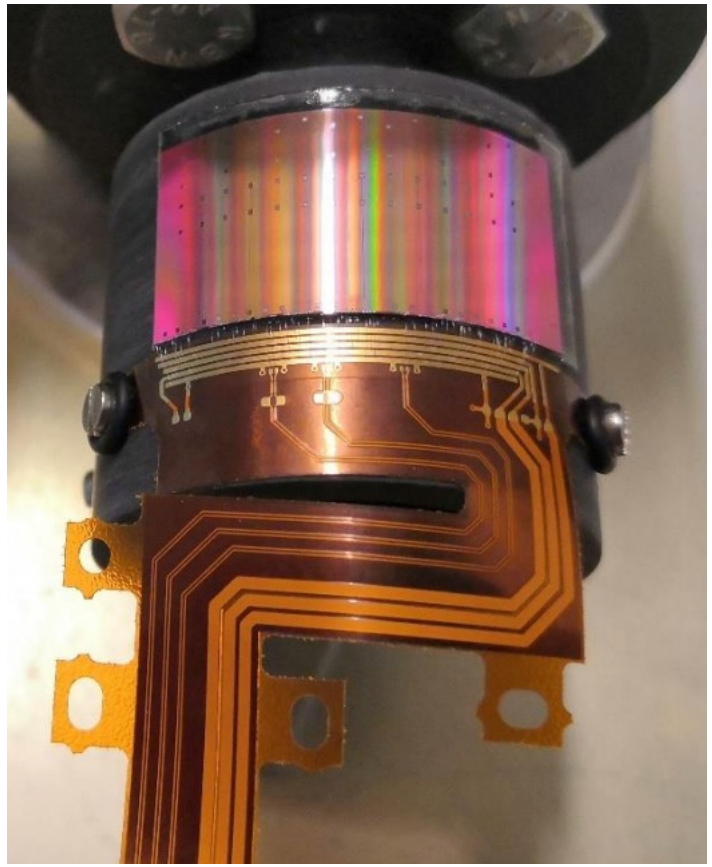


ITS3 - WP4: sensor thinning, bending and interconnections

convener: **G. Contin** – M. Mager





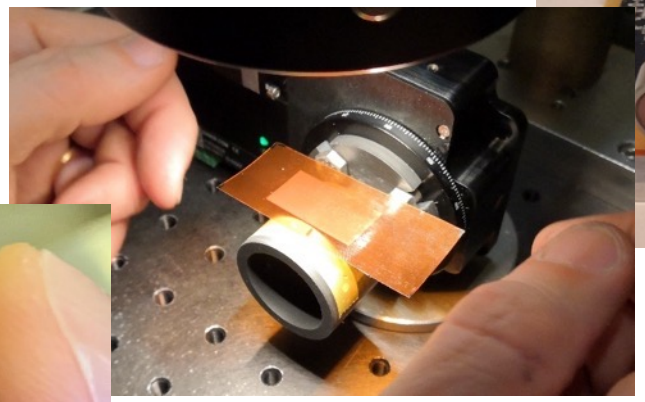


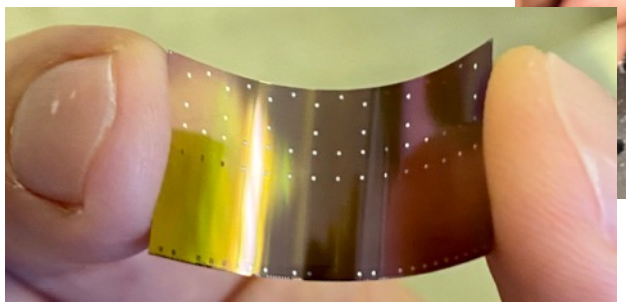
interesse da diverse sedi INFN:

- Bari/Bologna: wire bonding
- Trieste: thinning, bending, wire bonding
- Torino: spTAB bonding

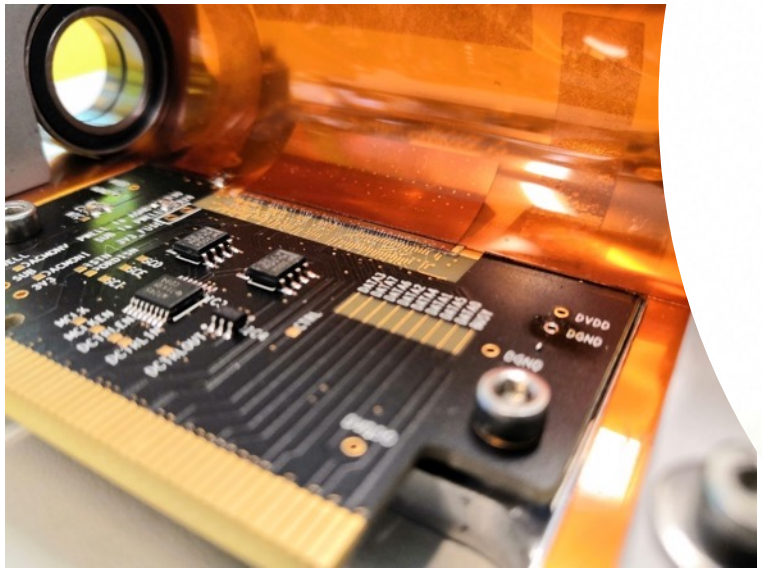
Sensor bending

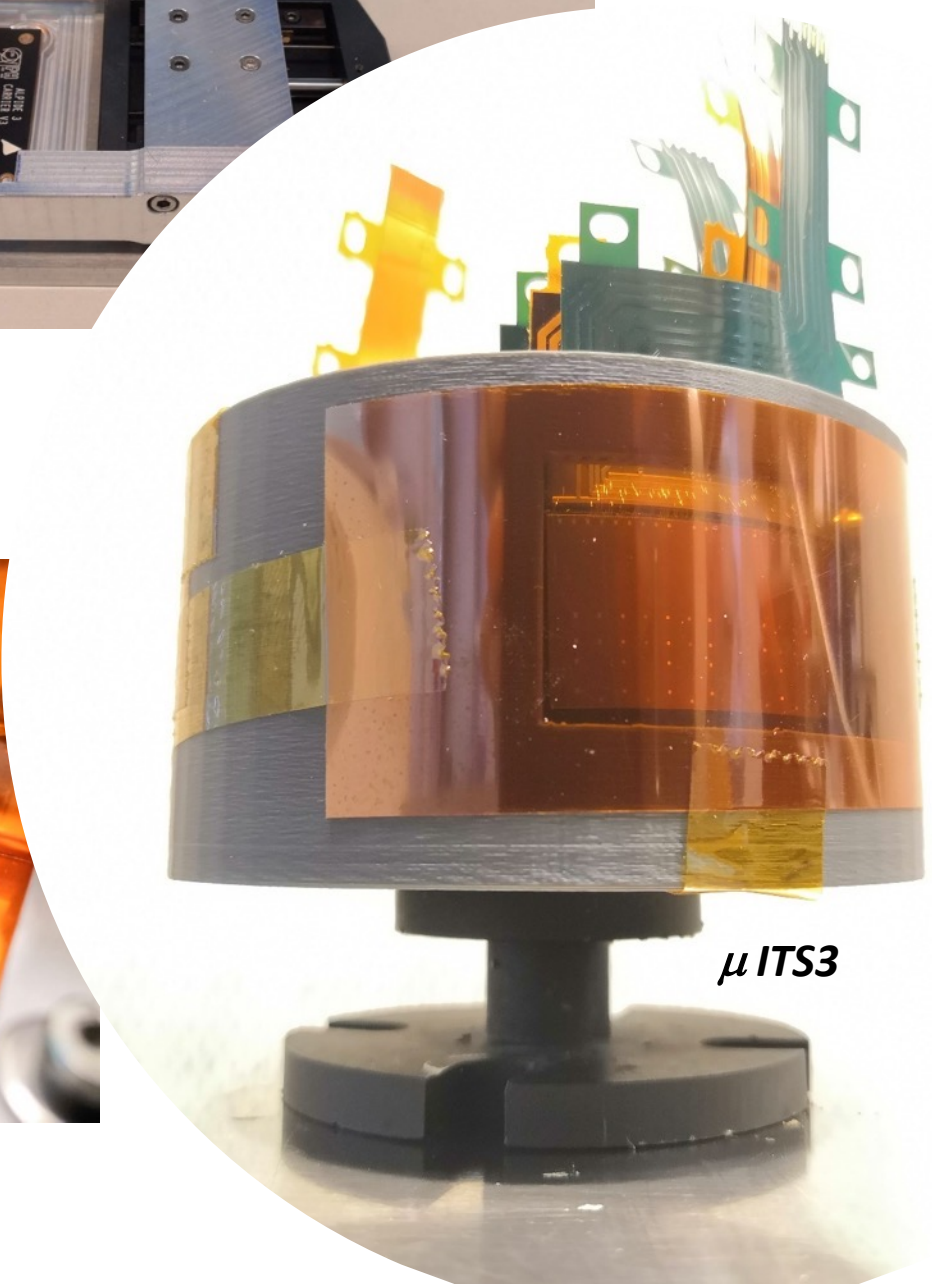
Manual bending





Controlled bending

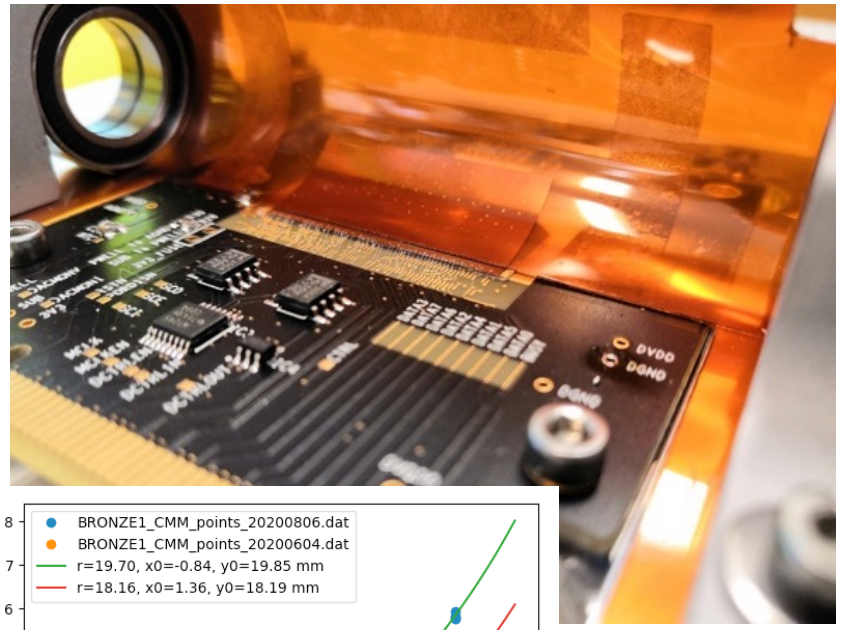


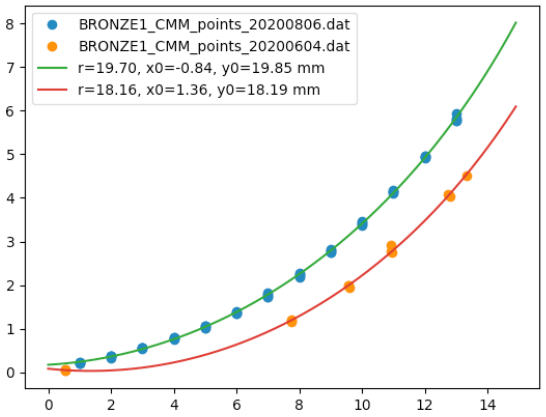


μ ITS3

- Measured curvature radius:
  - DUT1: ~ 16mm
  - DUT2: ~ 18mm
- **Test beam performed at Desy, no possibility to participate due to COVID-19 (article ready for publication)**

Preparazione DUTs e telescopi per testbeams





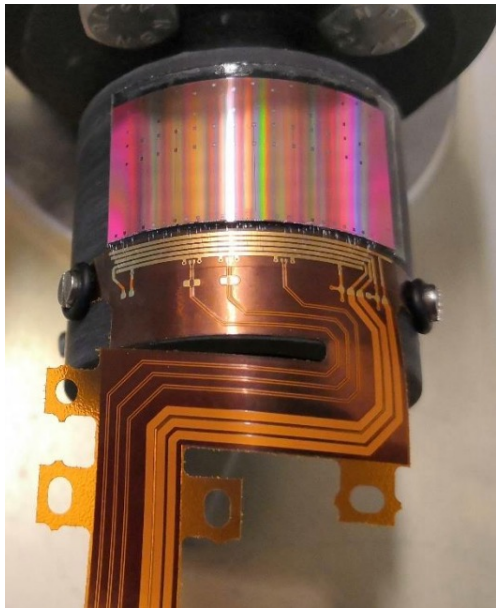
Monitoraggio della curvatura

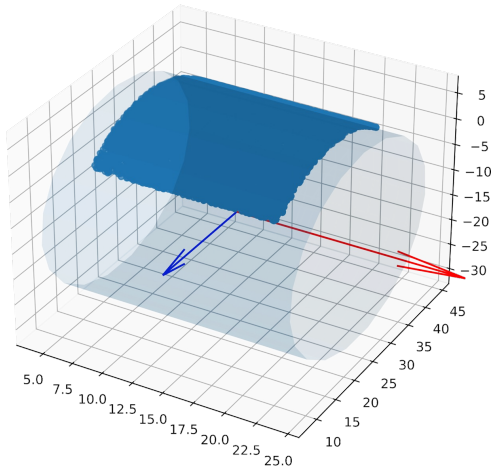
Preparazione DUTs per diversi Testbeam 2020-2021 avvenuta principalmente a Trieste e al CERN

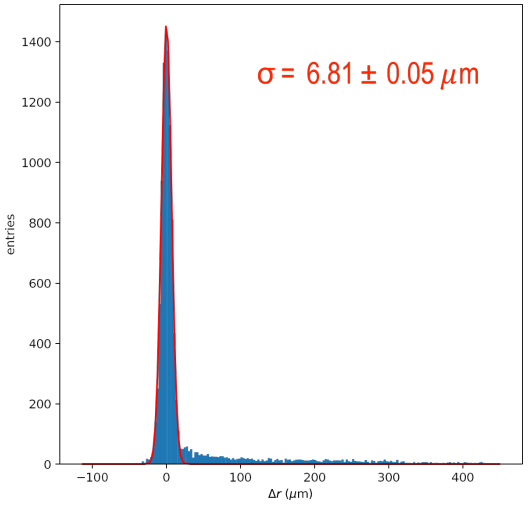
R&D su:

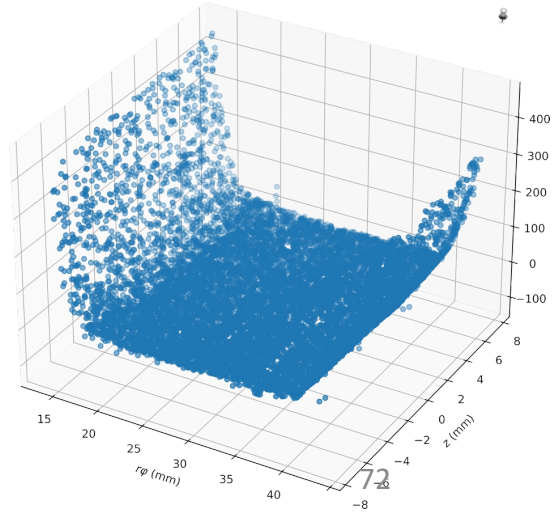
- Meccaniche e procedure per curvatura
- Wire-bonding su superfici curve
- Misura di precisione della curvatura (CMM)
- Primi test elettrici in laboratorio

→ Risultati pubblicati in [arXiv:2105.13000]

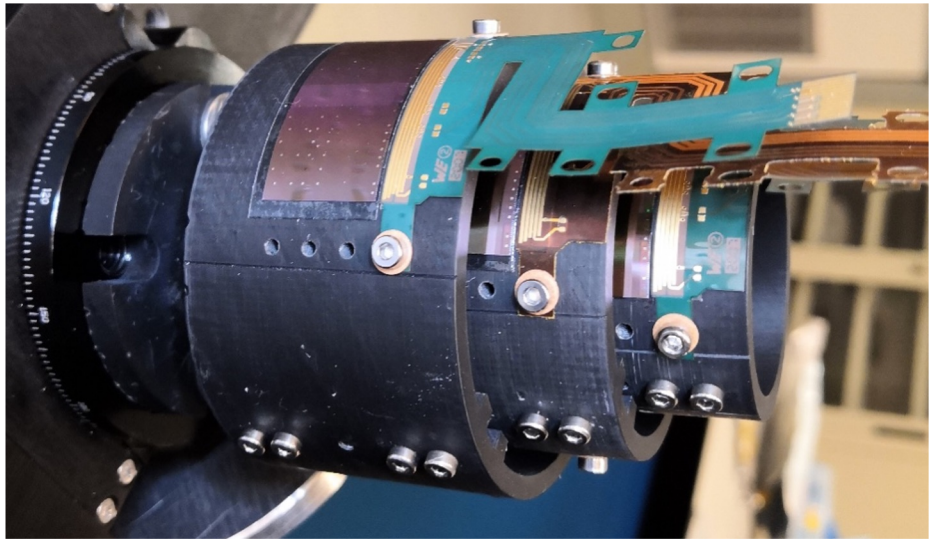








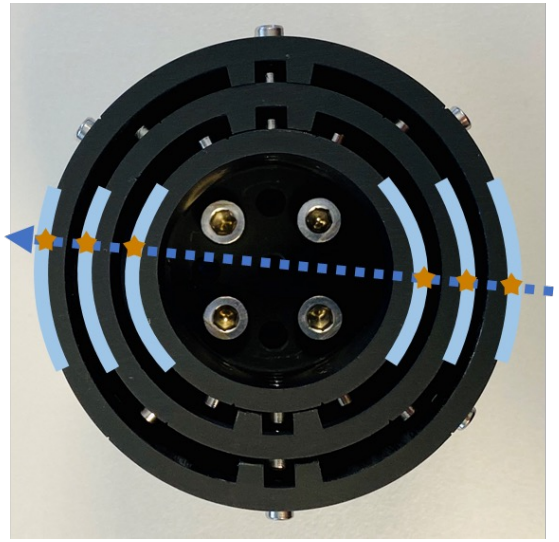
Preparazione µITS3 e prossimi DUTs



µITS3

3 strati di ALPIDE curvati con raggio di curvatura nominale dell'ITS3

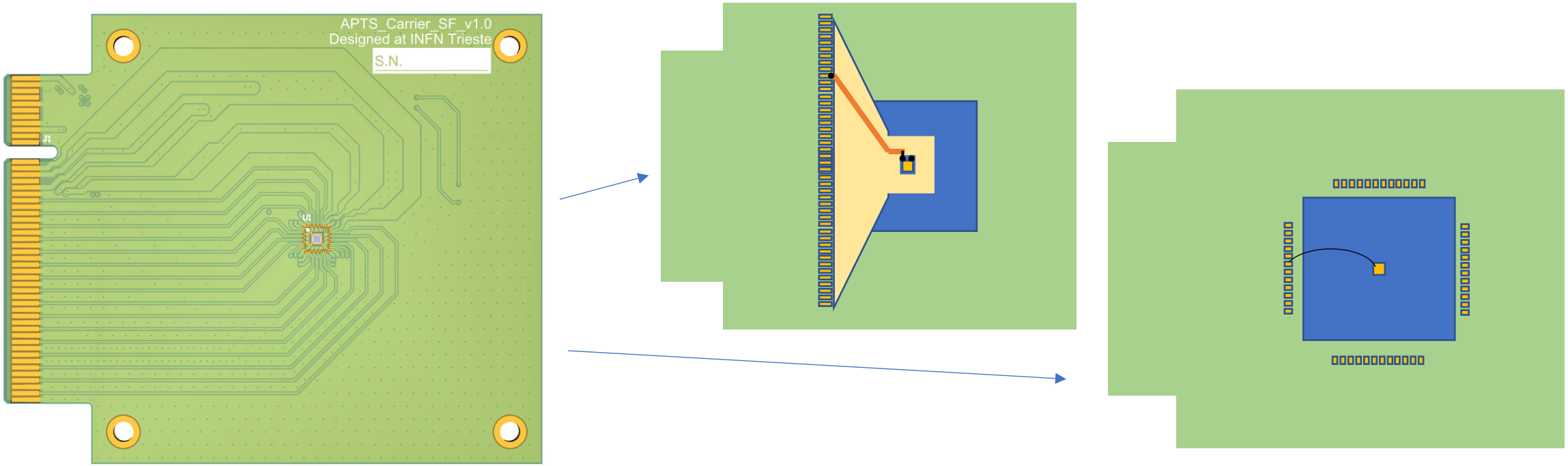
- Tracciamento con 6 punti registrati da strati di silicio curvo!



Piani 2022 per WP4 INFN (TS)

- Preparazione DUTs basati su ALPIDE e strutture di test MLR1
- Sviluppo meccaniche di curvatura di chip di media grandezza
- Sviluppo elettroniche di caratterizzazione segnali veloci per prossime sottomissioni
- Costruzione telescopi per caratterizzazione prestazioni DUTs

Piani per curvare strutture di test MLR1



Le carrier board sviluppate a Cagliari, Torino, Trieste saranno modificate per poter ospitare chip flessibili di area 3x3 cm^2 contenenti le strutture di test MLR1

Opzioni considerate: wire bonding e SpTAB bonding
Attualmente allo studio:

- Sviluppo FPC/chipcable e interconnessioni
- Miglior layout di tracce e piani di alimentazione
- Connessione meccanica e elettrica

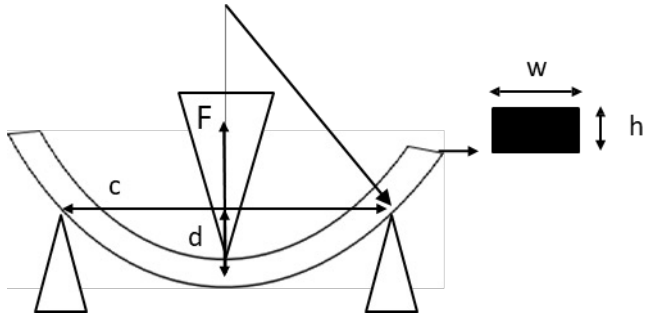
Thinning e caratterizzazione meccanica

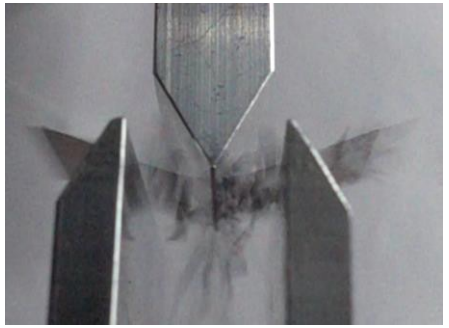
- Automated 3-p test setup

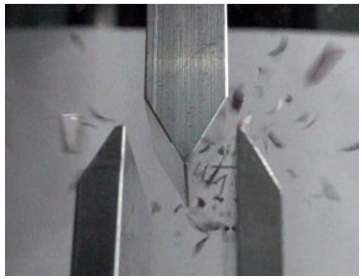
Planned measurements:

- Bending modulus
- Elastic – plastic region
- Breaking point
- Minimum radius

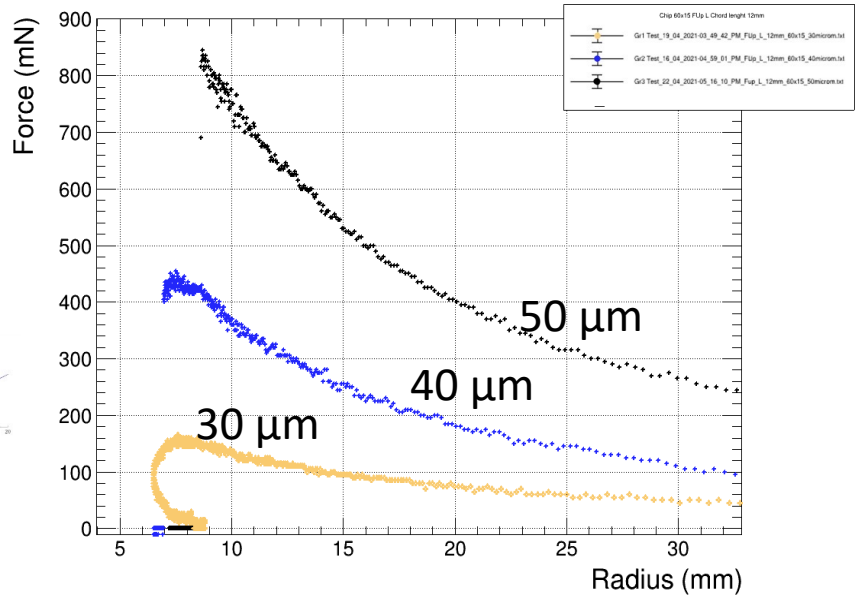
- **At 30-40-50 µm thickness!**





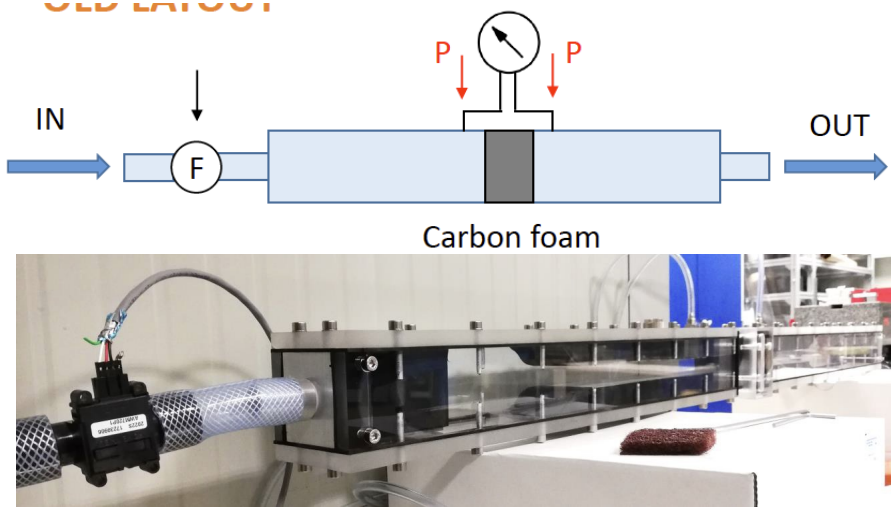


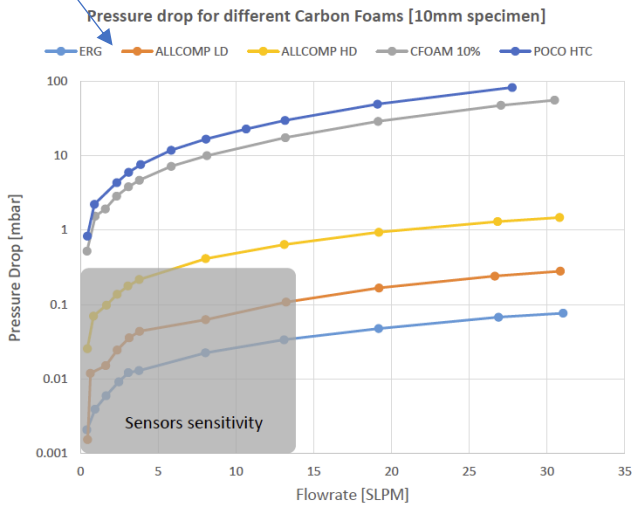
ALICE ITS3 Bending Test

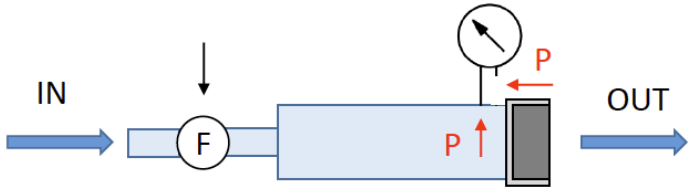


Caratterizzazione proprietà Carbon Foam (CF)

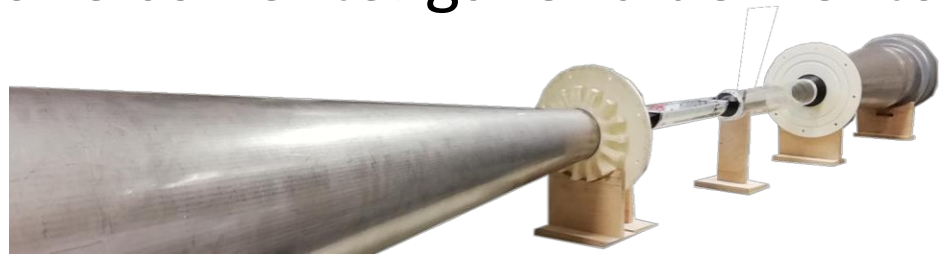
- Pressure drop test
  - Diversi layout provati nel 2021
  - Misure su diversi tipi di CF



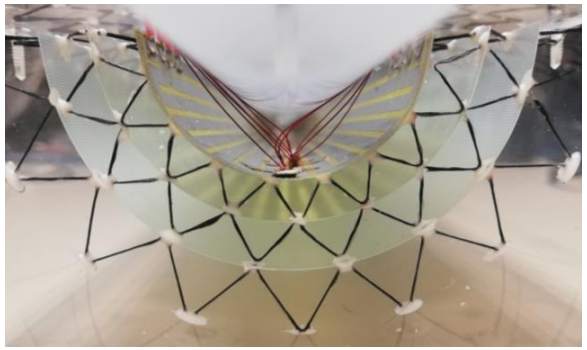




- Versione corrente: galleria del vento



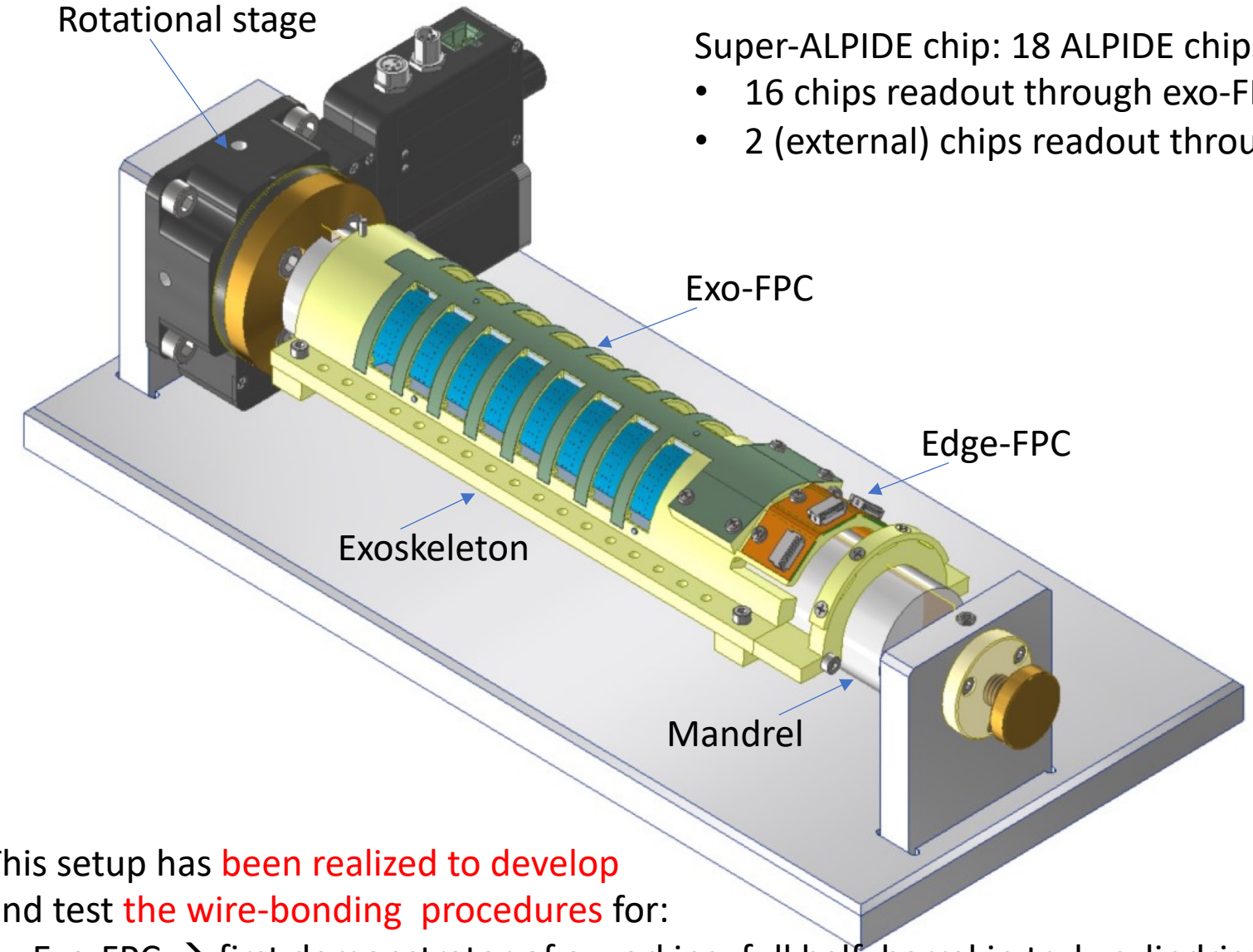
L0 equipped with 3 PT1000 temperature sensors



Studio del raffreddamento a valle del primo supporto (ring) in fibra di carbonio

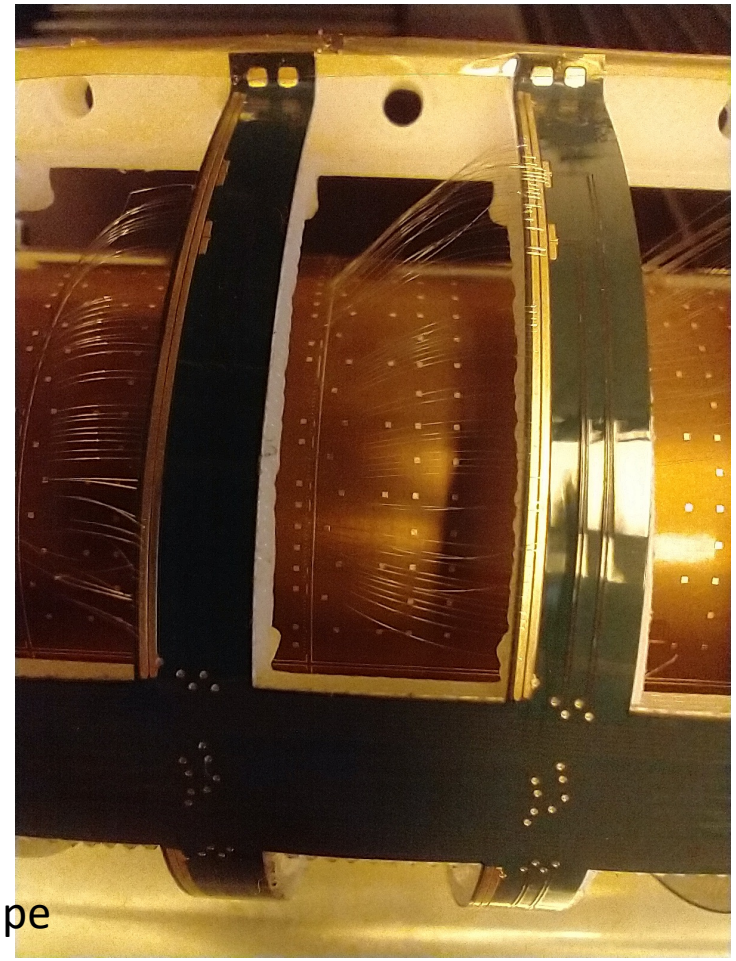
2022: attività di simulazione ed ottimizzazione

Super-ALPIDE (mock-up) setup: development of the wire-bonding procedure and FPC design



Super-ALPIDE chip: 18 ALPIDE chips over 2 rows in one big structure

- 16 chips readout through exo-FPC [bond over 7 mm pads vertical distance]
- 2 (external) chips readout through edge-FPC [bond at the same quota]



This setup has been realized to develop
and test the wire-bonding procedures for:

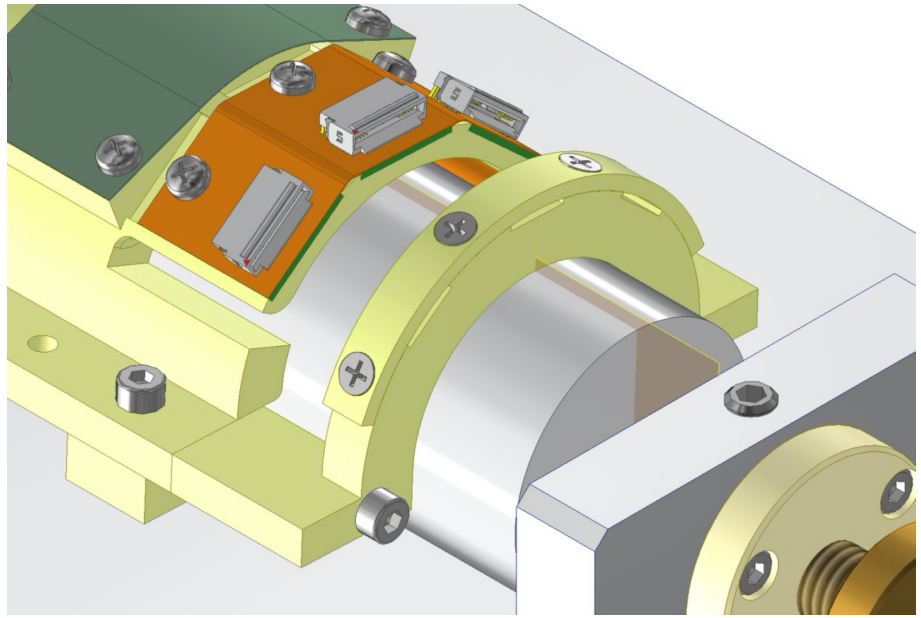
- Exo-FPC → first demonstrator of a working full half barrel in truly cylindrical shape
- Edge FPC → main interest for the further developments (final detector)

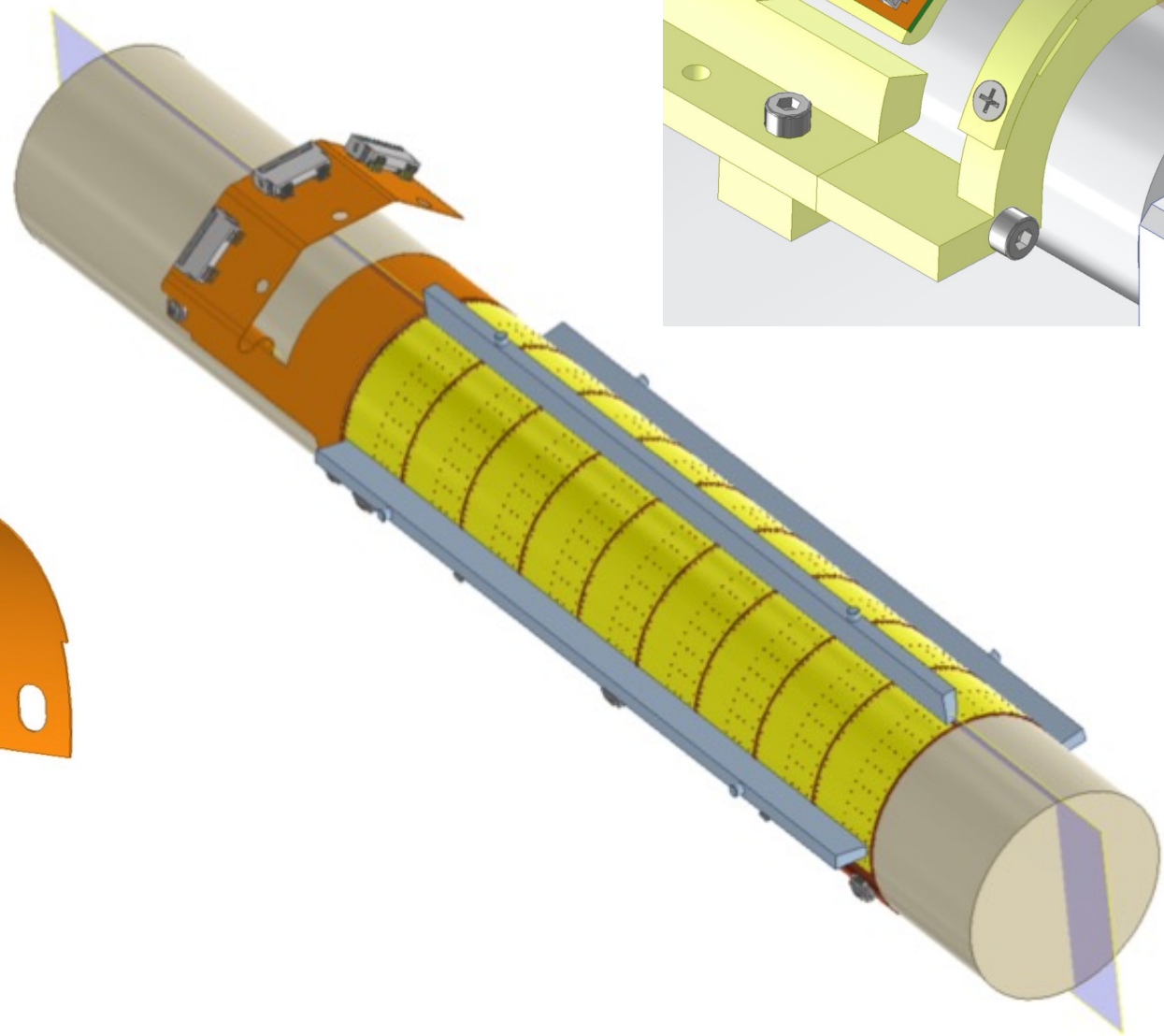
The present mandril holds a mock-up of the bended super-ALPIDE

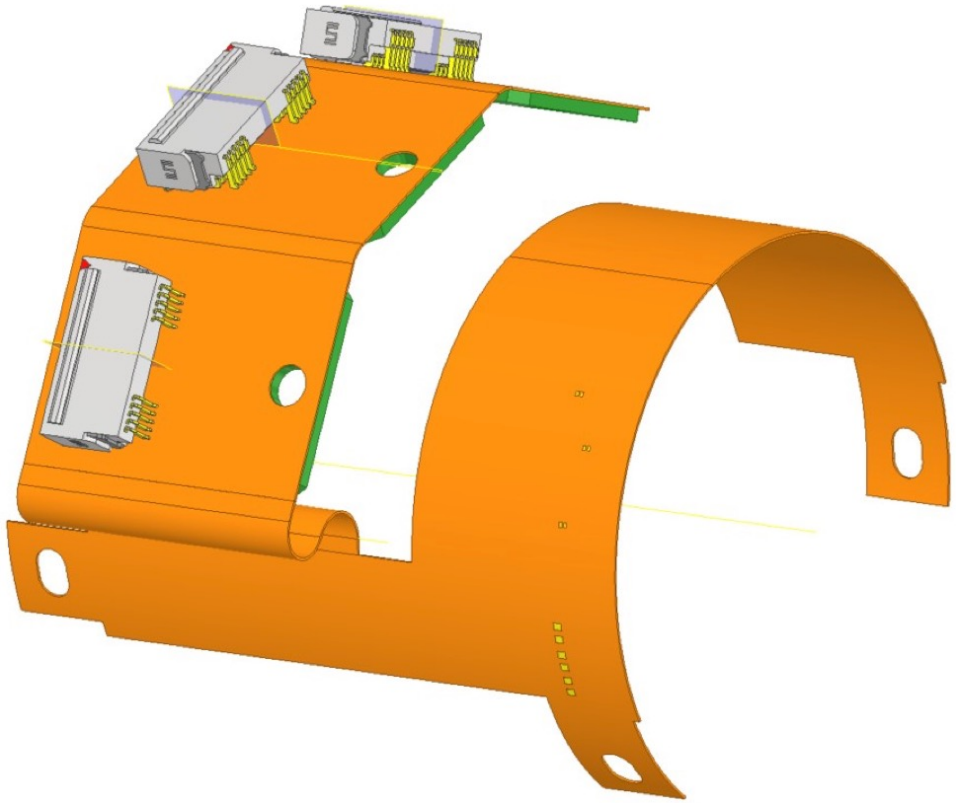
Super-ALPIDE setup

Edge-FPC

- Prototype of the final detector FPC
- Designed and integrated in Bari
- Under production
- Continue design toward next generation of large-area chips in 2022
  - new productions in 2022



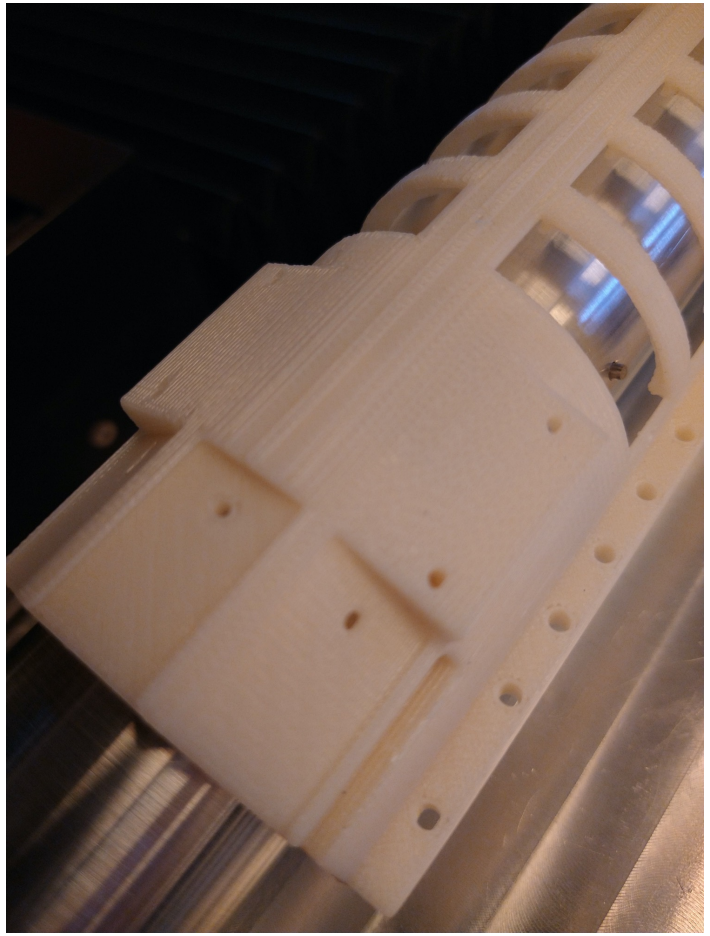


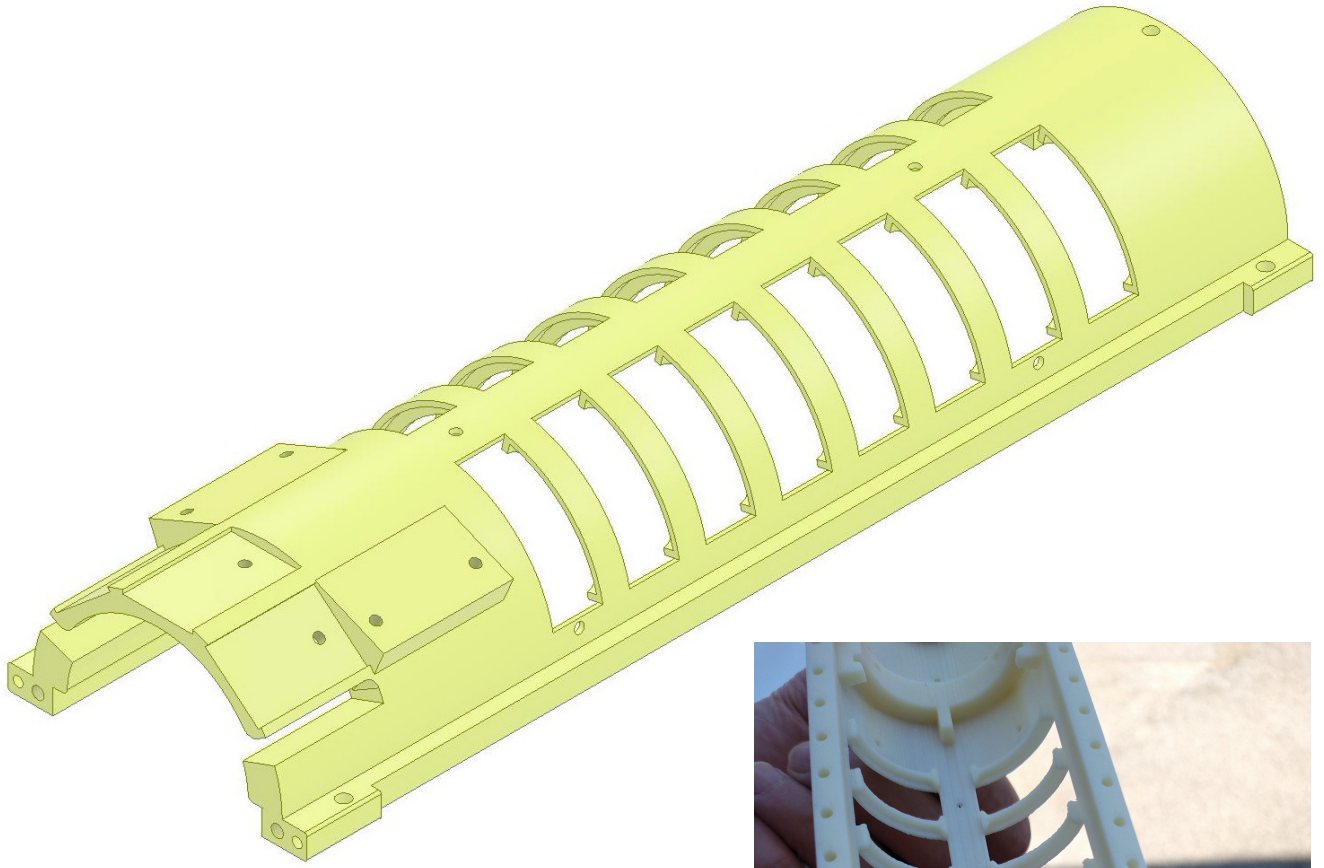


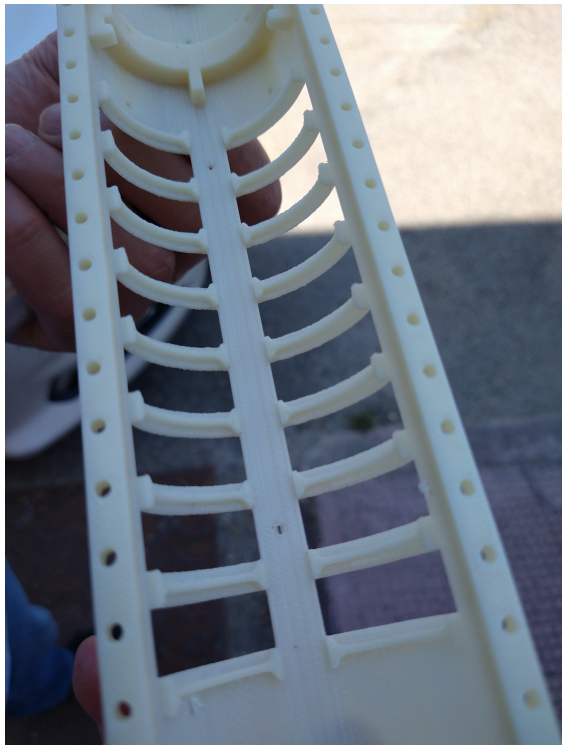
Super-ALPIDE setup

Exoskeleton

- First version designed by Magnus Mager
- Design finalization in Bari
  - edge-FPC integration
  - Bonding machine compatibility

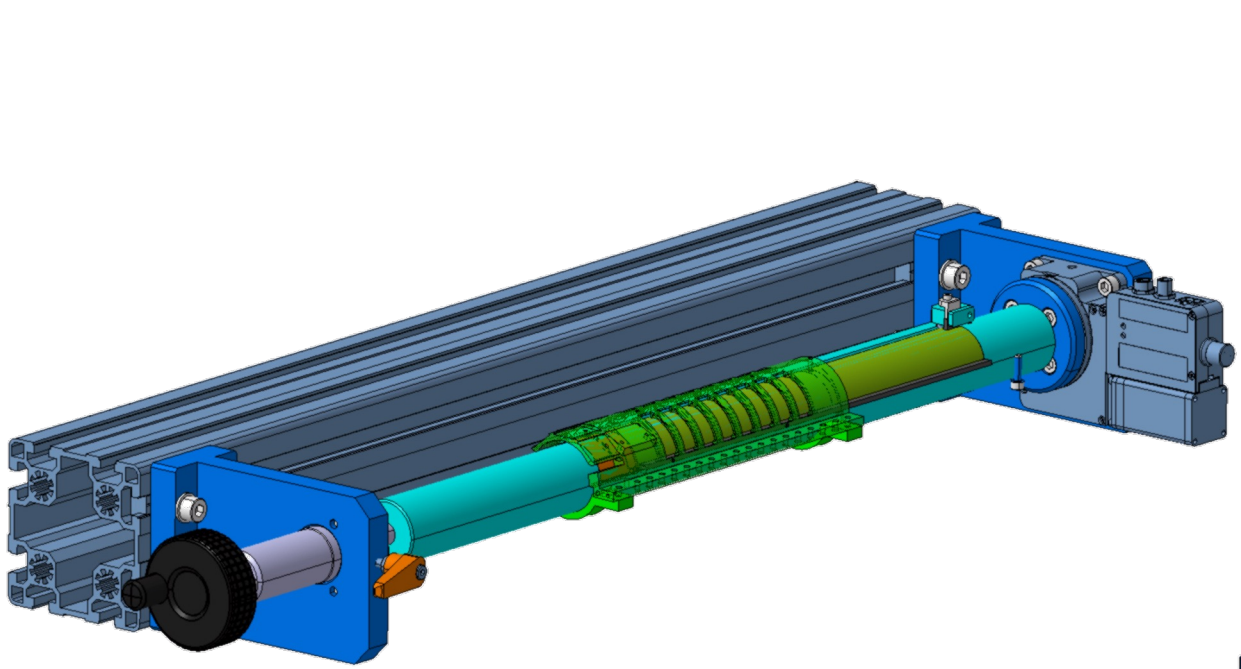


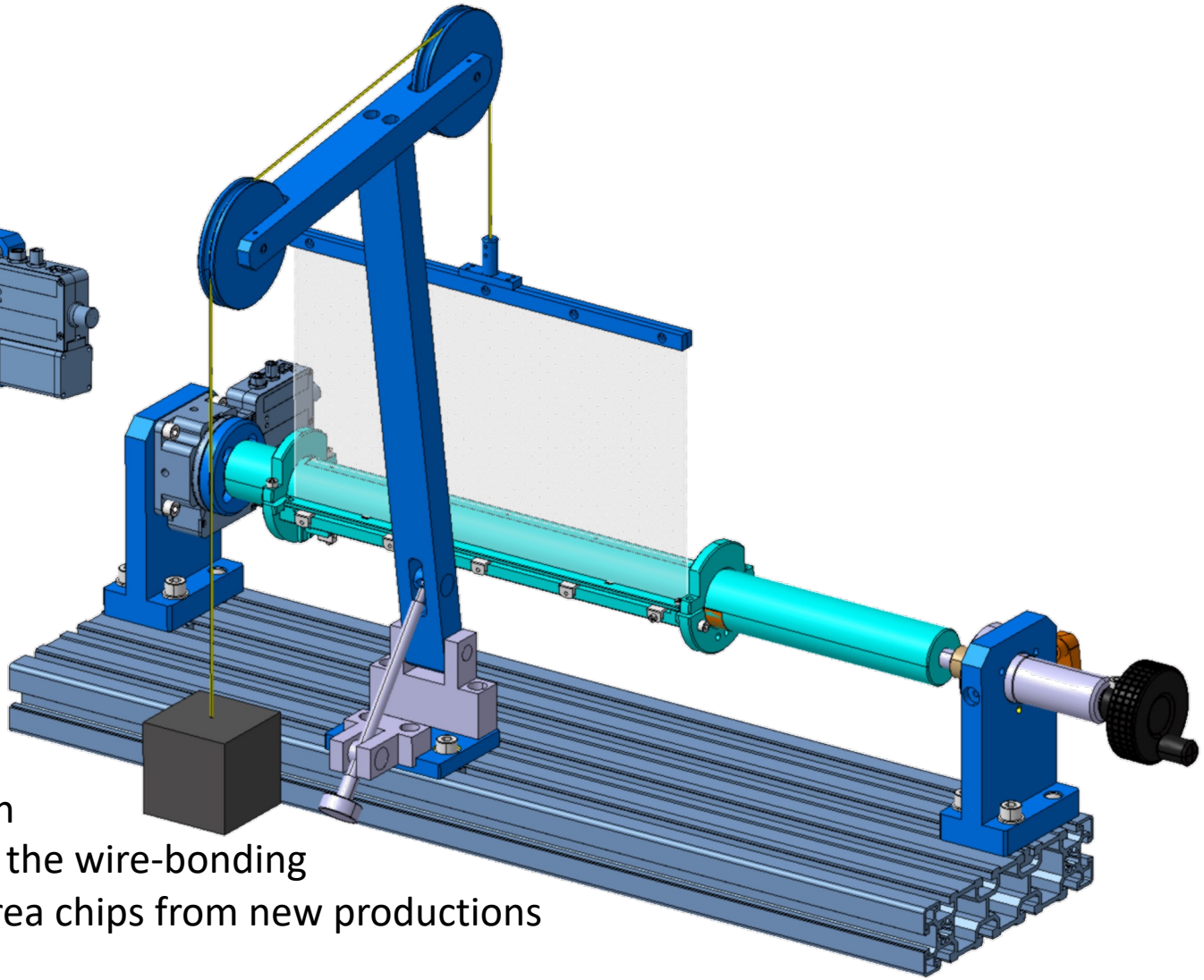




Super-ALPIDE setup - Bending tools

- Being designed at CERN
- Integration with the other components (exoskeleton and FPCs) in collaboration with Bari
- Next: full setup for complete super-ALPIDE assembly in Bari





The activity on the design of the edge FPC, its integration with the bending and assembly procedure of large area chips, and the wire-bonding procedure will be the focus of next year (2022), using large area chips from new productions