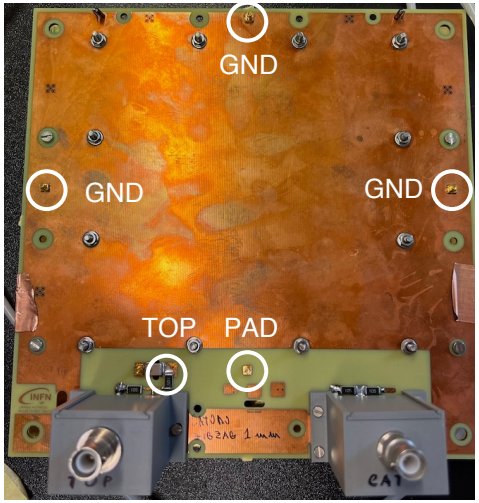
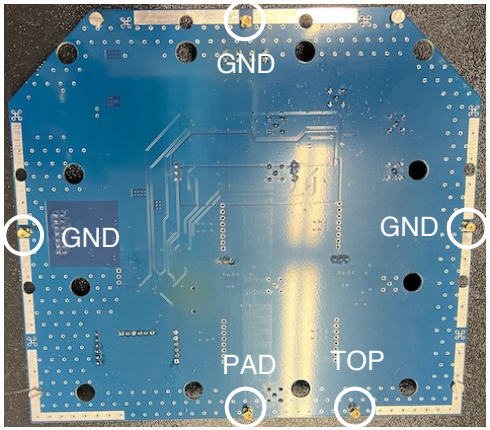
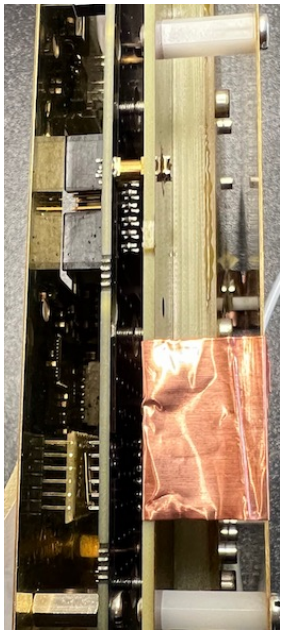
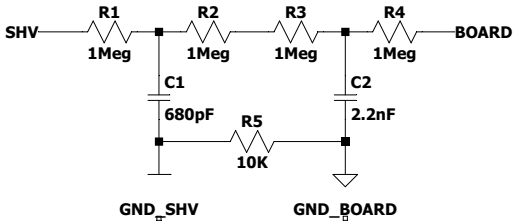
micro-RWELL
&
resistive detectors activity

URANIA BOARD MECHANICS & HV FILTERS



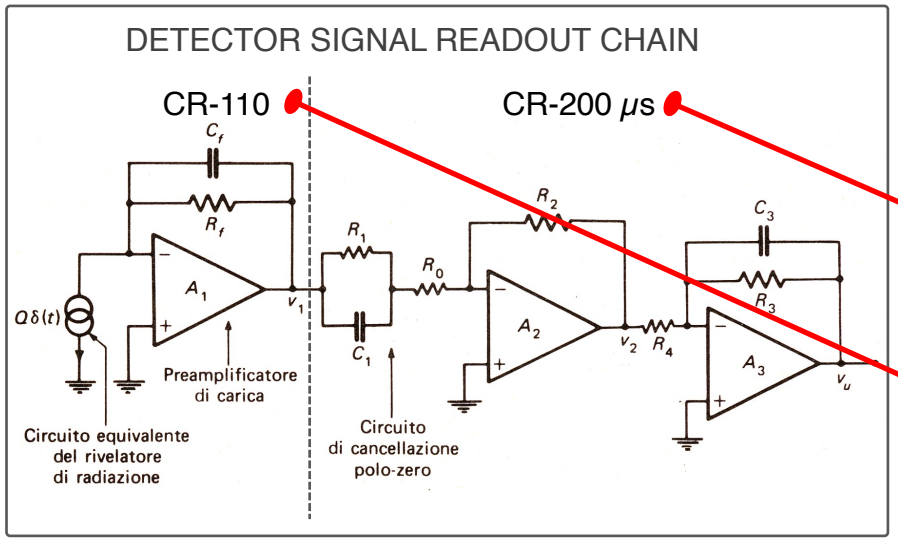


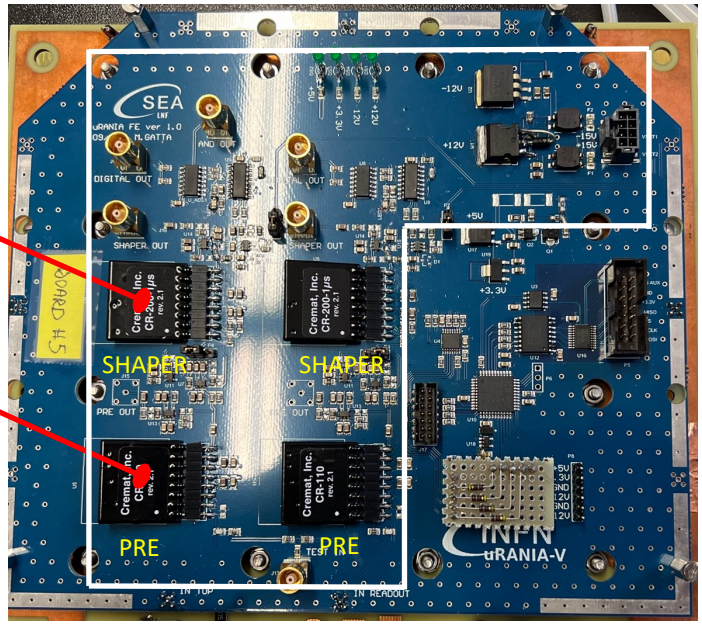


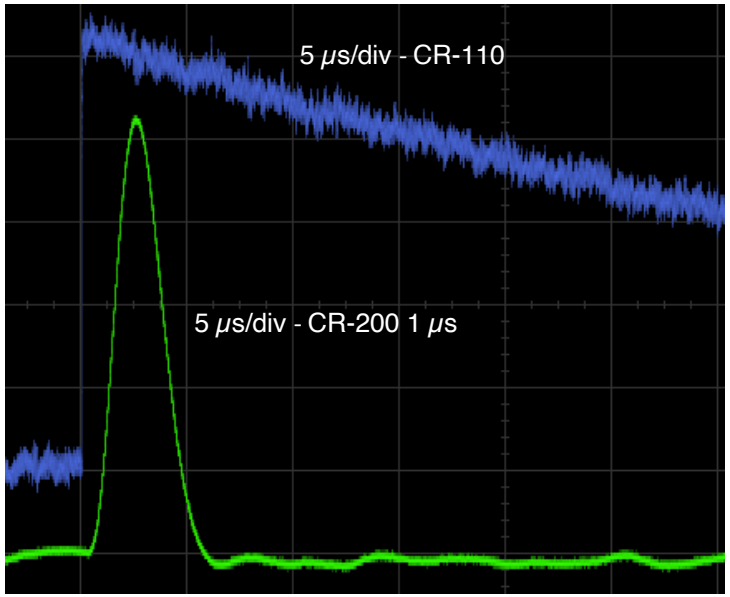


- Leaks on some filters probably due to wrong cleaning procedure and/or no passivation.
- Filter trace connectiond too close to the margin of the card

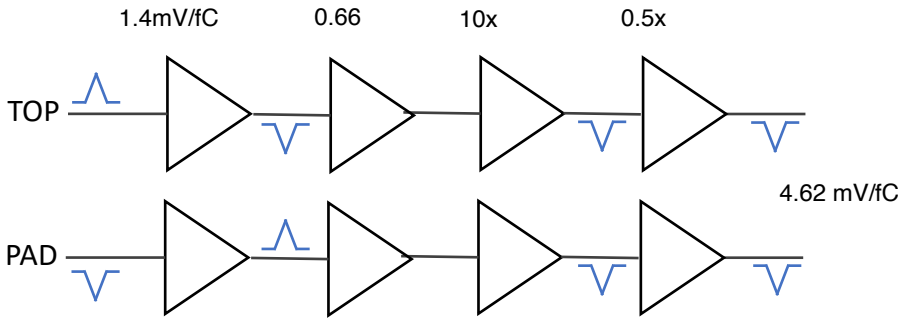
URANIA BOARD FEE



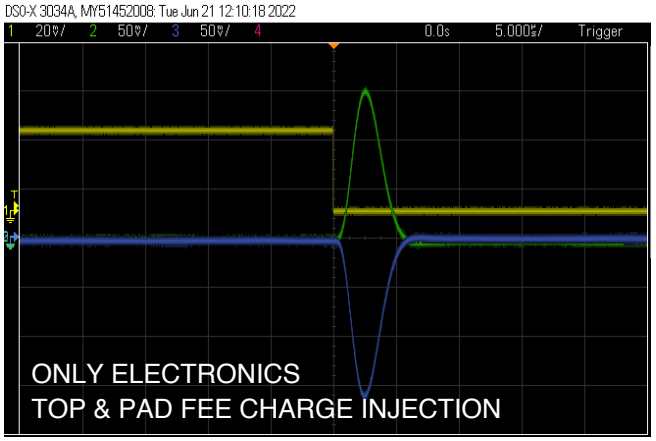


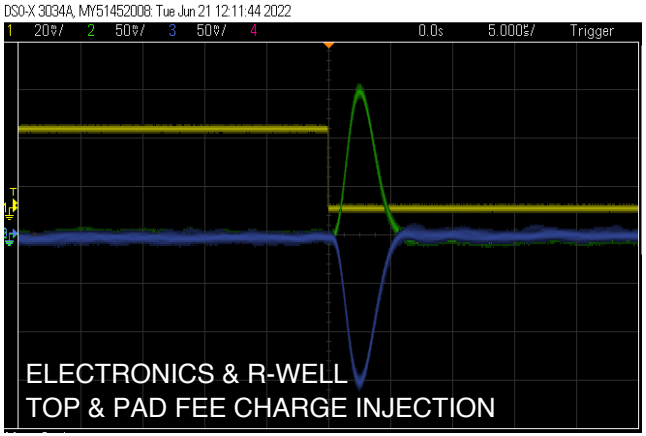


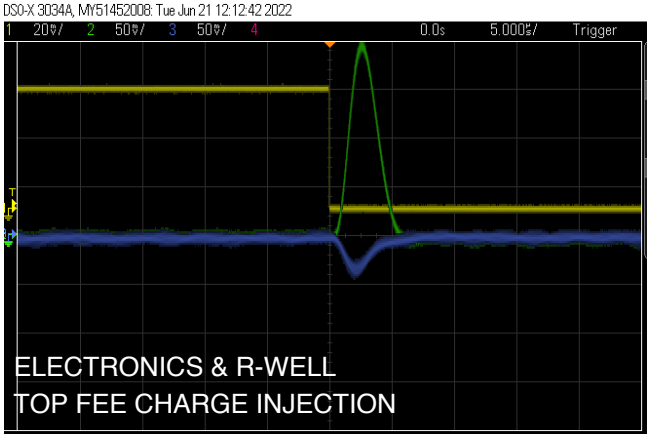
NOMINAL GAIN

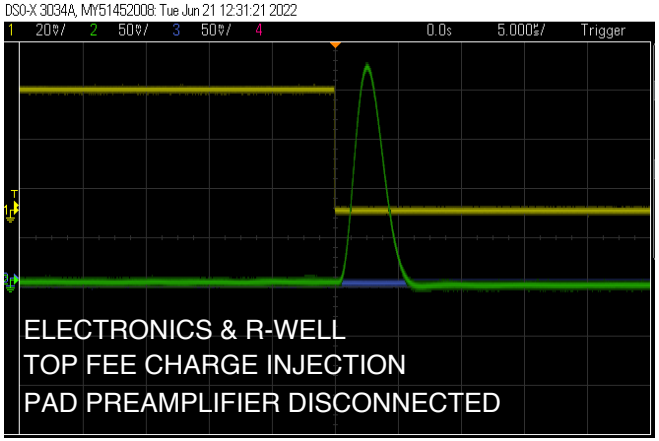


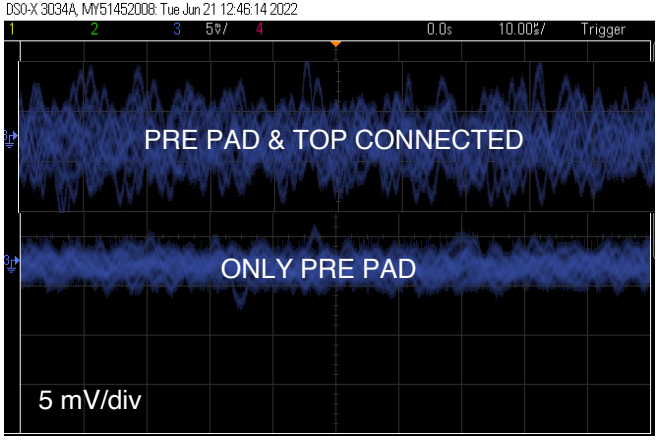
PAD-TOP COUPLING

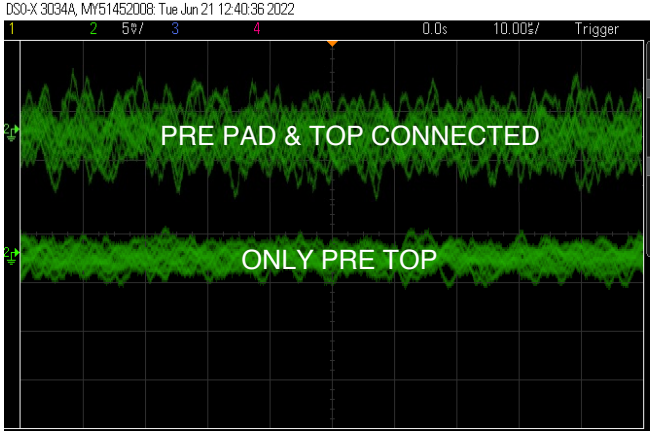






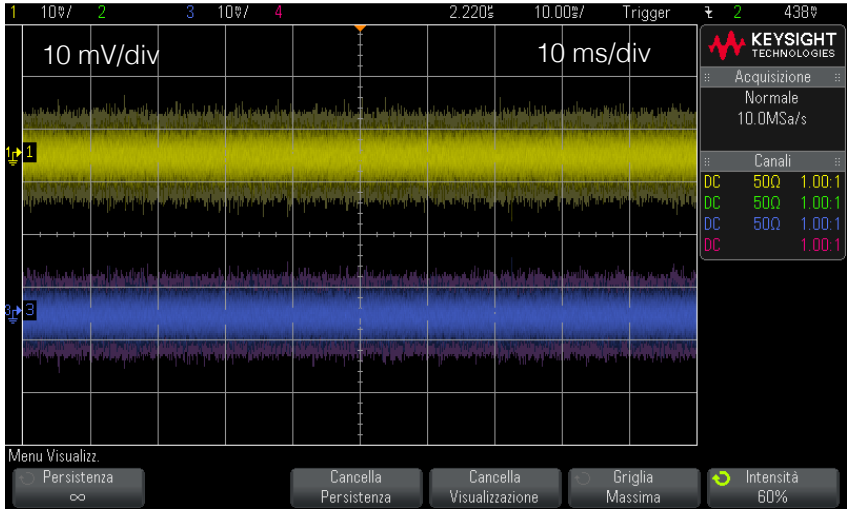




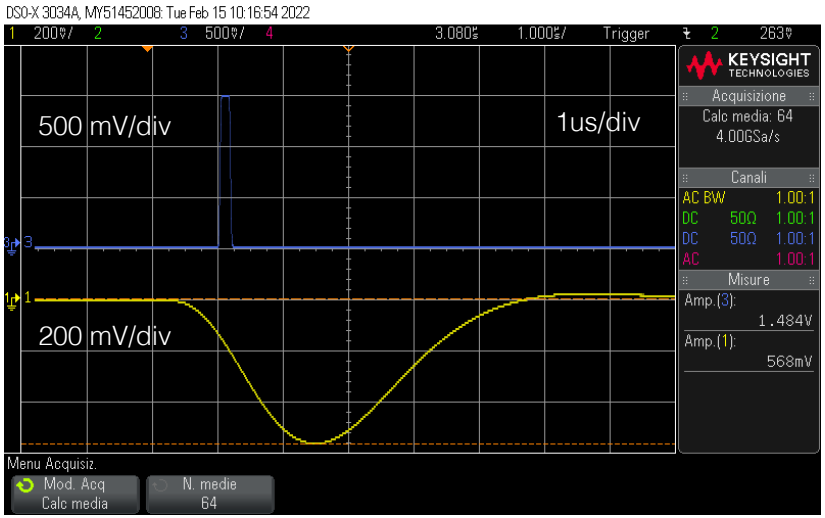


ANALOG SECTION

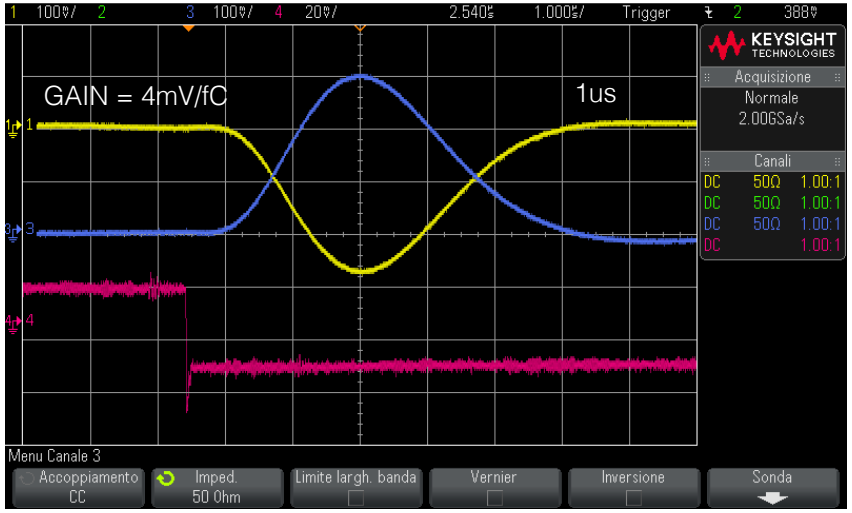
NOISE: NO HV CABLE/CONNECTOR



DISCRIMINATOR OUT

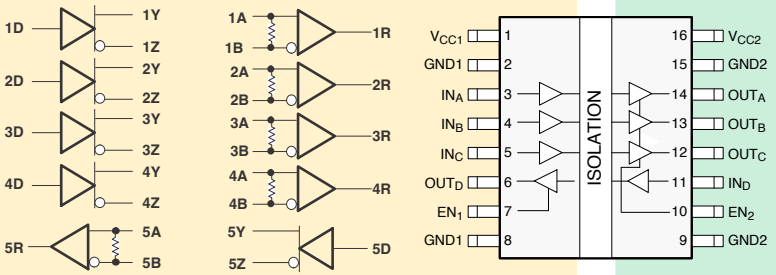


SELECTABLE OUTPUT POLARITY

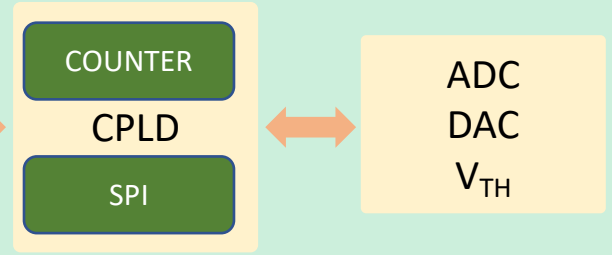


- PRE MAX OUTPUT SWING: +/- 3V (≃ 2pC)
- SHAPER MAX OUTPUT SWING: V_S – 0.5V (V_S max = +/- 13V)
  - GAIN = 10 → max V_{IN} ≃ 1.3 V

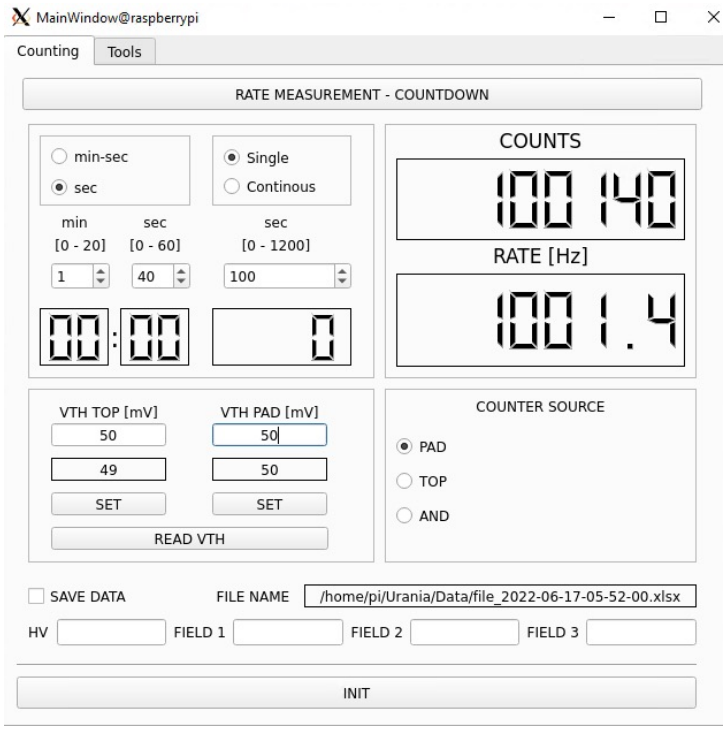
DIGITAL SECTION



Rpi Power Supply

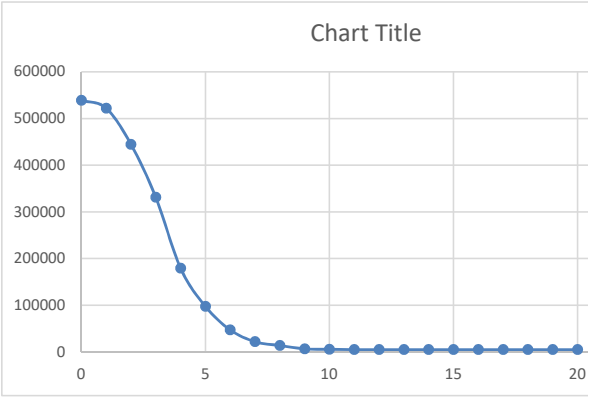


URANIA board Power Supply



mV	COUNTS
0	538990
1	522183
2	444562
3	331337
4	179543
5	97491
6	47253
7	21925
8	13719
9	6669
10	5645
11	5035
12	5014
13	5008
14	5009
15	5008
16	5008
17	5008
18	5008
19	5008
20	5008

PAD Threshold scan



CONCLUSIONS

MAIN FEATURES (ANALOG SECTION)

- CR-110 + CR-200 1us
- Gain ≈ 4 mV/fC (4.65 mV/fC @ $C_{IN} = 0$)
- Q_{IN} SAT ≈ 1 pC
- Input Noise ≈ 1.5 fC (measured - rms)
- CR110 input noise ≈ 4 erms/pF x 2nF ** ≈ 1.3 fC

- N. 2 channels
- Positive/Negative input polarity
- Preamplifier Out (x2)
- Shaper Out (x2)

** TOP - PAD capacitance

NB: FWHM ≈ 2.4 x Shaping Time

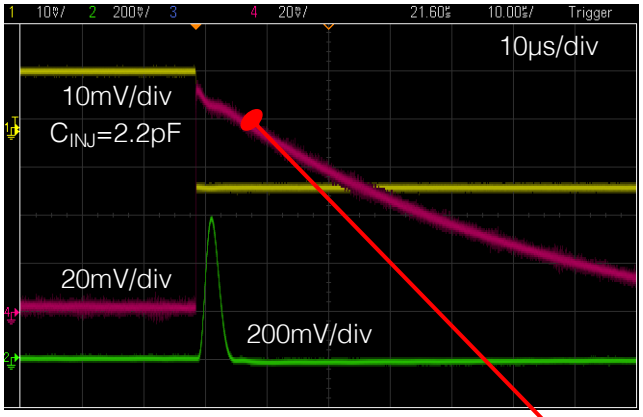
MAIN FEATURES (DIGITAL SECTION)

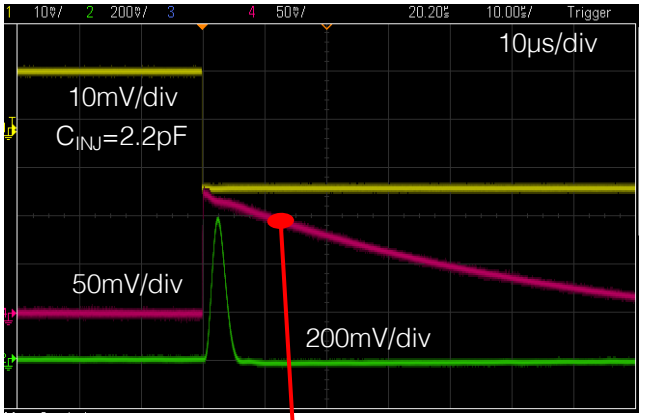
- 2 x V_{TH} sensing/setting
- 24 bits counter
- SPI interface
- Totally insulated control/readout lines

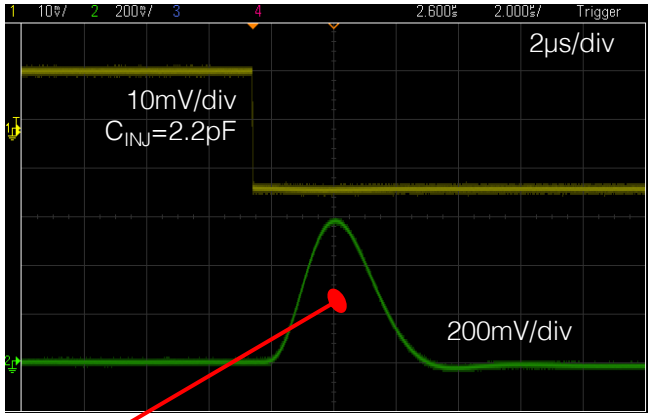
- Single Channel digital Output (positive/1.5V)
- AND Output (positive/1.5V)
- Threshold scan capabiliy

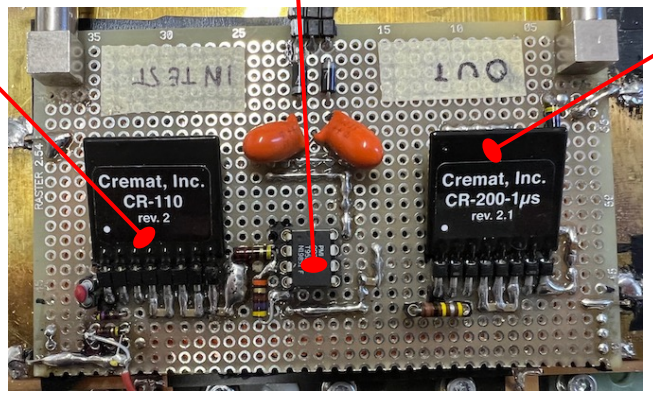
- EXCEL data file
- PyQt5 control GUI

SRPC FEE









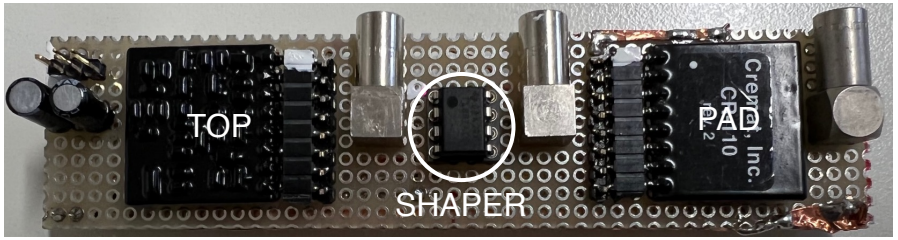
REAL GAIN ≃ 11 mV/fC

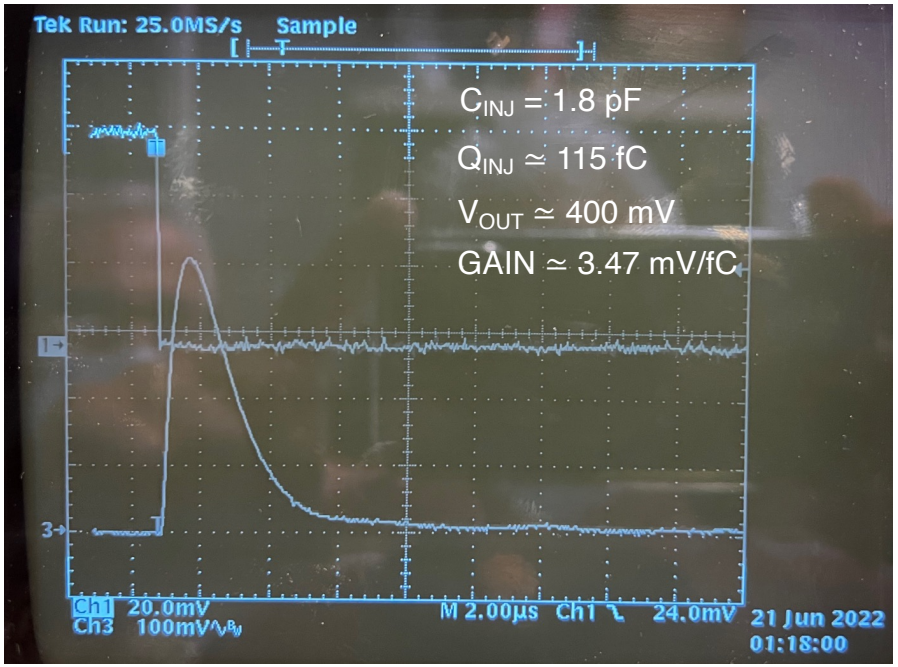
NOMINAL GAIN

25 mV (Test Pulse) x 2.2 pF x 1.4 mV/fC (CR-110) x 2 (AO) x 10 (CR-220) x 0.5 (line termination) = 770 mV/55 fC = 14mV/fC

55 fC

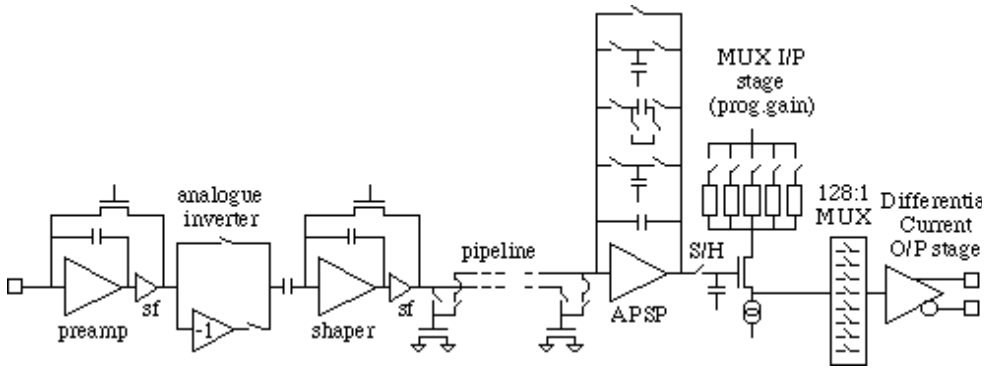
2021 URANIA FEE

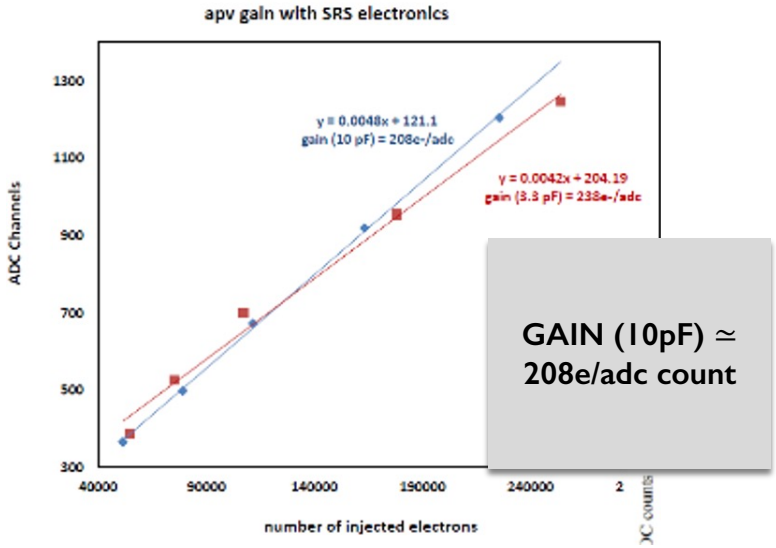




RWELL - FEE

APV25 Main Features (2001)





GAIN (10pF) ≃ 208e/adc count

MAIN FEATURES

- ★ 0.25μm CMOS process
- ★ 128 readout channels (> 100 Mrad tolerant)
- ★ 192 elements analog pipeline (160 used for latency 4 μs)
- ★ Differential output multiplexing
- ★ 40 MHz clock
- ★ GAIN (PREAMP) ≃ 5 mV/fC
- ★ GAIN (SHAPER) ≃ 5
- ★ SHPAING (CR-RC) ≃ 50 ns
- ★ LINEARITY ≲ 2% over 5 mip range
  - 1 mip ≃ 25000 e ≃ 4 fC
- ★ NOISE ≃ 300e + 40e/pF
  - es. assuming 20 pF input capacitance → σ_{erms} ≃ (300+800) erms ≃ 0.2 fC

DATA FRAME
Digital Header
(pipeline digital address)
analog sample #1
analog sample #2
----
mple 192

OPERATION MODE

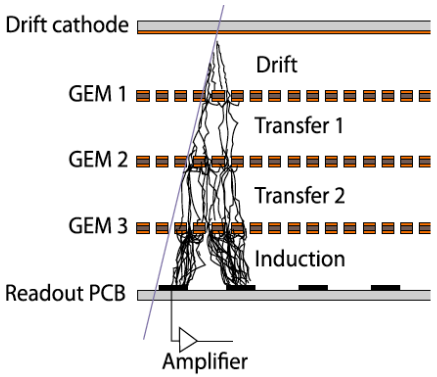
- peak mode
- deconvolution mode (three samples read from pipeline and combined (in a weighted sum) before output
- multi-mode (sequence of external triggers transmit a number of consecutive pipeline samples in consecutive data frames)

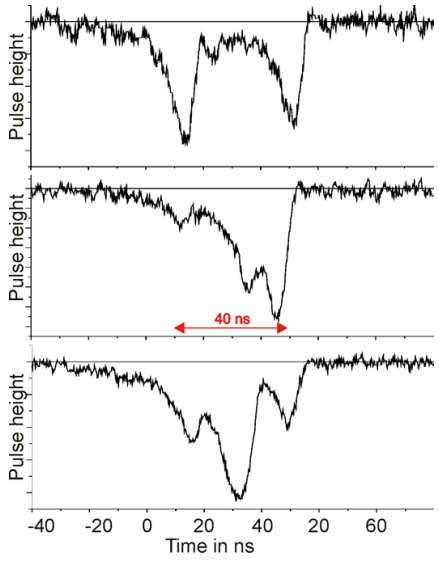
VFAT3 - CMS Upgrades (GEM Readout) - first submission: 2017

VFAT3 – 128 chs

- **128 channel chip**
- **Read +ve/–ve charge from GEM detectors**
- **Provide tracking and trigger information**
  - **Trigger : Fixed latency, granularity 2-4 channels**
  - **Tracking : Full granularity after LV1A**
- **LV1A capability: LV1A latency up to 20us, LV1A rate up to 1MHz**
- **Time resolution < 7.5ns (with detector).**
- **Integrated calibration and monitoring functions**
- **Interface to and from the GBT at 320 Mbps.**
- **Radiation resistant up to 100MRads (up to 1MRad needed for the muon application)**
- **Robust against single event effects**

Key Parameter	Comment
Detector charge polarity	Positive & Negative
Detector Cap. range	9-88 pF
Peaking Times (Tp)	25, 50, 75, 100, ns
Programmable gain	1.25 – 50 (mV/fC)
Max Dynamic range [DR] (fC)	20 (+-10), 50, 100, (200)
Linearity	<1% of DR
Power consumption	< 2.5 mW / ch
Power supply	1.2 V
Noise	~1100e (Tp=100ns, Cd=30pF)
Technology	TSMC 130nm





GEM SIGNAL PROCESSING

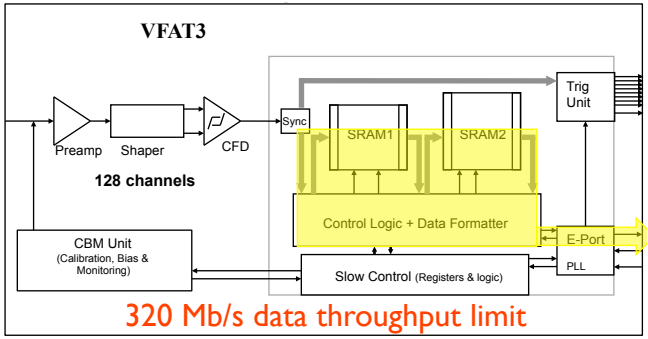
- ★ Slow shaping to integrate the GEM signal full charge
- ★ Improve S/N but time-walk affect timing resolution

VFAT3 FRONT-END:

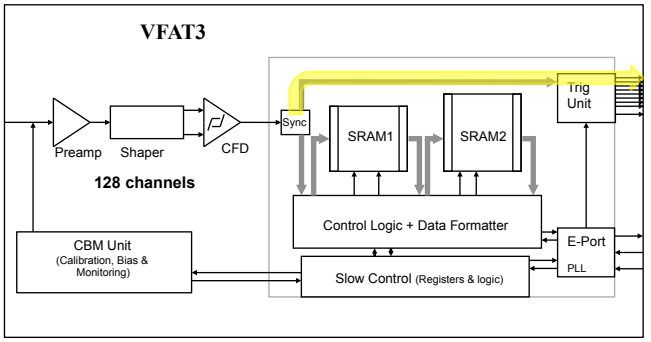
- ★ Programmable gain
- ★ Programmable shaping
- ★ CFD/LE discriminator

VFAT3 – Readout Architecture (I)

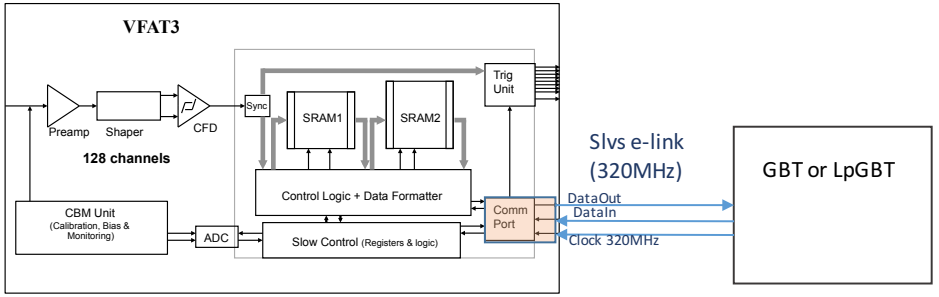
TRACKING DATA PATH



TRIGGER DATA PATH



COMMON PORT



TRACKING PATH

- ★ Full granularity after LV1a
- ★ time tag LV1a latency extended beyond 12.5us (designed to 26.5us)
- ★ Max LV1a rate beyond 1MHz

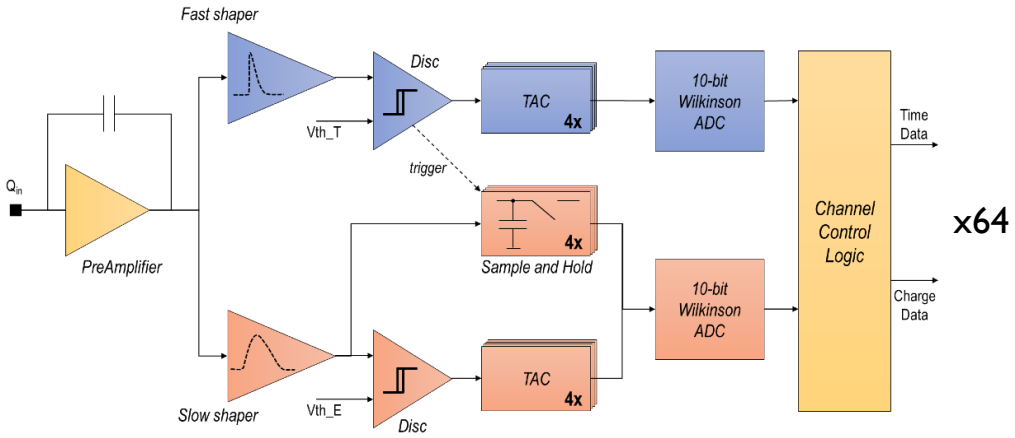
TRIGGER PATH

- ★ 8 sLVDS pairs @ 320Mbps
- ★ 64b/bx (128b/bx DDR)
- ★ Fast OR : Each pair of channels
- ★ DDR : Full granularity

COMMON PORT

- ★ Direct compatibility with GBTx and LpGBT
- ★ Bi-directional communication of control commands, slow control and data readout through a single port to the GBT

TIGER FRONT-END - BES C-GEM IT - 2016 FIRST PROTOTYPE

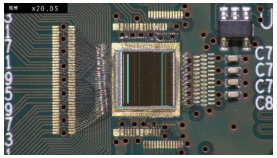


- ★ 4 TAC on T and Q branch of every channel
- ★ 64 bits word/hit
- ★ 4 TX SDR/DDR LVDS links@ 160 MHz – 8b/10b encoding
  - ★ 1.28 GBIT/S (250 kHz/channel – rate capability limited by front-end features)
- ★ 10 MHz SPI-like configuration link

TIGER FRONT-END MAIN FEATURES

- ★ 64 channels
- ★ 12 mW/ch power consumption
- ★ 100 kHz max sustainable rate
- ★ 50 fC input dynamic range
- ★ < 5 ns time resolution
- ★ 2000 erms @ 100 pF ENC
- ★ Charge & Time information
- ★ SEU protected
- ★ Tunable internal test pulse
- ★ 110 nm cmos process

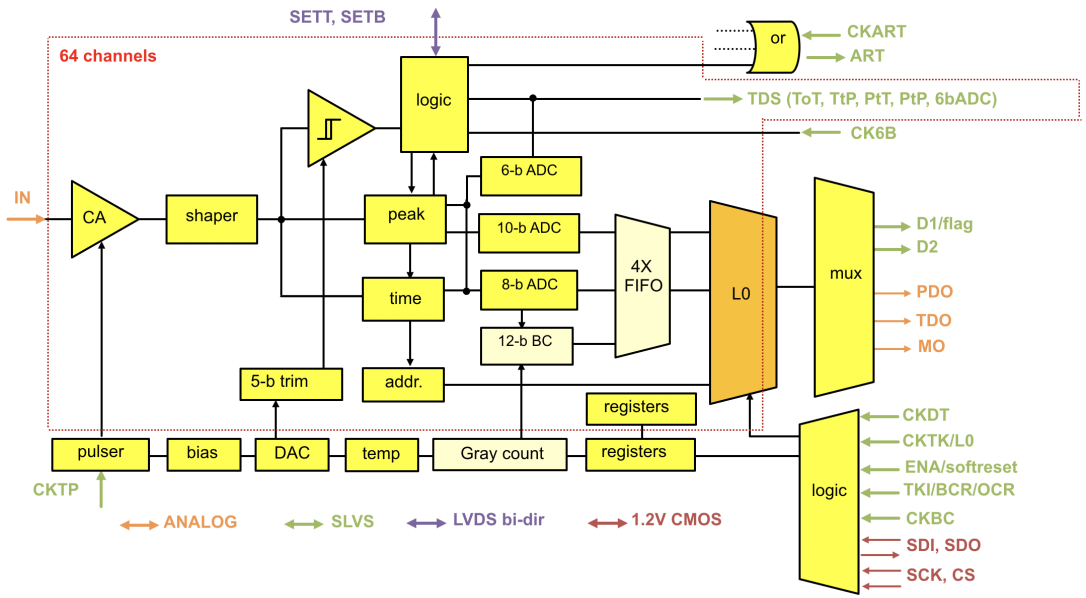
- ★ SEU protected
- ★ Tunable internal test pulse
- ★ 110 nm cmos process
- ★ 60 ns fast-shaper (time measurement)
- ★ 170 ns slow-shaper (charge measurement)
- ★ Time measurement accuracy limited by FE stage
  - ★ 50 ps fine time measurements

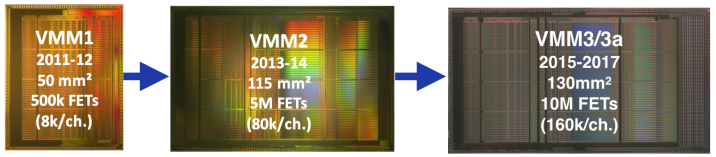


TIGER bonded on PCB

Front end board (FEB)

VMM3 (ATLAS MUON UPGRADES - MicroMegas & sTGC)





Continous Mode Operation

- 38 bits
- 2 Outputs @200MHz DDR

flg	1-bit
thr	1-bit
addr	6-bit
ampl	10-bit
time	8-bit
BC	12-bit

- Mixed mode with peak & time analog output + address (external ADCs)
- Digital continuous with internal ADCs and 38-bit data at 2 outputs with 200MHz DDR, trigger-less or with external trigger and auto reset
- Level-0 processor external trigger mode with 64-deep latency FIFO programmable acceptance windows with 8b/10b encoding

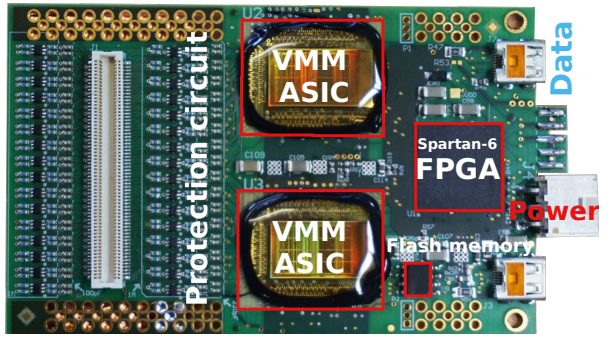
VMM3 (ATLAS MUON UPGRADES - MicroMegas & sTGC)

VMM3 – 64 chs

- Design
  - First rel: 2012-VMM3: 2016-130 nm
- Input Stage
  - Gain: 0.5, 1, 3, 4.5, 6, 9, 12, 16mV/fC
  - Shaping: 25, 50, 100, and 200 ns
  - Full baseline return: less than 600 ns
  - Detector Capacitance: few pF to 3 nF
- TIME DETECTOR
  - TAC circuit (threshold crossing/peak time - BC clock)
    - Ramp duration 60/100/350/650 ns)
- ADC
  - 6/8/10 bits - 250 ns conversion time
- READOUT MODE
  - Two-Phase mode: Acquisition + Readout
  - Continous mode: simultaneous R/W operation (4 MHz max rate x channel - 38 bits data - 4 events FIFO - 2 lines @200 MHz)
  - Lo mode: ATLAS RO (Latency); two serial lines @ 160 MHz Double Data Rate; 640 Mbits/s → 560 Mbits/s max BW including data encoding 8b/10b protocol)
- FAST OUTPUTS
  - Direct Data Output: ToT, TtP, PtT, 10ns pulse occurring at peak (PtP) , address in Real Time (channel number of first hit), 6 bits low res ADC value (25 ns conversion time)
- NEIGHBOURING LOGIC

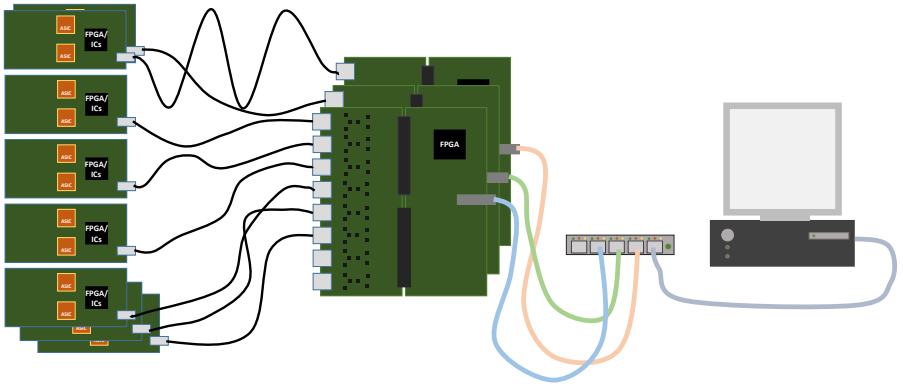
- MAX INPUT RATE
  - 4MHz (limited by the
- DATA OUTPUT
  - 38 bits/hit
  - 4 buffers
  - 2 data lines @ 200 MHz - DDR 800 Mbit/s Max
- RADIATION TOLERANCE
  - Single Event Upset & Total Ionizing Dose

VMM3 Hybrid
(APV25 interchangeable)

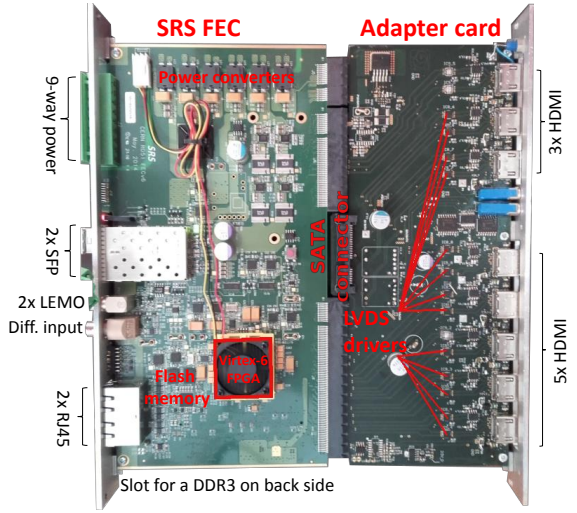


VMM3 – THE ECOSYSTEM (≈ 20 k€)

Up to 16 hybrid boards (2048 chs)



Hybrid → HDMI cable → Adapter card + FEC → Ethernet → Switch →Ethernet → PC

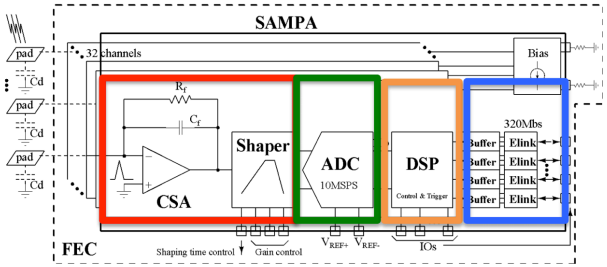


"The RD51 collaboration has developed a hybrid front-end for triggerless SRS read-out system, incorporating initially VMM2 ASICs, the final version planned for mid 2016 will integrate VMM3 ASICs. Compared to the purely analogue APV ASICs, the VMM ASICs integrate both ADCs and Zero suppression, al- lowing for considerably higher readout bandwidth and trigger rates up to 1 MHz. The VMM2-based hybrid which has been tested by us integrates two VMM2 ASICs, corresponding to 128 channels. A FPGA contains the interface logic for Data, Trigger, Clock and Configuration (DTCC) via HDMI links to the SRS backbone"

** a complete system should cost about 20 k€

SAMPA ASIC (ALICE TPC RO)

SAMPA overview (2)



32 FEs (CSAs + Shapers)

32 ADCs

Output Drivers

DSP

SAMPA was designed by Sao Paulo University (Brasil) and Bergen University (Norway) for ALICE TPC and MCH systems

- TSMC CMOS 130 nm, 1.25V technology
- 32 channels, Front-end + ADC + DSP
- package size ≤15x15mm^2 (total footprint)
- ADC: 10-bit resolution, 10MS/s, ENOB>9.2
- DSP functions: pedestal removal, baseline shift corrections, zero-suppression
- Data transmission: up to 11 e-link at 320 Mbps to GBT, SLVS I/O
- Power < 32 mW/channel (Front End + ADC)

TPC Mode

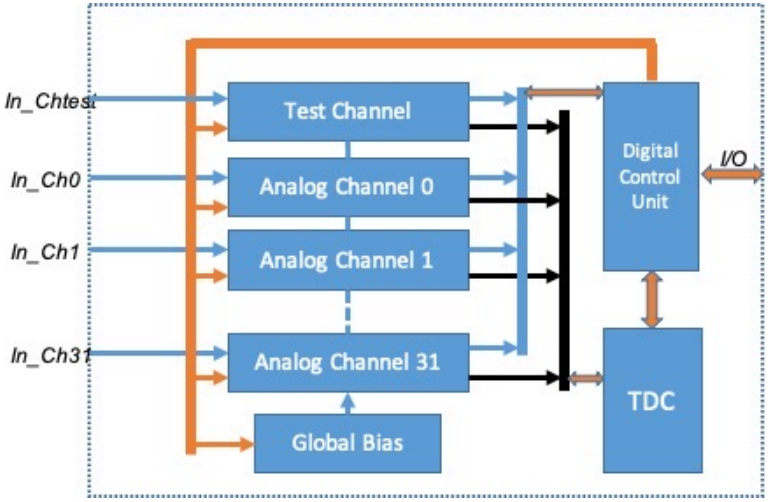
- Negative Input charge
- Sensor capacitance: 12 – 25 pF
- Sensitivity: 20mV/fC & 30mV/fC
- Noise: ENC ≤ 580 e$^-$ @ 18.5pF
- Peaking time: ~160 ns, return to
- Baseline return: <500 ns

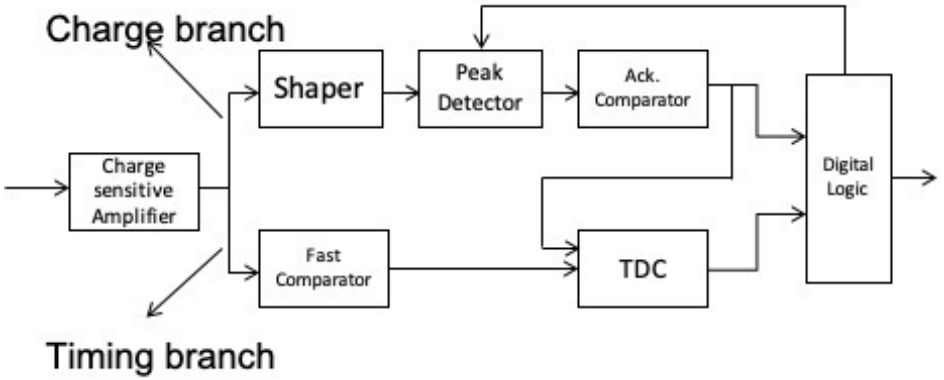
MCH Mode

- Positive input charge
- Sensor capacitance: 40–80 pF
- Sensitivity: 4mV/fC
- Noise: ENC ≤ 950 e- @ 40pF
  1600 e- @80pF
- Peaking time: ~300 ns
- Baseline return: <550 ns

* ALICE TPC upgrade and the SAMPA asic [Christian Lippmann]

FATIC ASIC (New Development)





Analog Section:

- 32 Front-end channels:
  - Fast output: designed for timing measurements
  - Slow output: input signal acknowledgement and charge measurement
  - Global Bias: temperature and power supply independent, internal calibration, bias monitoring

Digital Section:

- Control Unit:
  - 320 MHz SLVS I/O link
  - Channel & Global bias adj. bits
  - TDC control

CSA settings:

- Input signal polarity: positive & negative
- Gain: High ≈ 50mV/fC, Low ≈ 10 mV/fC
- Recovery time: adjustable

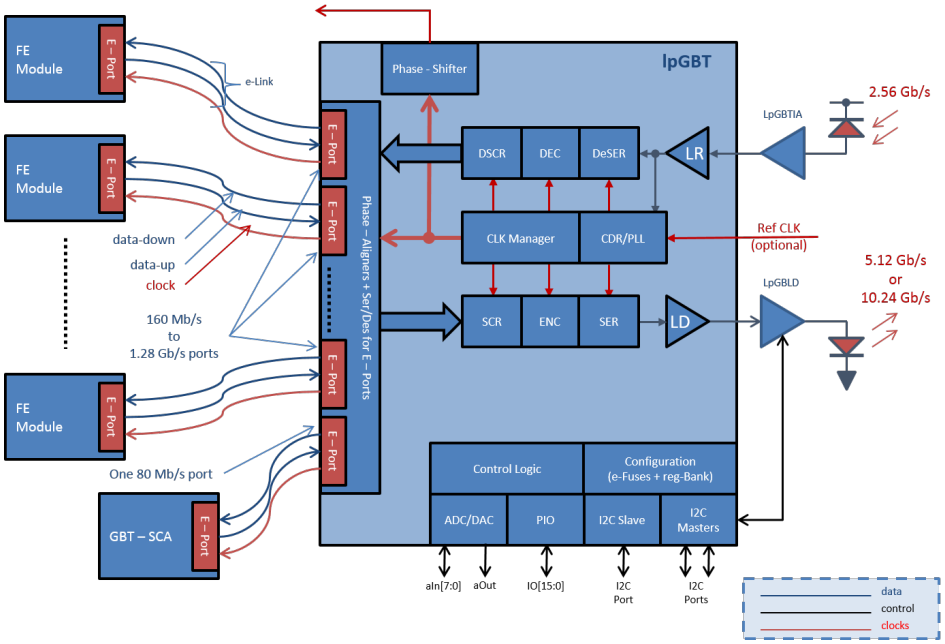
Shaper settings:

- Peaking time: 25ns, 50ns, 75ns, 100ns (polarity adj)

TDC resolution:

- 100ps (5 bits fine + 16 bits coarse)

LpGBT



lpGBT (Low Power Giga Bit Transceiver): radiation tolerant serializer/deserializer asic used to implement multiporpose high speed bidirectional OL

up to 2.56 Gbps in downlink and up to 10.24 Gbps in uplink

Provide distint path for timing and Trigger Control, Data Acquisition and Slow Control

It is possible to implement many input combination; ex: selecting uplink at 10.24 Gb/s with FEC5 it is possible to have 3 at 1.28 Gb/s, 4 at 640 Mb/s and 8 at 320 Mb/s

Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

THANK YOU