



UNIVERSITÀ DI PISA



Sant'Anna
Scuola Universitaria Superiore Pisa

FALAPHEL Meeting

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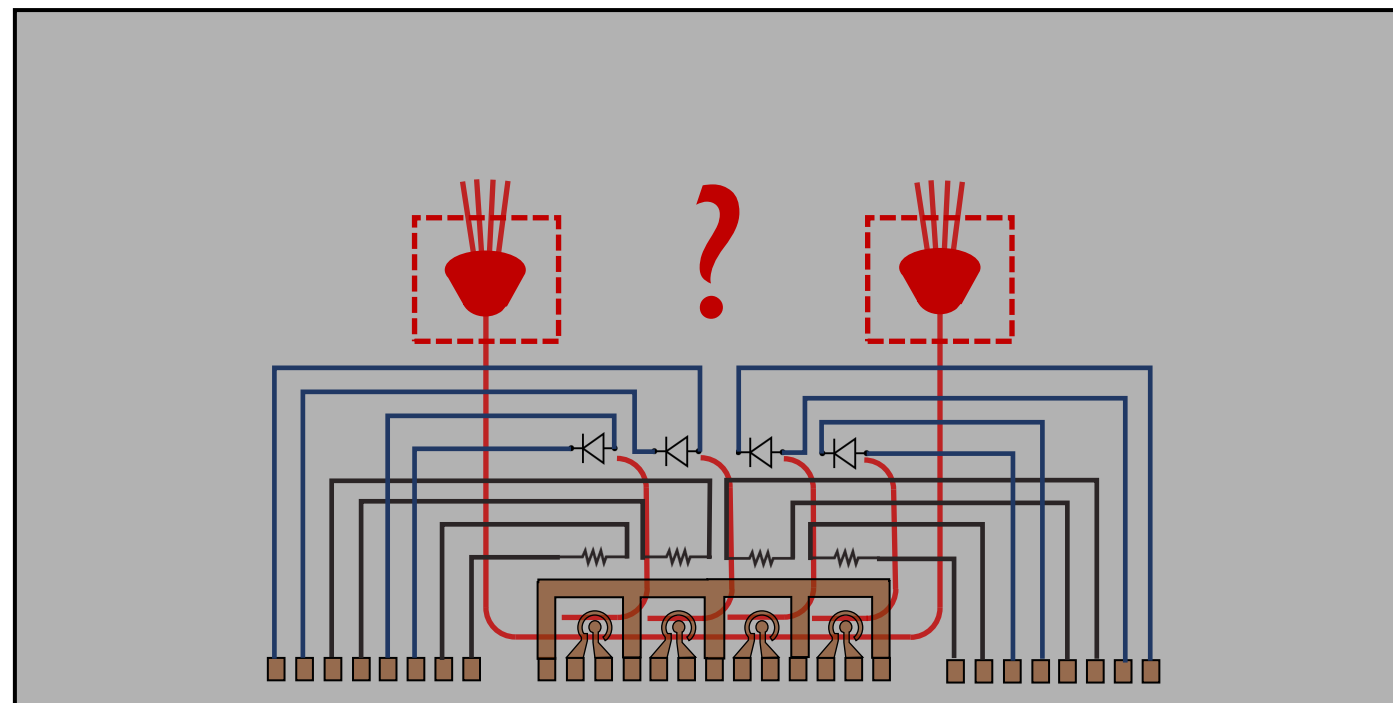
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PIC v2 – Overview

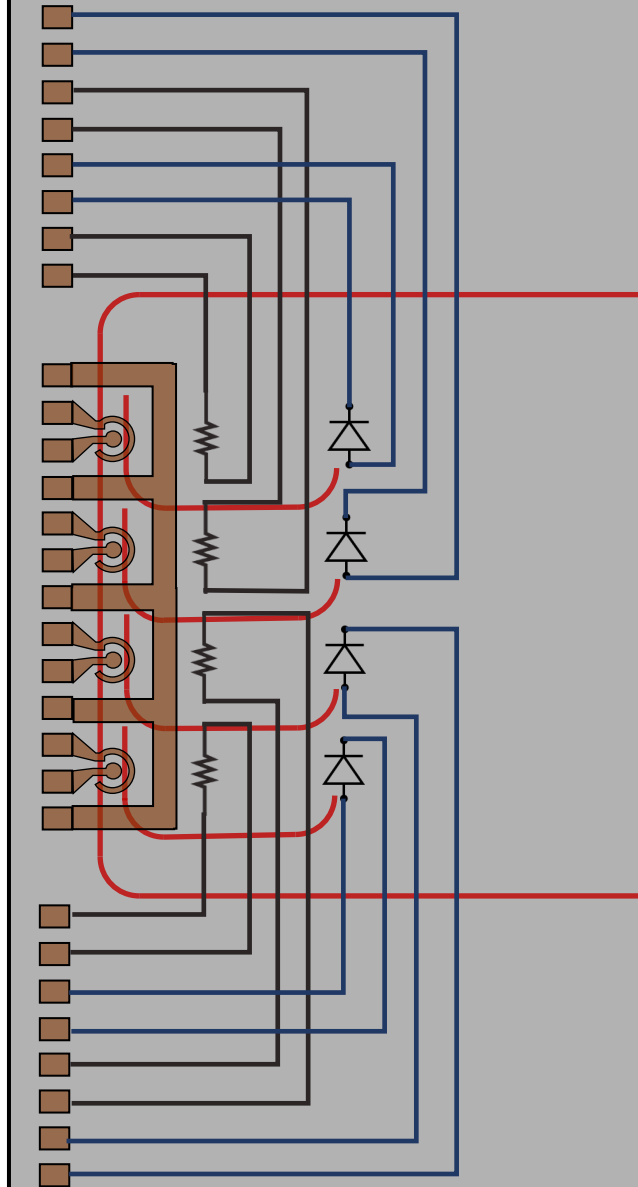
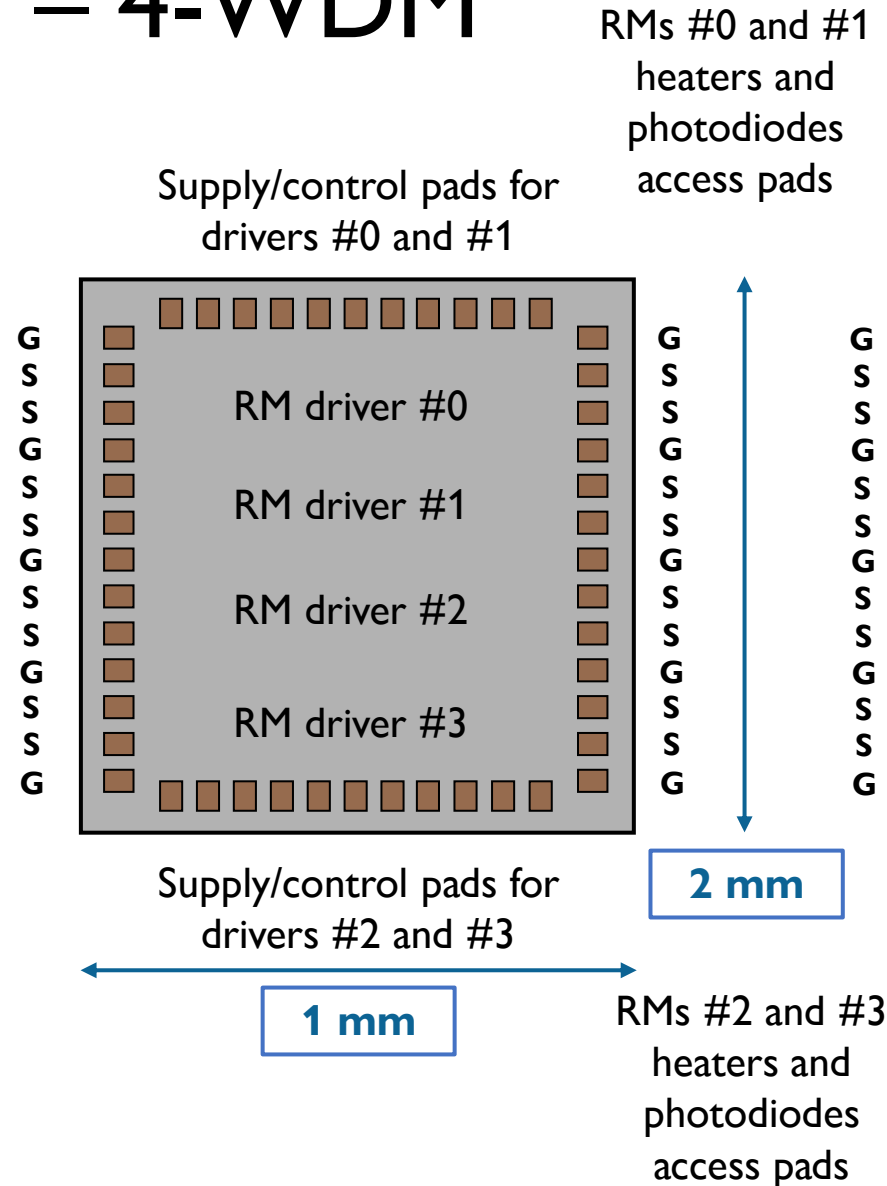
- N -WDM demonstrator with *all-pass* Imec's RMs (no feedback!)
 - N -WDM demonstrator with *add-drop* custom RMs. **Achtung!** Design should be done from scratch: test structures give only limited info for this type of RMs
1. Decision to take: $N = 2$ or 4 ?
 2. Decision to take: integrated or external wavelength MUXs ?



- **Achtung!** Complete demonstrators can presumably stay only on the “long” PIC side. At most 2 (4) complete 4-WDM (2-WDM) structures can be accommodated on the PIC

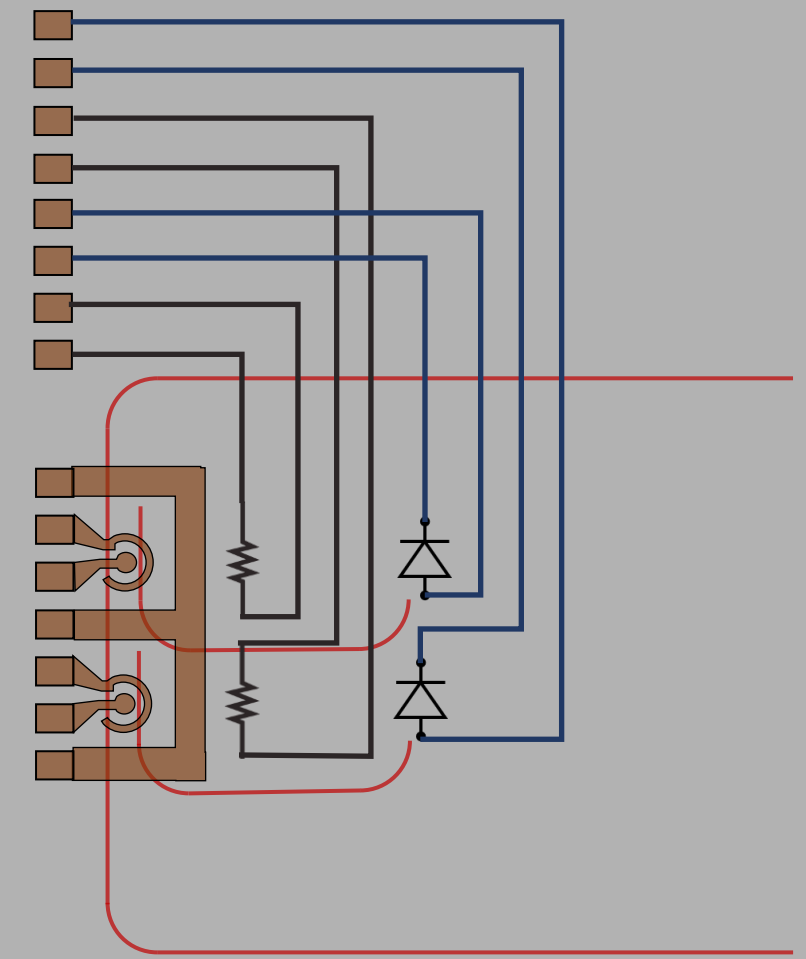
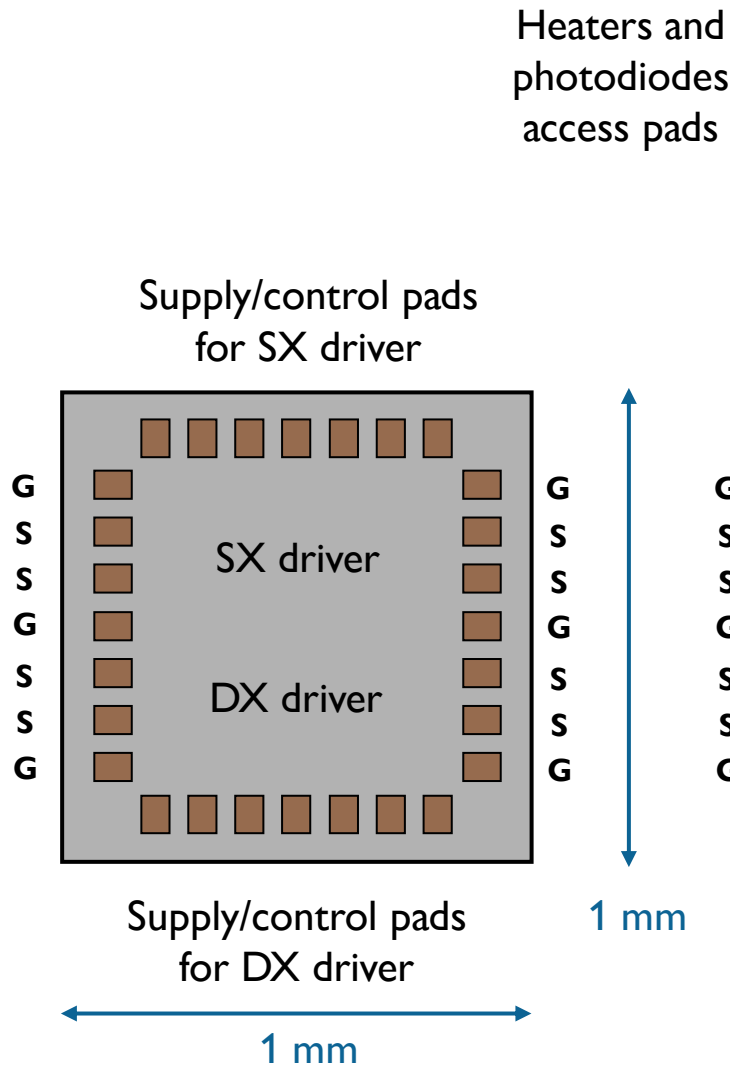
PIC-EIC Integration – 4-WDM

- Differential driver architecture to double effective peak-to-peak voltage swing on RM
- RM as differential load on a CML-like output stage requires signal-signal (SS), i.e., anode-cathode, pad configuration
- **GSSG** pattern preferred to limit RM-to-RM cross-talk
- **4-WDM** demonstrator: 4 drivers in a single EIC (flip-chip packaging constraints permitting)



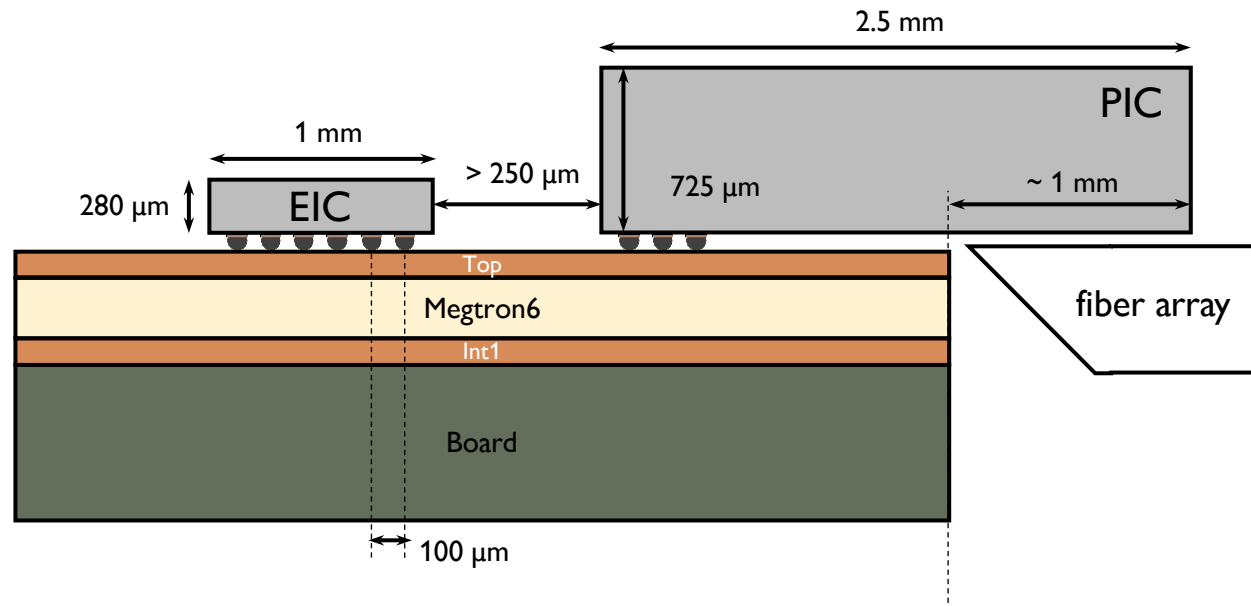
PIC-EIC Integration – 2-WDM

- Differential driver architecture to double effective peak-to-peak voltage swing on RM
- RM as differential load on a CML-like output stage requires signal-signal (SS), i.e., anode-cathode, pad configuration
- **GSSG** pattern preferred to limit RM-to-RM cross-talk
- **2-WDM** demonstrator: 2 drivers in a single EIC

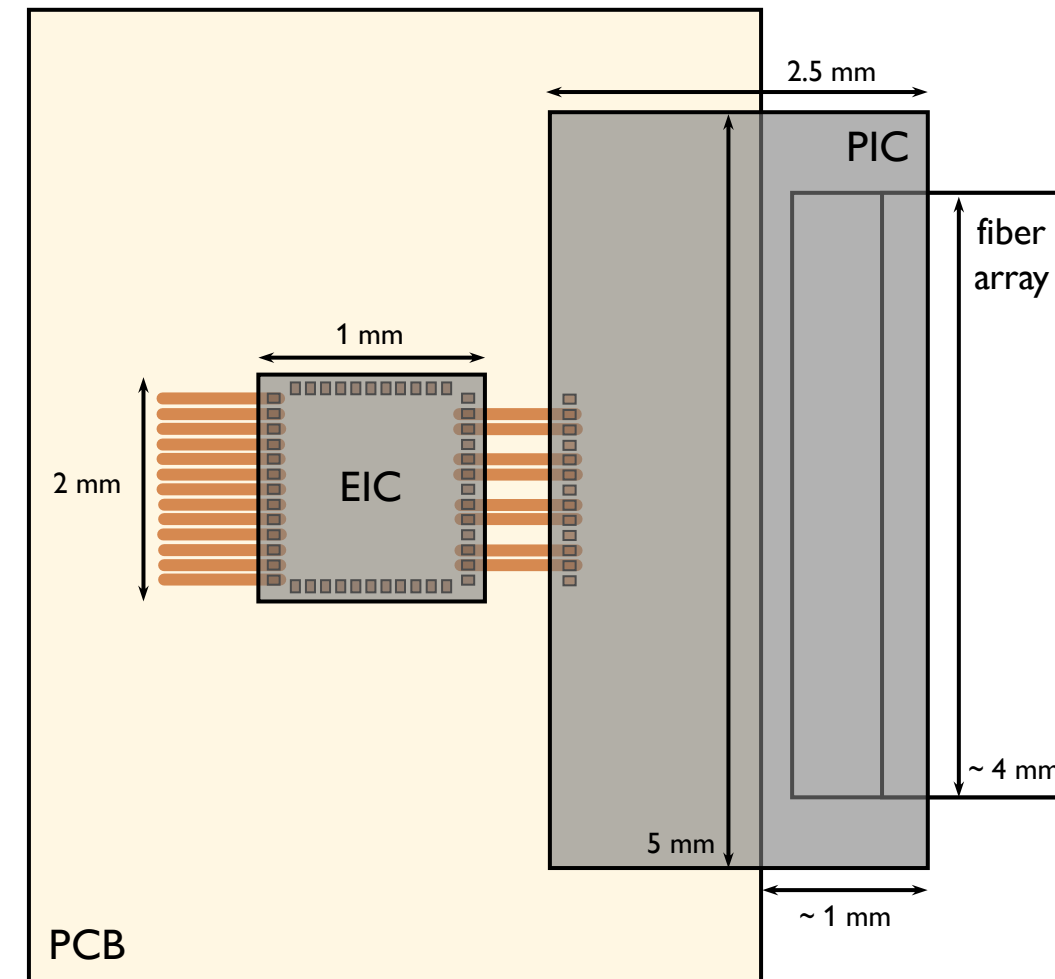


2.5-D RF-PCB – Single-bumping

Side view



Top view



- **Interposer-free** flip-chip design
- Au stud-bumping (CamGraphic) + solder jetting (Valencia) + die attach (CamGraphic)
- Viable solution also for some devices included in the current PIC

Thanks for the attention