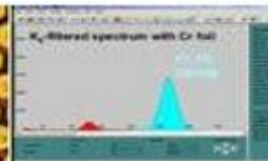
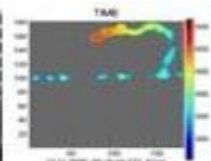
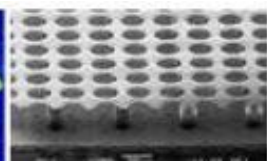
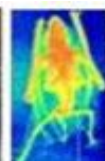
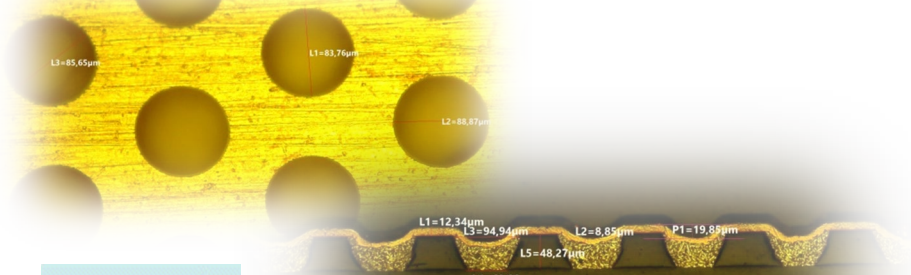




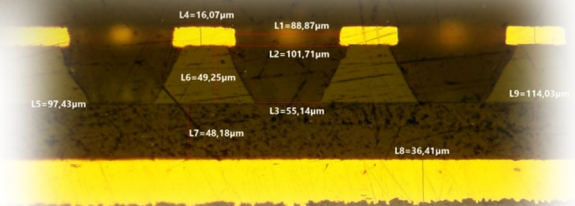
RD51 Collaboration



μ -RWELLS in LHCb

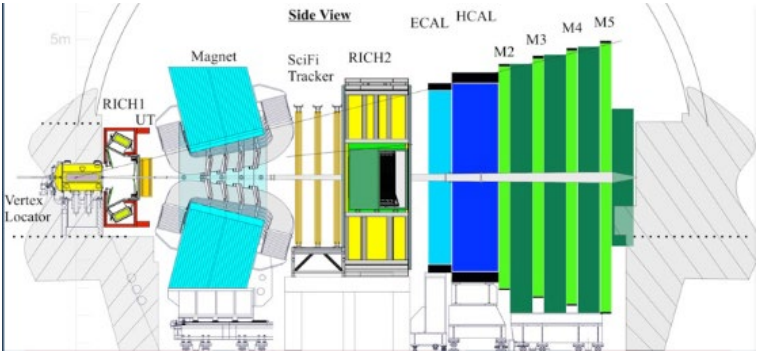


Future Upgrades of LHCb Muon System 27-28 June 2022

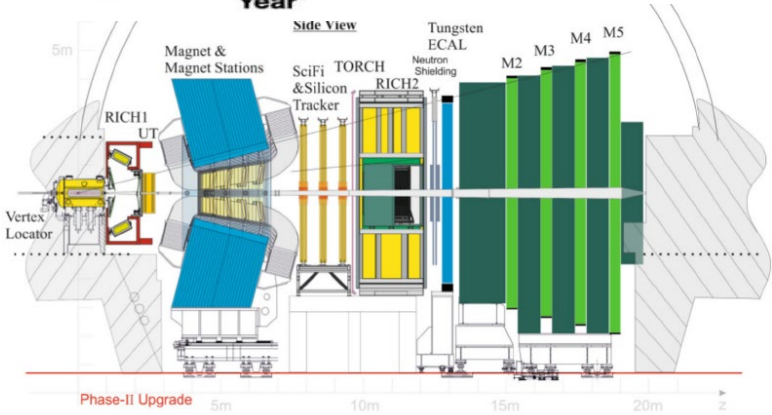


M. Poli Lener
On behalf of DDG – LNF - INFN

LHCb upgrade II (Run5 – Run6)



Current LHCb apparatus



Phase-2 upgrade apparatus

LHCb upgrade II (Run5 – Run6)

The Muon system (MWPC+GEM) during Run1 & Run2 ($1 \div 4 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$) exhibited tracking inefficiency, from dead time, at level of 1% in Run1 and 2% in Run2

Detector requirements Run5 – Run6

- Rate up to 1 MHz/cm² on detector single gap
- Rate up to 700 kHz per electronic channel
- Efficiency (station) > 95% within a BX (25 ns)
- Long stability up to 1C/cm² accumulated charge in 10 y of operation (M2R1, G=4000)
- Pad cluster size < 1.2

Rates (kHz/cm ²)	M2	M3	M4	M5
R1	749	431	158	134
R2	74	54	23	15
R3	10	6	4	3
R4	8	2	2	2

Area (m ²)	M2	M3	M4	M5
R1	0.9	1.0	1.2	1.4
R2	3.6	4.2	4.9	5.5
R3	14.4	16.8	19.3	22.2
R4	57.6	67.4	77.4	88.7

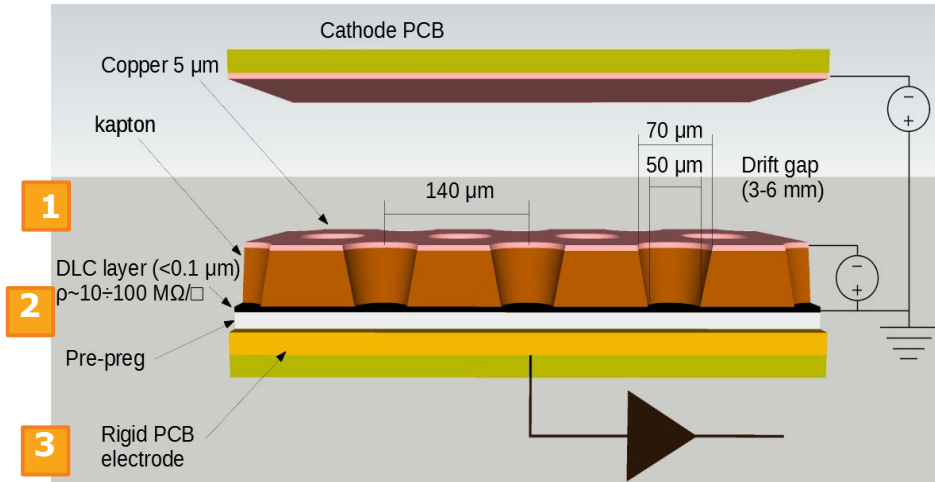
Detector size & quantity (4 gaps/chamber - redundancy)

- R1 ÷ R2: 576 gaps, size 30x25 to 74x31 cm², 90 m² det., 130 m² DLC
- R3: 768 gaps, size 120x25 to 149x31 cm², 290m² det.
- R4 : 3072 gaps, size 120x25 to 149x31 cm², 1164 m² det.

Proposed solution:
μ-RWELL technology

Under discussion the replacing of part of R3:
no problem with detector size (CLAS12- JLab Upgrade – 150x50 cm² uRWELL chambers)

The μ -RWELL



The μ -RWELL is a resistive MPGD composed of two elements:

- μ -RWELL_PCB
- Cathode

The μ RWELL_PCB is realized by coupling the resistive (grounded) amplification stage with the readout PCB through a thin prepreg foil.

Max DLC size: 50 x 200 cm² (limited by CERN-INFN DCL machine)

1 a WELL patterned kapton foil (with a Cu-layer on the top) acts as amplification stage

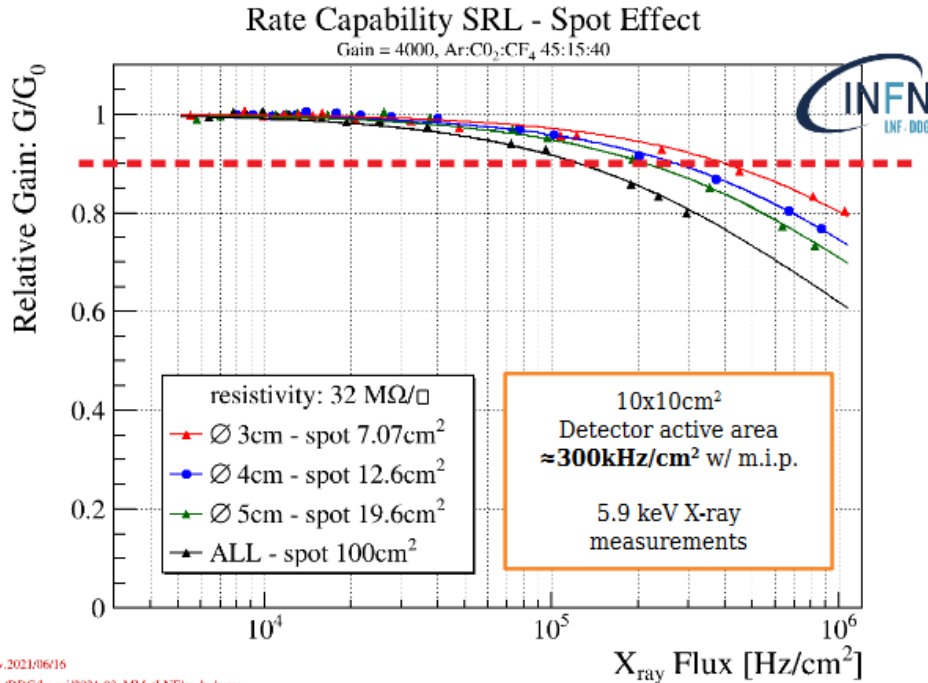
2 a resistive DLC layer^(*) (Diamond-Like-Carbon), with $\rho \sim 40 \div 100 \text{ M}\Omega/\square$

3 a standard readout PCB with pad segmentation

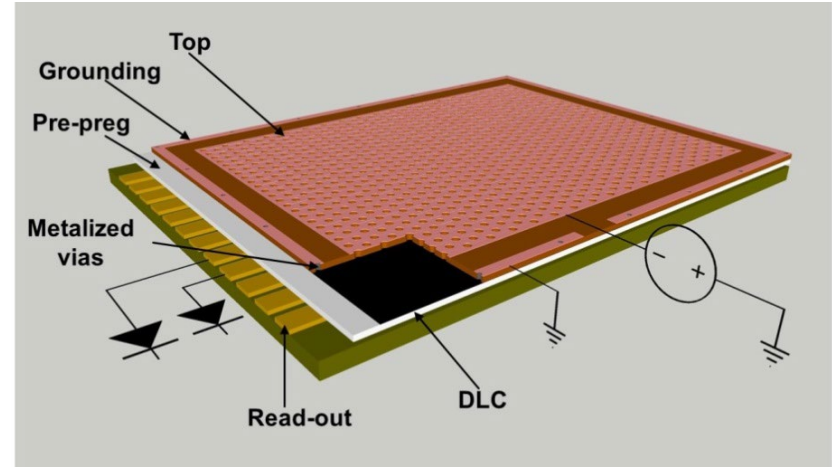
$$C = \epsilon_0 \times \epsilon_r \times \frac{S_{pad}}{t} \approx 72 \text{ pF} \times S(\text{cm}^2) \mid t \cong 0.05 \text{ mm}$$

^(*) DLC foils are currently provided by the Japan Company – BeSputter in future with DLC machine @ CERN

The low-rate layout



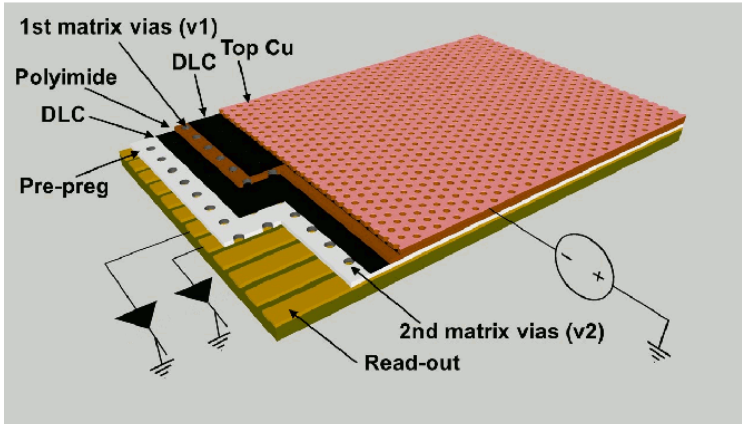
v.2021/06/16
~:DDG/lavori/2021-03_MMdetLNFRc_lr_barre



Single Resistive Layer (SRL)

- 2-D current evacuation scheme based on a single resistive layer
- grounding around the perimeter of the active area
- limitation for large area: the path of the current towards ground connection depends on the particle incidence point → detector response inhomogeneity → **limited rate capability <100 kHz/cm²**

High-rate layouts

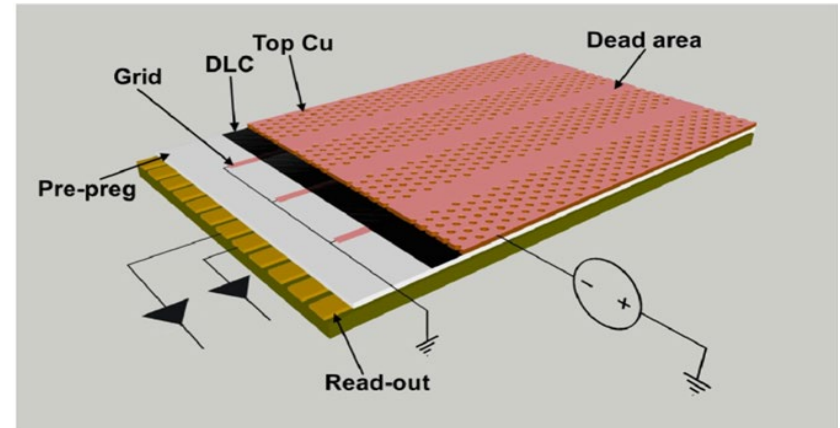


Double Resistive Layer

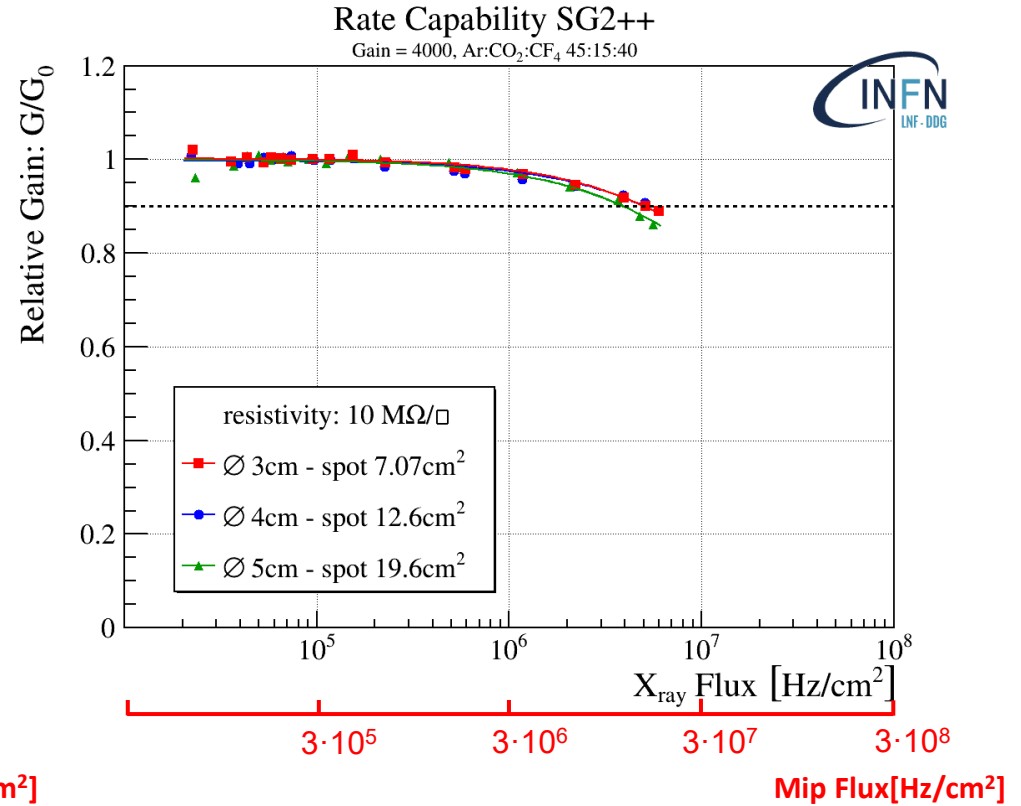
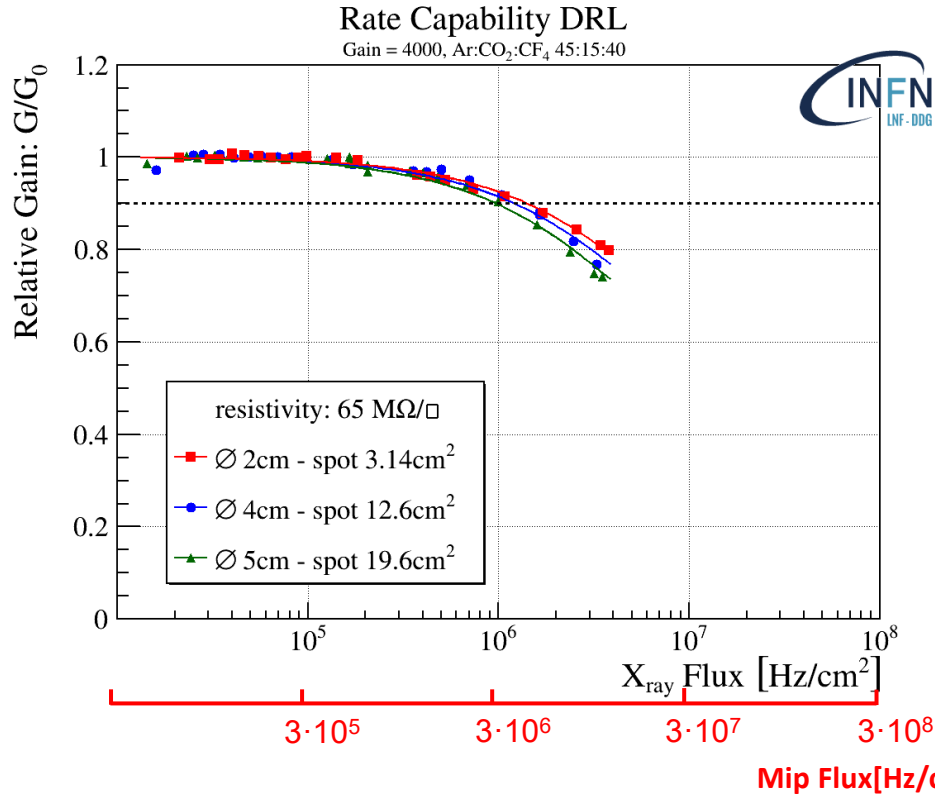
- 3-D current evacuation scheme
- two stacked resistive layers connected through a matrix of conductive vias
- Resistive stage grounding through a further matrix of vias to the underlying readout electrodes
- pitch of the vias with a density less than $1/\text{cm}^2$

The Silver Grid

- simplified HR scheme based on a SRL
- 2-D evacuation scheme by means a conductive grid realized on the DLC layer
- grid lines can be screen-printed or etched by photo-lithography
- pitch of the grid lines of the order of $1/\text{cm}$

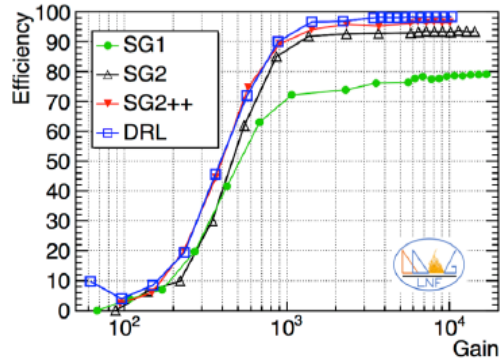
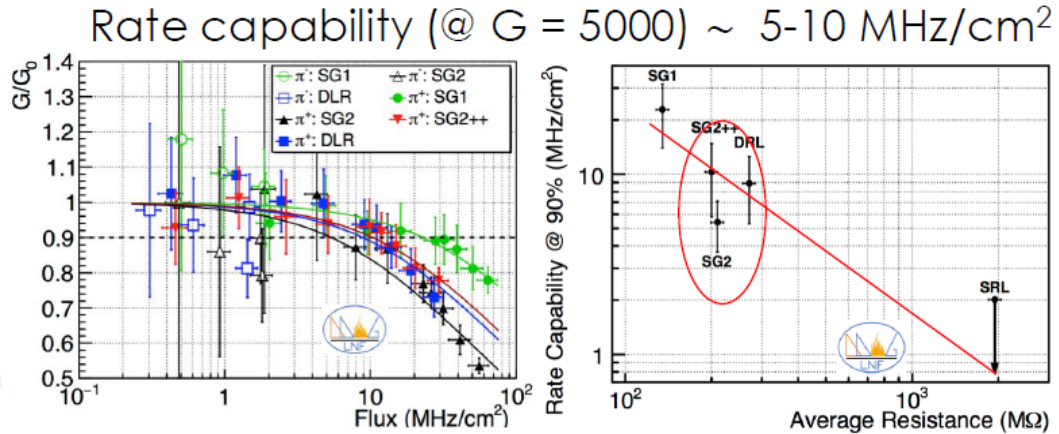
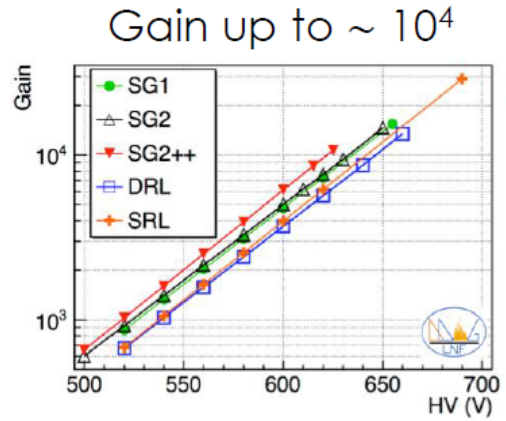


High-rate layouts: performance w/X-rays

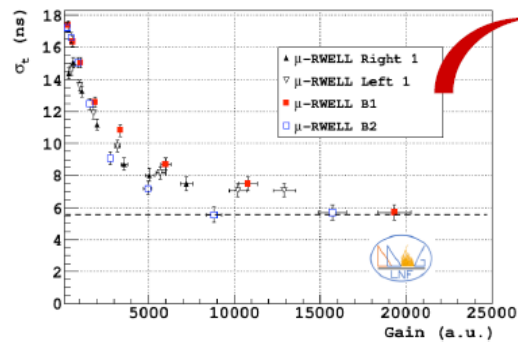


Rate capability w/m.i.p. ~ 3 times X-rays

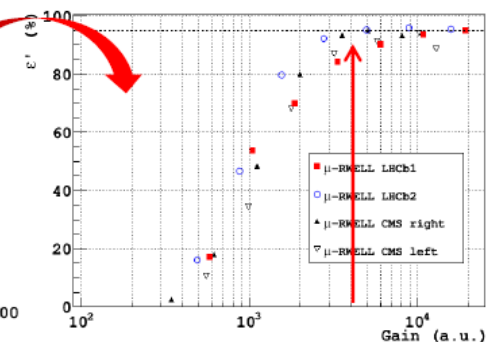
High-rate layouts: performance w/m.i.p.



Efficiency $\sim 98\%$



$\sigma_t \sim 5-6$ ns



Efficiency in 25 ns

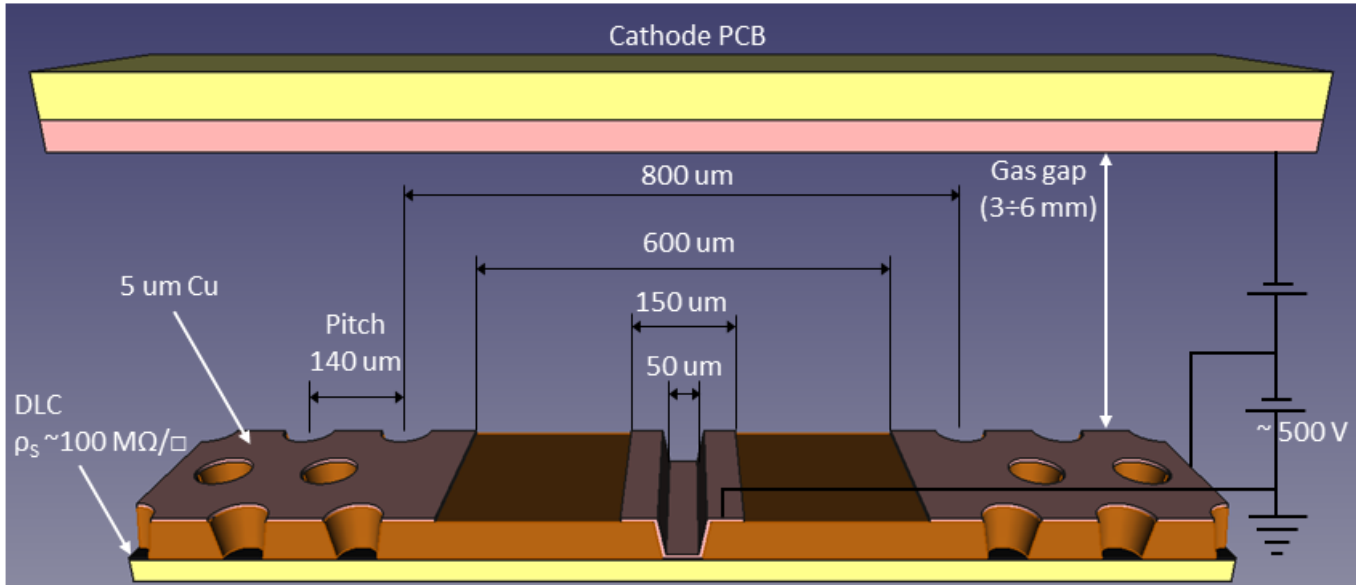
Limitations of DRL/SG layouts

Both **DRL** and **SG** show **very good performance**, but **some practical limitations**:

- both layouts require for **DLC+Cu sputtering technology**
- The **DRL** based on **double matrix of vias** require complex manufacturing
- The **SG** layout is more simple than **DRL**, **BUT** a bit **critical for the alignment** of the **conductive grid pattern on DLC** wrt the **amplification pattern on the top** (the well-pattern)

New layouts have been proposed in the last year in order to overcome such limitations, further simplifying the PCB manufacturing of the HR layouts.

The new PEP HR layout

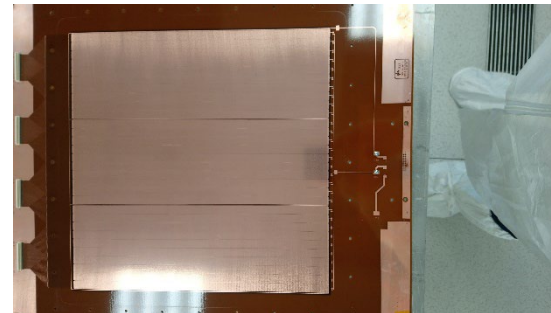


Layout	GND pitch [mm]	Dead Area [mm]	DOCA [mm]	Geom. Acceptance
PEP1	6 // 8	1	0.475	66%
PEP2.1	8.9	0.8	0.375	91%
PEP2.2	17.8	0.8	0.375	95.5%

DOCA (Distance of Closest Approach): minimum distance between a grounding line and an amplification channel

PEP: Patterning – Etching – Plating

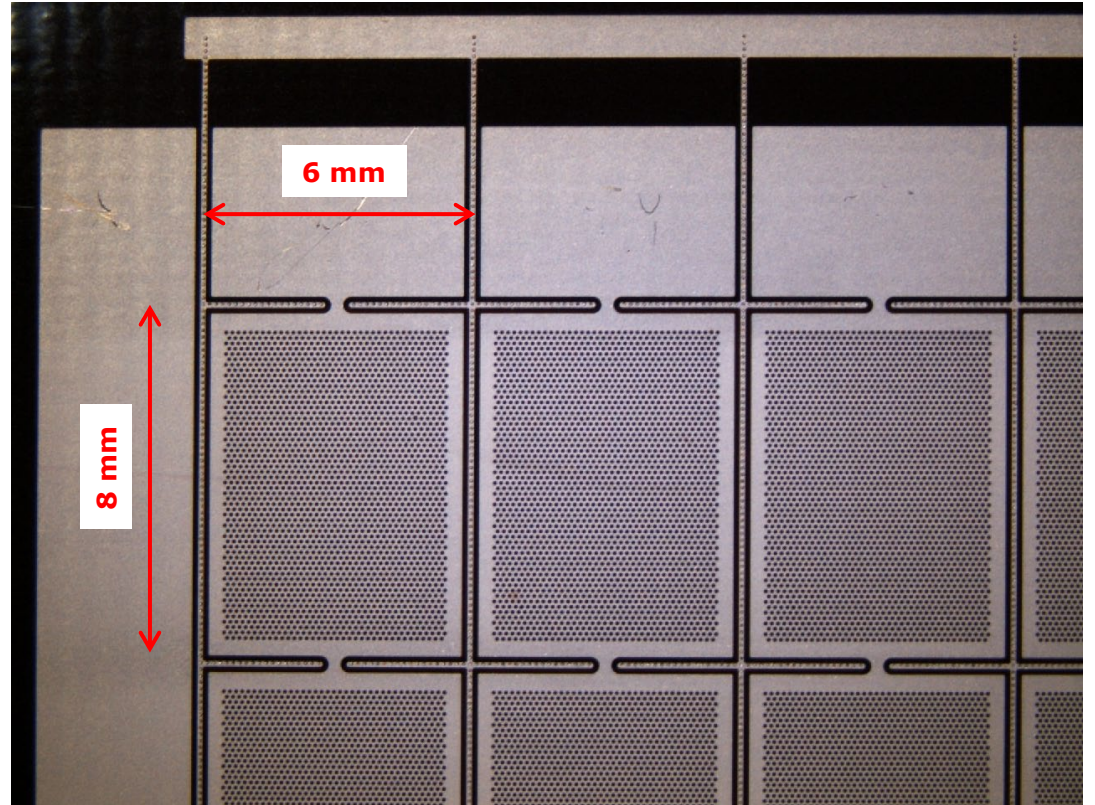
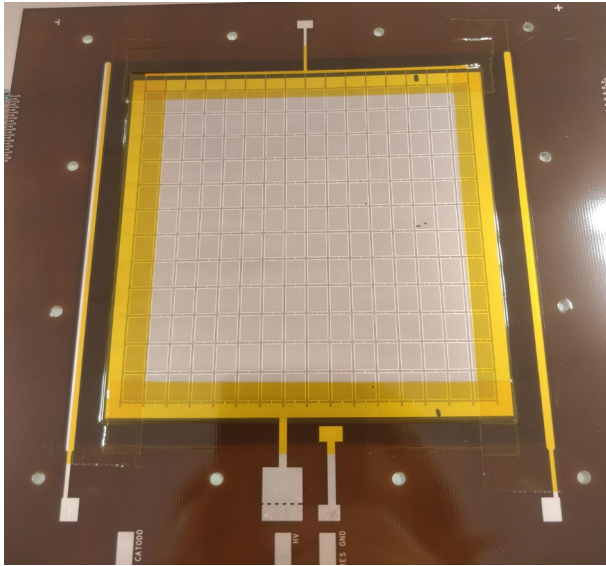
- Single DLC layer
- Grounding from top by kapton etching and plating
- No alignment problems
- **Scalable to large size**



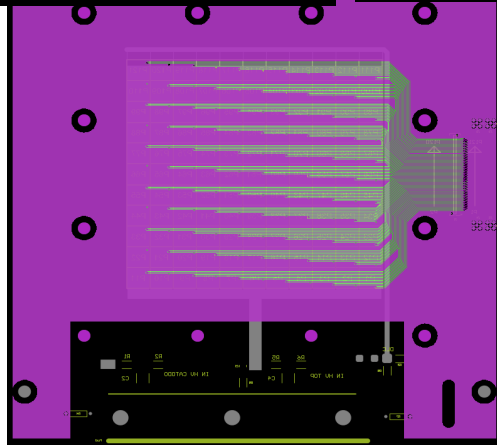
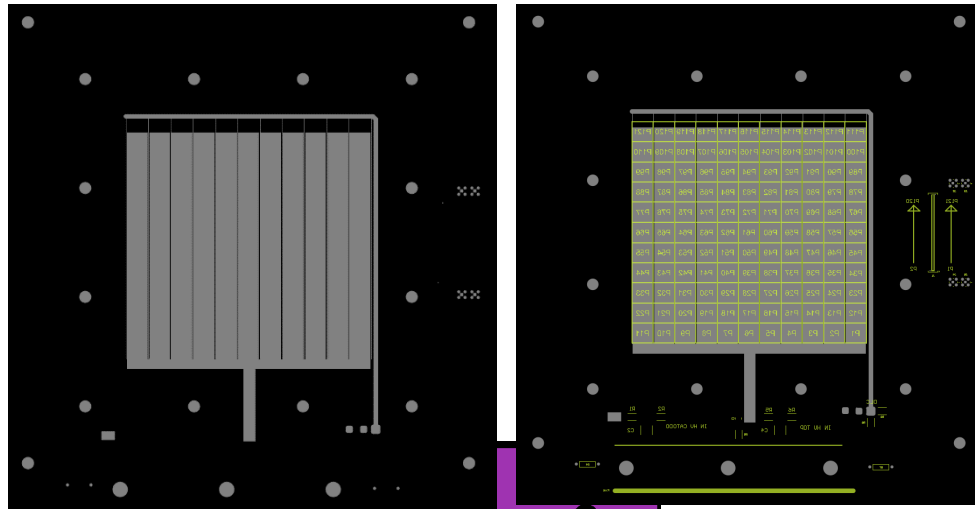
ACTIVE AREA 30 x 30 cm²

PEP-1 layout

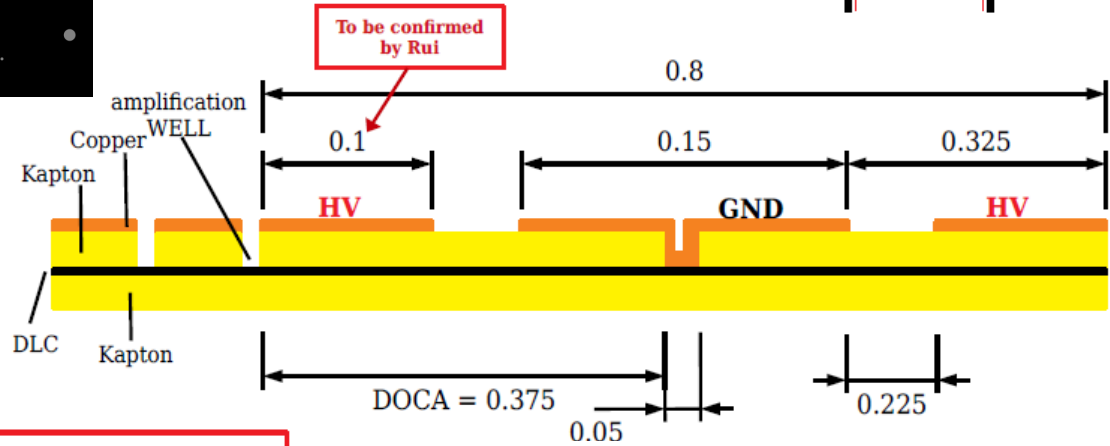
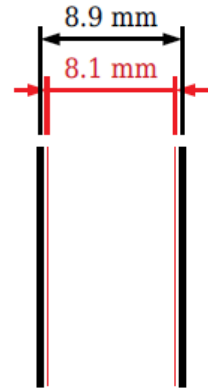
A first high rate PEP prototype, developed for LHCb, has been realized and it has been extensively tested (layout optimization in progress)



PEP-2 layout (geometry optimization)

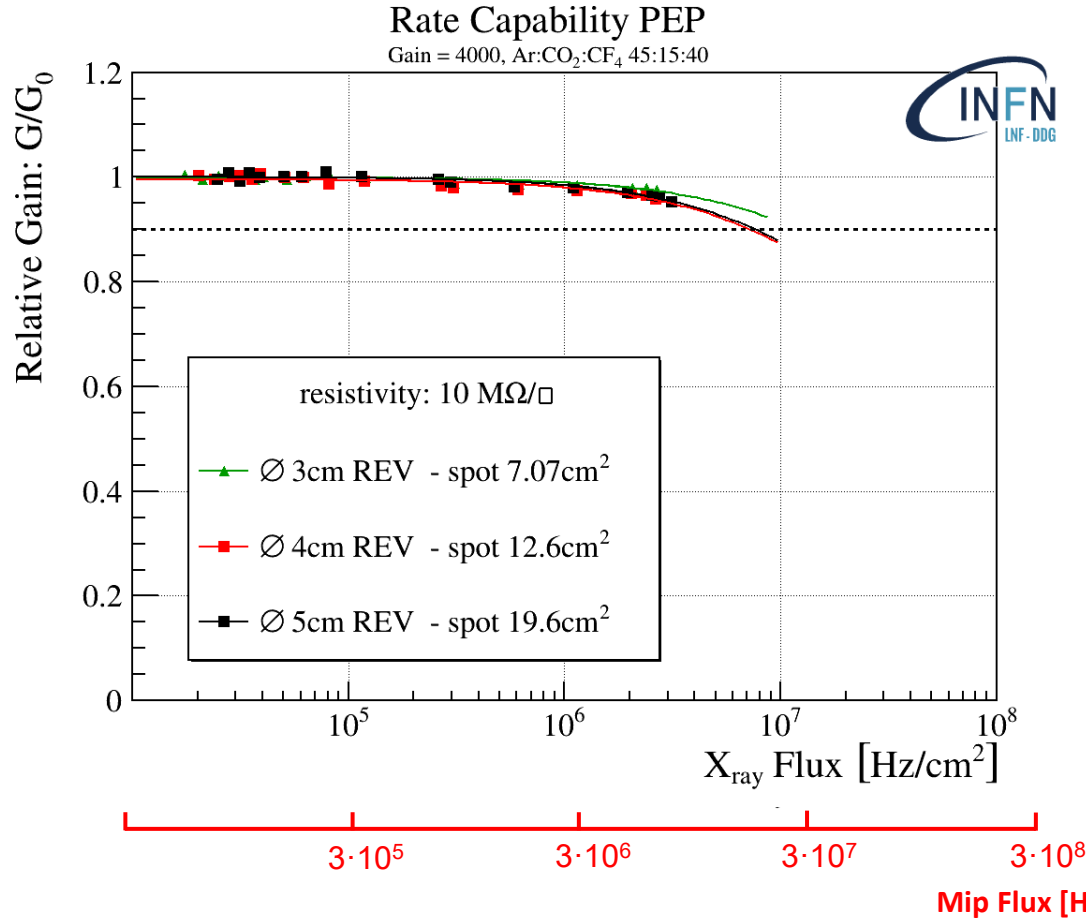


Unitary cell **dead zone**:
 $1 - (8.9 - 0.8) / 8.9 = 0.089 \rightarrow 9\%$



NOT IN SCALE,
 values given in mm

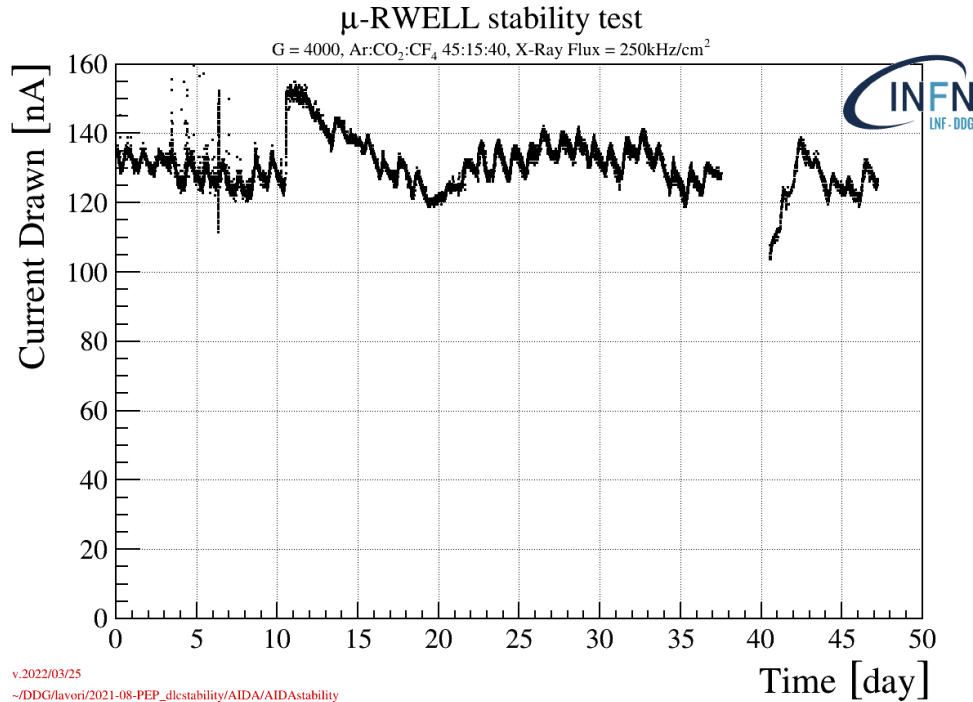
The PEP performance



Rate capability defined as the rate where a 10% of gain drop is observed.
It shouldn't affect the detection efficiency once chosen a working point **well above the efficiency knee**

The rate capability has been measured by irradiating the detector with **5.9 X-ray** with **Pb collimators** with different spot size. **The diameter of collimators was larger than the DLC ground pitch.** $\text{RC}_{\text{mip}} > 10 \text{ MHz}/\text{cm}^2$.

PEP-1 layout performance

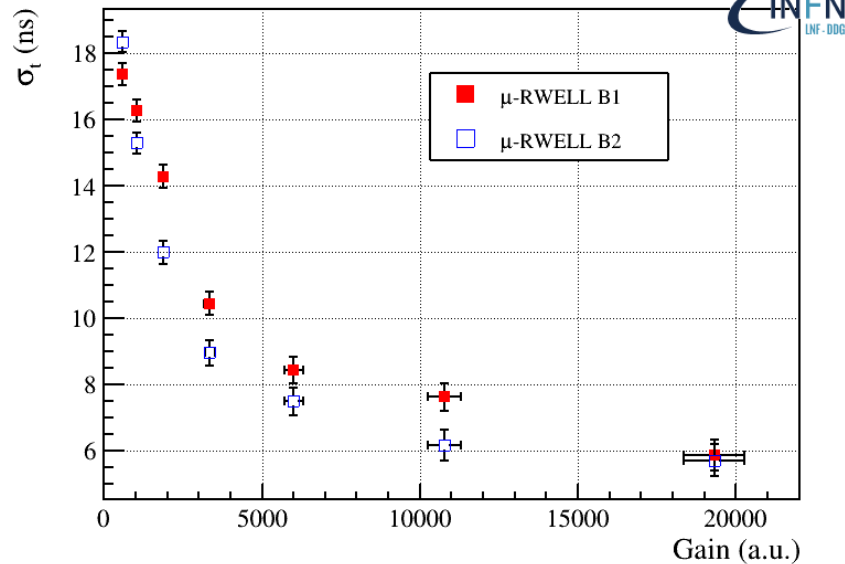


A long-term X-ray irradiation is on-going: the current of the detector electrodes (I_{top} , I_{cat}) as well as ambient parameters (T , P , RH) are constantly monitored.
 $Q_{int.} \sim 100\text{mC}$ over all the test period (irradiated area= 20 cm²).

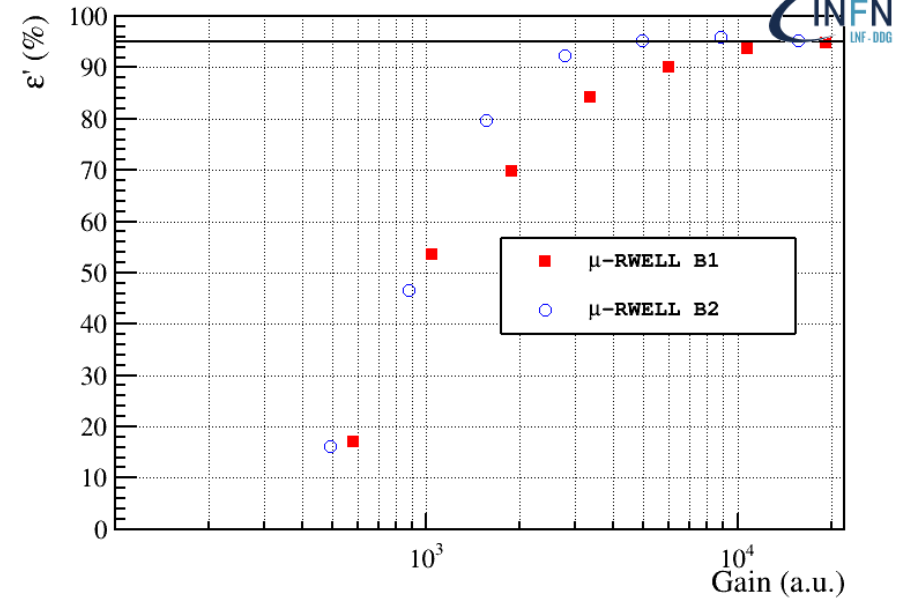
Because of the common effort in the scientific community to reduce the F-based components, we are changing the gas mixture to Ar:CO₂:iC₄H₁₀ 68:30:2 and starting the stability measurement

Time performance (old measurement)

μ -RWELLS time resolution vs gain



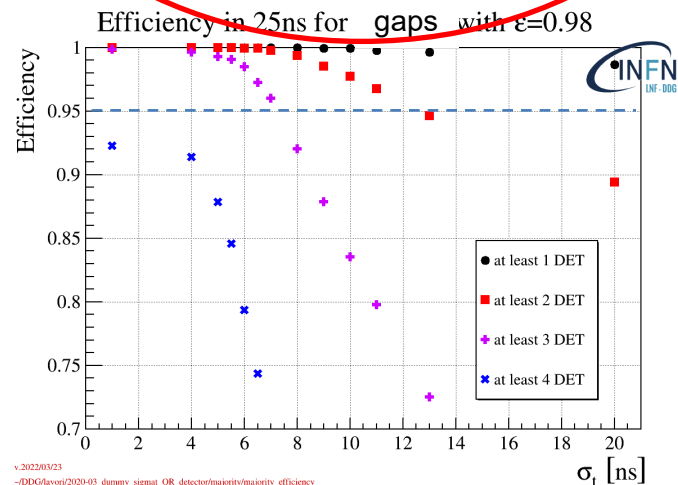
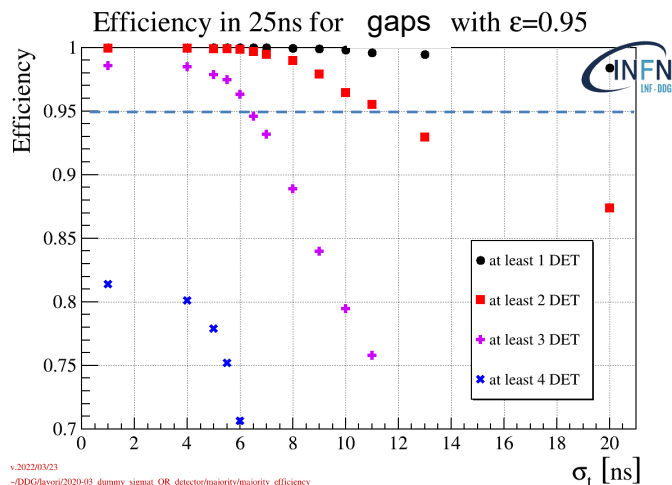
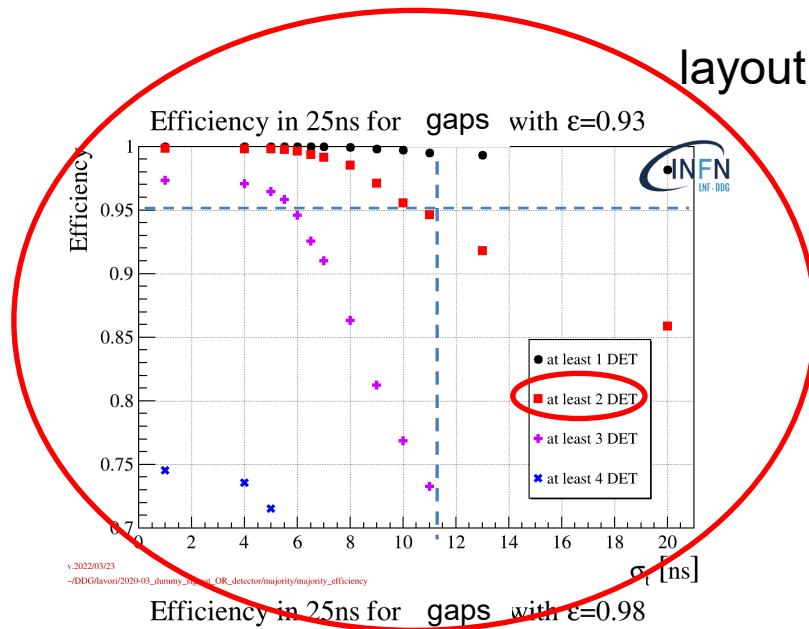
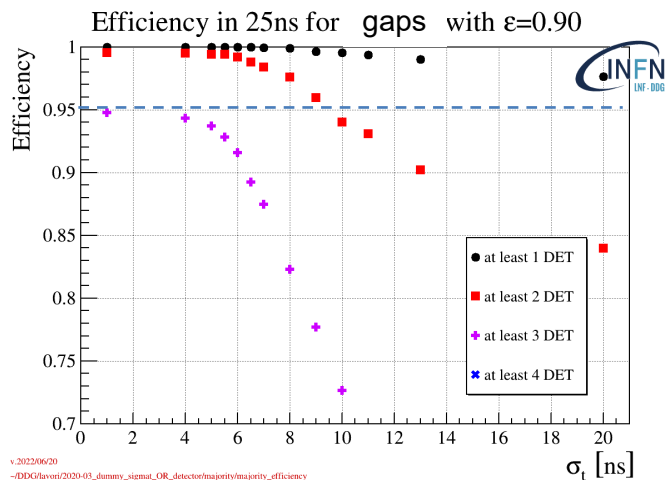
Efficiency in 25 ns



- A first measurement of the time resolution has been done at H8C CERN - NA
- The detectors were operated with **Ar:CO₂:CF₄ 45:15:40** gas mixture (the same used by GEM @LHCb) and equipped with **VFAT2**. A saturation due to FEE is visible at high gain
- There is room to improve the resolution, improving the FEE

Time performance (simulation)

layout PEP



2022 plans

- **9/2022** – delivery **10x10 cm² PEP2.1-RWELL** pad layout (LNF)
- **11/2022** – assembly, characterization w/X-ray, **long-term test w/Xrays** (LNF)
- **11-12/2022** – **FATIC integration & preliminary test w/cosmics** (Bari + LNF)
- **7/2022** – meeting for **eco-gas mix** with CERN – Gas group (B. Mandelli)
- **> 2022** – start **eco-gas mix search/test**

2023 tentative plans

- Test Beam of **10x10 cm² PEP2.1-RWELL** pad layout (LNF + Bari) – Ottobre 2023
- Design/production of the **M2R1 (20x25cm²) PEP-RWELL** pad layout following results on 10x10 cm² (LNF)
- **Electronics ...** (Bari)
- **GIF++**

Open R&D

Gas related R&D:

- **CF4 is not an eco-gas, responsible of strong kapton etching** observed on GEM detectors (*STUDY OF ETCHING EFFECTS ON TRIPLE-GEM DETECTORS OPERATED WITH CF₄-BASED GAS MIXTURES*, M. Alfonsi et al., *IEEE Trans.Nucl.Sci.52 (2005) 2872-2878.*)
- F⁻ (responsible of kapton etching) is produced with any small CF4 concentration (Studies on fluorine-based impurity production in Triple-GEM detectors operated with C-based gas mixture, B. Mandelli et al., *NIM A 1004 (2021) 165373.*)
- **Old GEM detectors at LHCb will be analysed** to check for **CF4 etching effects** (we can learn from this study)
- **PEP μ-RWELL** irradiated with X-Rays at LNF will be **analysed to check for possible CF4 etching effects**
- **Eco-gas mix for RWELL: looking for collaboration** (Gas – CERN group will provide support for gas analysis)
- **Long-term test of a PEP μ-RWELL will be started soon with Ar/Co2 gas mix** (no CF4): X-Rays (LNF) & GIF++ (looking for collaboration)

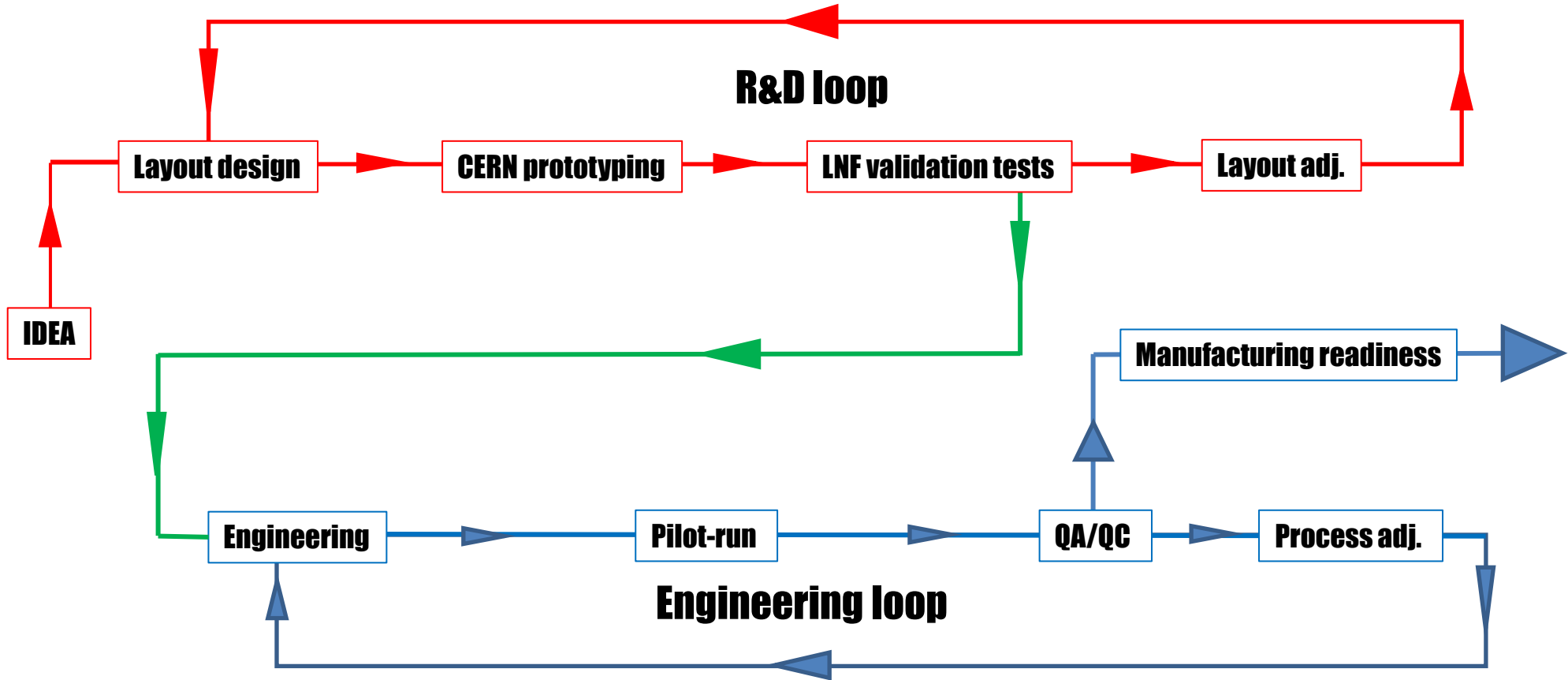
Mechanics related R&D:

- **Defining a safe assembly/testing procedure: DI-washing+electrical hot-cleaning, humidity control in the gas line, detector conditioning** (in strict collaboration with Rui)
- **Replacing FR4 frames with PEEK frames**, more expensive BUT not hygroscopic and then compatible with CF4 (eventually only in closed mode)

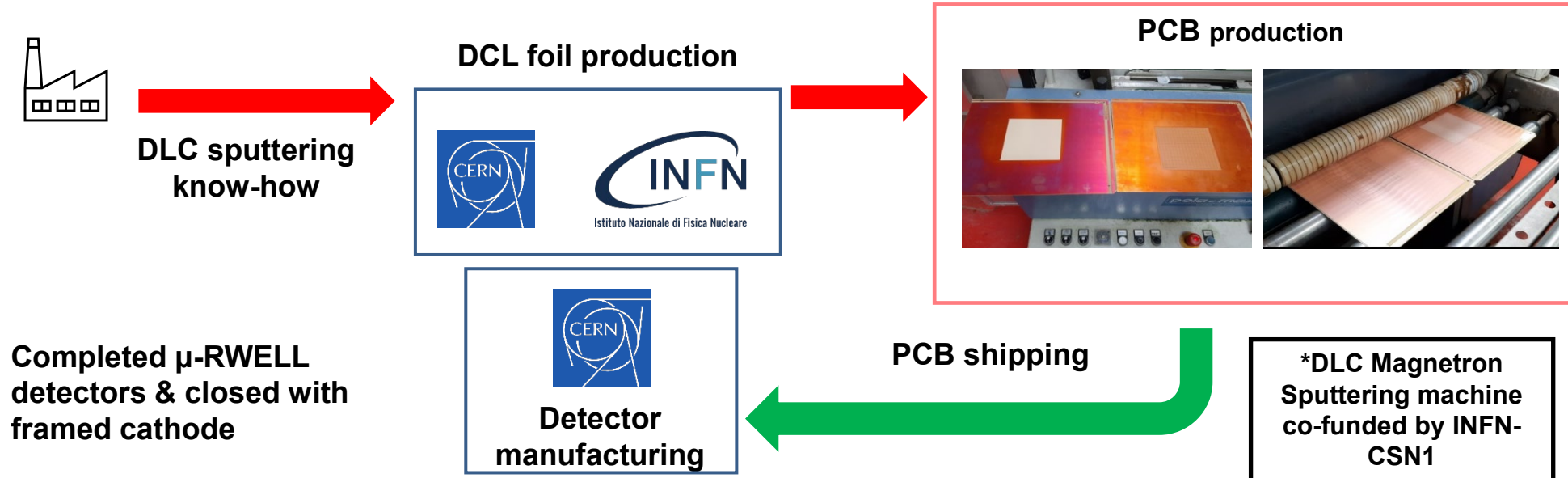
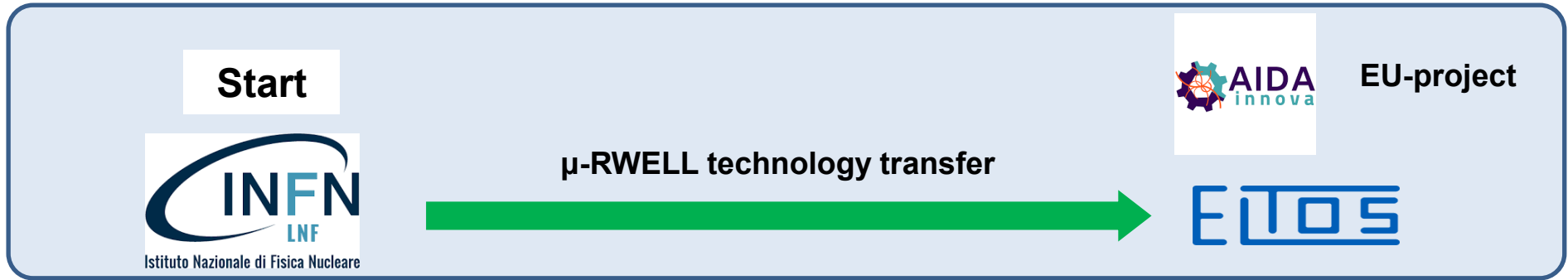
Electronics & detector design:

- **FATIC design and integration with detector**
- **Detector layout optimization (FEE & HV connectors, gas pipe, ect)**

The road-map: R&D + Engineering



Technology transfer



Manufacturing steps

Step 0 - CERN_INFN DLC sputtering machine @ CERN

- bid concluded
- delivery foreseen end of July 2022 – operational within end of 2022

Step 1 - producing PCB readout for μ -RWELL (pad/strip readout) @ ELTOS

- with top patterned (pad/strip side)
- without patterning bottom layer (connector side)

Step 2 - DLC patterning → two options under investigation:

- photo-resist ⊕ patterning with BRUSHING-machine (ELTOS)
- photo-resist ⊕ patterning with JET-SCRUBBING-machine (CERN)

Step 3 - DLC foil gluing on PCB → three options under investigation:

- double 106-prepreg, $\sim 2 \times 50 \mu\text{m}$ thick (by ELTOS - before 2021)
- PCB planarizing w/early-stripping of suitable prepreg (115°C/15min) ⊕ single 106-prepreg (by CERN)
- PCB planarizing w/gap filling with epoxy Taiyo THP-100DX1 VF (screen printing) ⊕ single 106-prepreg (by ELTOS - NOW)

Step 4 - Top copper patterning for successive kapton etching to create evacuation vias (by CERN and/or ELTOS)

Step 5 - Amplification stage patterning: kapton etching ⊕ plating ⊕ ampl-holes (by CERN)

Tests in ELTOS (I)

DLC patterning

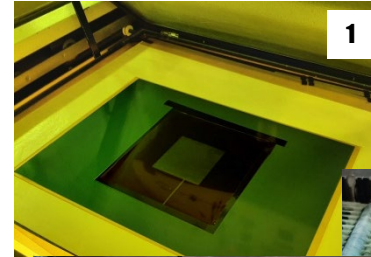
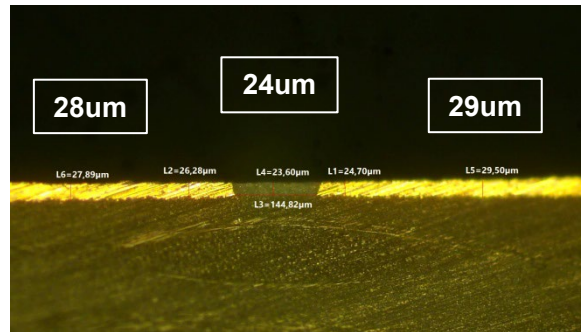
- **photo-resist** application/developing ⊕ **patterning with brushing-machine**
- while at CERN a different approach, based on a **JET-SCRUBBING-machine**, is implemented

PCB planarizing

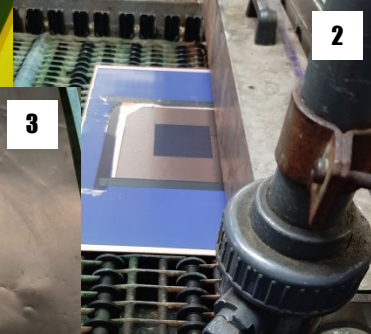
- **PCB planarizing** by filling the gap between pads with epoxy resin **Taiyo THP-100DX1 VF** (screen printing) ⊕ **PEM planarizer (POLA&MASSA)**
- While at CERN a **PCB planarizing w/early-stripping** of suitable prepreg (115°C/15min)

gap filling
pad

24 um
29 um



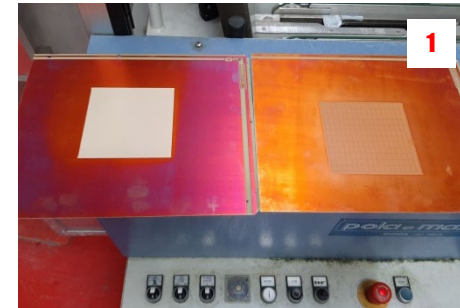
1



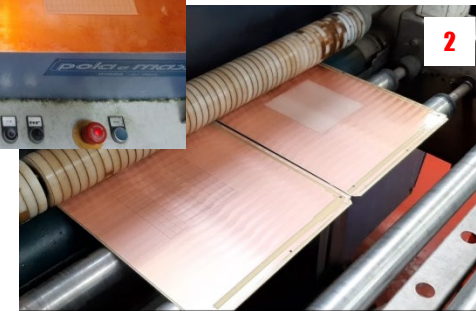
2



3



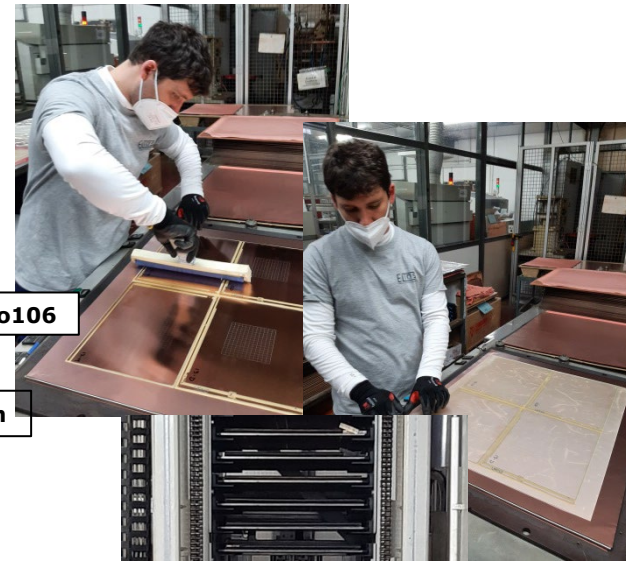
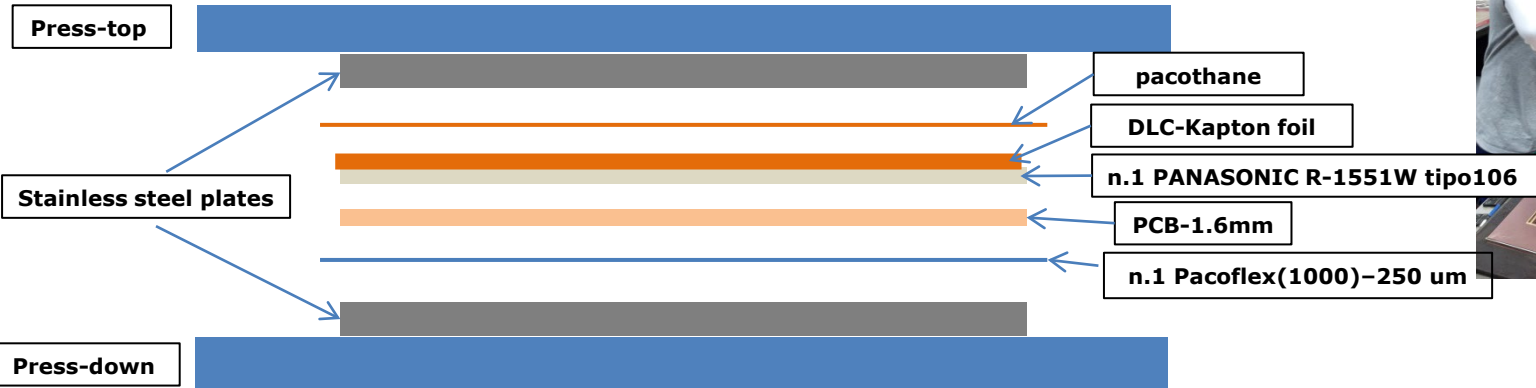
1



2

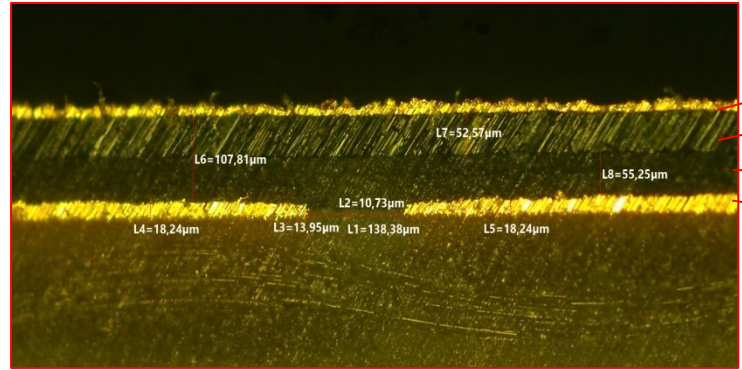
Tests in ELTOS (II)

DLCed Kapton foil gluing on PCB w/pressing machine



Main parameters:

- pressure 180 N/cm²
- temperature 210°C



- 5 um Cu
- 50 um Kapton
- 55 um 1xpreg-106
- 18 um Cu readout



Good uniformity & DLC-readout distance close to CERN stackout

Tentative schedule μ -RWELL in LHCb (un solo «integration group»)

	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	
	RUN3				LS3				RUN4				LS4		
new HR layout design & test (w/X-ray)															
eco-gas searches															
test beam with PEP-RWELL with FATIC															
global irradiation test (GIF++)															
finalizing design HR layout															
proto-0 construction & test															
TDR															
preparation mass production (ELTOS+ CERN)															
DLC production w/CID															
R1 - Production (ELTOS + Rui)															
R1 - integration & test (INFN)															
R2-M2/M3 - production(ELTOS+Rui)															
R2-M2/M3 - integration & test (INFN)															
R2-M4/M5 - production(ELTOS+Rui)															
R2-M4/M5 - integration & test (INFN)															
Installation/commissioning															

La costruzione segue i seguenti step(*):

- CERN → produzione DLC con macchina sputtering di cui INFN è co-proprietario (costo materie prime e missione personale INFN) consegna prevista fine luglio 2022 – in operazione inizio 2023
- Eltos → PCB, DLC patterning & gluing
- CERN → finalizzazione rivelatore con etching kapton (RUI)
- CERN → assemblaggio con frame e catodi e procedura di conditioning (RUI)
- CERN → test finale rivelatori e integrazione elettronica (personale INFN)

(*) tempi e modalità di produzione definite con Rui & Eltos e considerando un solo «integration group»



L3=85,65μm

L1=83,76μm

Spare Slides

L2=88,87μm

LHCB upgrade II (Run5 – Run6)

Aggiornamento Tabella (dimensioni pad, rate, ecc)

Capacità x2 (t=0.05mm)

	#cmb/region	cmb X (cm)	cmb Y (cm)	cmb Area cm	pad0 X (cm)	scale fact X	pad X (cm)	pad0 Y (cm)	scale fact Y	pad Y (cm)	pad Area (cm2)	max rate (kHz/cm)	rate/pad (kHz)	C (pF)	Nch/gap	Nch/4gap
M2R1	12	30	25	750	0.63	0.70	0.90	3.1	3.50	0.89	0.80	3300	2630.00	28.22	940	3760.00
M2R2	24	60	25	1500	1.25	1.40	0.89	6.3	3.50	1.80	1.61	300	482	56.89	933	3732.00
M3R1	12	32	27	864	0.67	0.70	0.96	3.4	3.50	0.97	0.93	1900	1766.00	32.91	929	3716.00
M3R2	24	65	27	1755	1.35	1.40	0.96	6.8	3.50	1.94	1.87	220	412	66.32	936	3744.00
M4R1	12	35	29	1015	2.9	2.80	1.04	3.6	3.50	1.03	1.07	650	692.00	37.71	952	3808.00
M4R2	24	70	29	2030	5.8	5.60	1.04	7.3	3.50	2.09	2.16	85	183	76.47	939	3756.00
M5R1	12	37	31	1147	3.1	2.80	1.11	3.9	3.50	1.11	1.23	550	678.00	43.67	929	3716.00
M5R2	24	74	31	2294	6.2	5.60	1.11	7.7	3.50	2.20	2.44	55	133	86.22	941	3764.00

Detector size & quantity (4 gaps/chamber - redundancy)

- R1÷R2: 576 detectors, size 30x25 to 74x31 cm², 90 m² det. - 130 m² DLC
- R3: 768 detectors, size 120x25 to 149x31 cm², 290m² det. - 414 m² DLC
- R4 : 3072 detectors, size 120x25 to 149x31 cm², 1164 m² det. - 1662 m² DLC

LHCb upgrade II (Run5 – Run6)

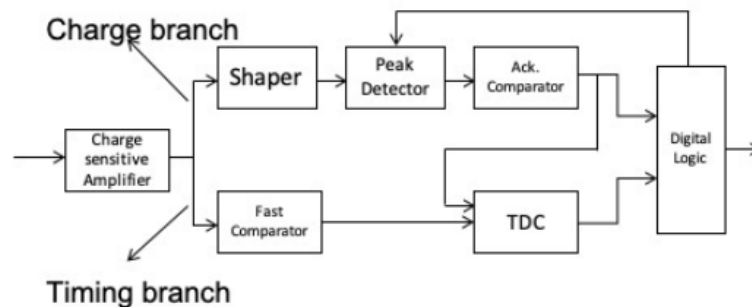
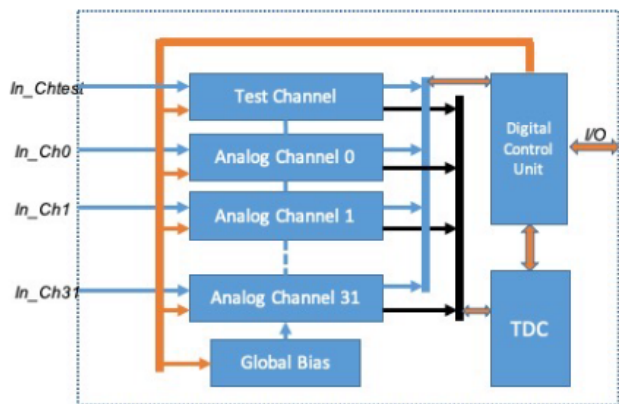
Aggiornamento Tabella (dimensioni pad, rate, ecc)

Capacità x2 (t=0.05mm)

	#cmb/region	cmb X (cm)	cmb Y (cm)	cmb Area cm	pad0 X (cm)	scale fact X	pad X (cm)	pad0 Y (cm)	scale fact Y	pad Y (cm)	pad Area (cm2)	max rate (kHz/cm2)	rate/pad (kHz)	C (pF)	Nch/gap
M2R1	12	30	25	750	0.63	1.00	0.63	3.1	5.00	0.62	0.39	3300	1288	13.82724	1920
M2R2	24	60	25	1500	1.25	2.00	0.63	6.3	5	1.26	0.79	300	236	27.8775	1904
M2R3	48	120	25	3000	2.5	2.00	1.25	12.5	5	2.5	3.13	35	109	110.625	960
M2R4	192	120	25	3000	5	1.00	5.00	25	1	25	125.00	20	2500	4425	24
M3R1	12	32	27	864	0.67	1.00	0.67	3.4	5.00	0.68	0.46	1900	865	16.12824	1896
M3R2	24	65	27	1755	1.35	2.00	0.68	6.8	5	1.36	0.92	220	201	32.4972	1911
M3R3	48	130	27	3510	2.7	2.00	1.35	13.5	5	2.7	3.65	19	69	129.033	962
M3R4	192	130	27	3510	5.4	1.00	5.40	27	1	27	145.80	5	729	5161.32	24
M4R1	12	35	29	1015	2.9	4.00	0.73	3.6	5.00	0.72	0.52	650	339	18.4788	1944
M4R2	24	70	29	2030	5.8	8.00	0.73	7.3	5	1.46	1.06	85	89	37.4709	1917
M4R3	48	139	29	4031	11.6	7.00	1.66	14.5	5	2.9	4.81	9	43	170.1222857	838
M4R4	192	139	29	4031	23.1	1.00	23.10	29	1.00	29	669.90	3	2009	23714.46	6
M5R1	12	37	31	1147	3.1	4.00	0.78	3.9	5.00	0.78	0.60	550	332	21.3993	1897
M5R2	24	74	31	2294	6.2	8.00	0.78	7.7	5	1.54	1.19	55	65	42.2499	1922
M5R3	48	149	31	4619	12.4	7.00	1.77	15.5	5	3.1	5.49	7	38	194.3965714	841
M5R4	192	149	31	4619	24.8	1.00	24.80	30.9	1.00	30.9	766.32	4	3065	27127.728	6

Capacità /2 (riduzione dimensione PAD)

FATIC ASIC (New Development)



Analog Section:

- 32 Front-end channels:
 - Fast output: designed for timing measurements
 - Slow output: input signal acknowledgement and charge measurement
 - Global Bias: temperature and power supply independent, internal calibration, bias monitoring

Digital Section:

- Control Unit:
 - 320 MHz SLVS I/O link
 - Channel & Global bias adj. bits
 - TDC control

CSA settings:

- Input signal polarity: positive & negative
- Gain: High $\approx 50\text{mV/fC}$, Low $\approx 10\text{ mV/fC}$
- Recovery time: adjustable

Shaper settings:

- Peaking time: 25ns, 50ns, 75ns, 100ns (polarity adj)

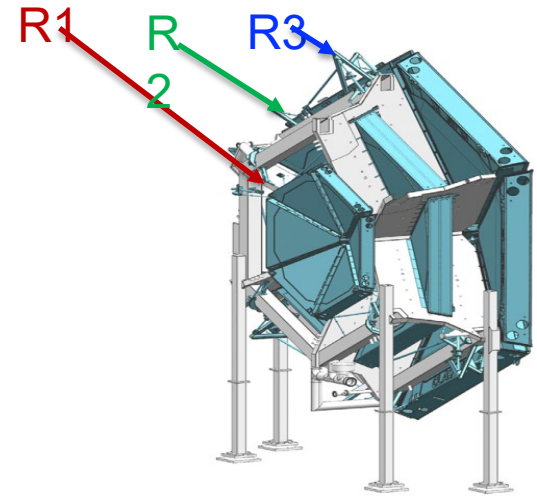
TDC resolution:

- 100ps (5 bits fine + 16 bits coarse)

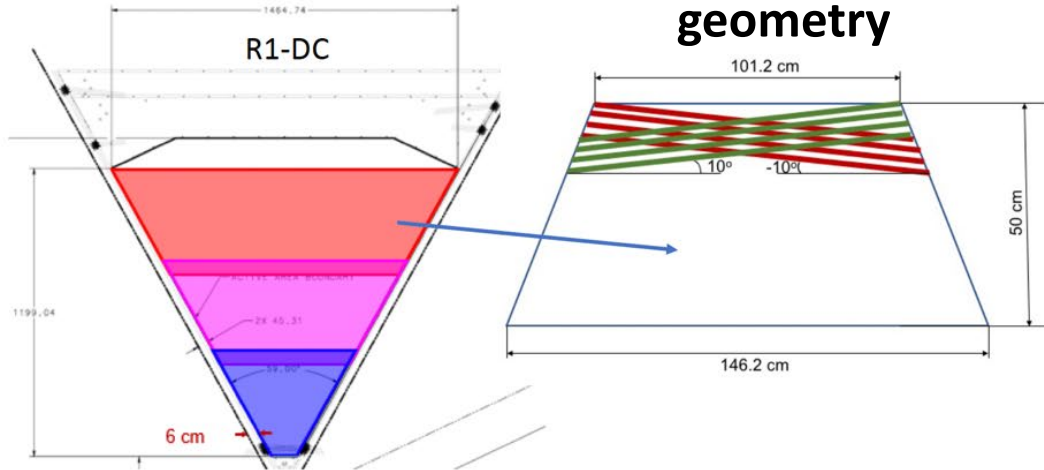
Cdet < 200 pF

Clas12 upgrade @ JLAB

- Replace tracking planes in **DC R1** with **MPGD** tracker
- **DC chambers in R1** are made of **2 superlayers**, of **6 layers** each, and should be replaced with **6 layers of 2D μ – RWELL**
- **Requirements**
 - Tracking resolution: $100 \mu\text{m}$
 - Timing resolution: 10 ns
 - Rate: 100 KHz/cm^2
 -



R1 – detector geometry



- The largest segment is a trapezoid with a large base of 146.2 cm, the height of the chamber will be 50 cm, the small base of 101.2 cm
- The readout concept is U-V strips with $\pm 10^\circ$ stereo angles relative to the base of the trapezoid, strips traced on two sides of the readout plane will be used.
- The charge share will be through capacitive coupling. The pitch size of the readout 0.8 mm, the strip width 0.4 mm.
- The total number of U&V readout strips is about 685.

Operative meetings

21 Sept. 2021 - joint INFN-ELTOS-CERN meeting

- **standardizing manufacturing procedures of μ -RWELL layout**

1-3 Dec. 2021 - CERN-INFN meeting

- **status of the R&D on the High Rate layout**
- **measurement with high intensity X-ray beam**
- **2D layout based on the readout of a segmented amplification stage**

7-10 Dec. 2021 – 1st test batch in ELTOS

- **DLC patterning**
- **PCB planarizing tests**

7-8 Mar. 2022 - 2nd test batch in ELTOS

- **PCB planarizing tests**
- **Kapton DLCed foil coupling with PCB-readout**

28 Mar. 2022 - joint INFN-ELTOS-CERN meeting

- **discussion with Rui about the results obtained**

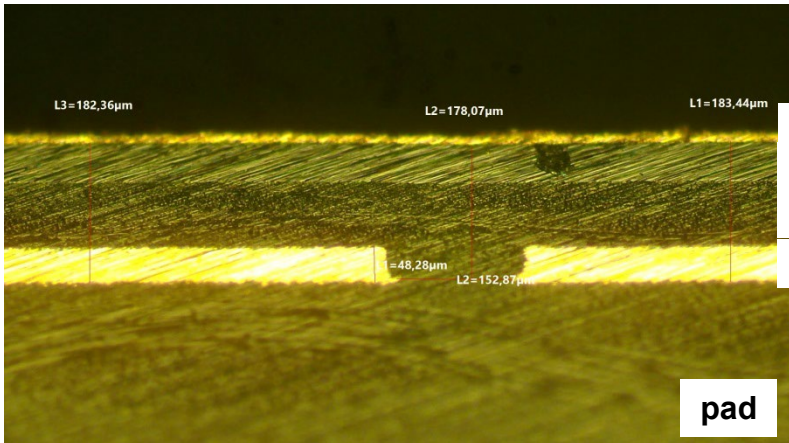
Starting point (2017-2020): ELTOS vs CERN

DLCed Kapton foil gluing on PCB

The **coupling/gluing** is performed through a **106-prepreg foil**. Main requirements:

- **good planarity**
- **minimizing the DLC-readout distance** (to maximize the signal amplitude):
 - preliminary **PCB planarizing at CERN + prepreg-106**
 - different approach implemented in the past in **ELTOS** with a **double prepreg-106**

Standard ELTOS stacking

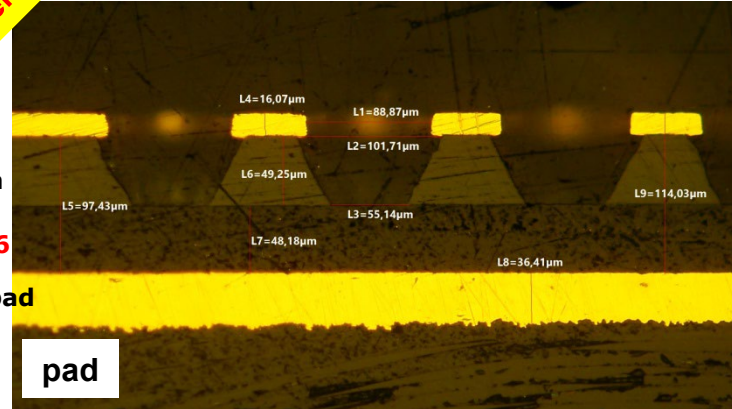


to be optimized

5 um Cu
50 um Kapton
80 um 2xprepreg-106
48 um Cu readout

Standard CERN stacking

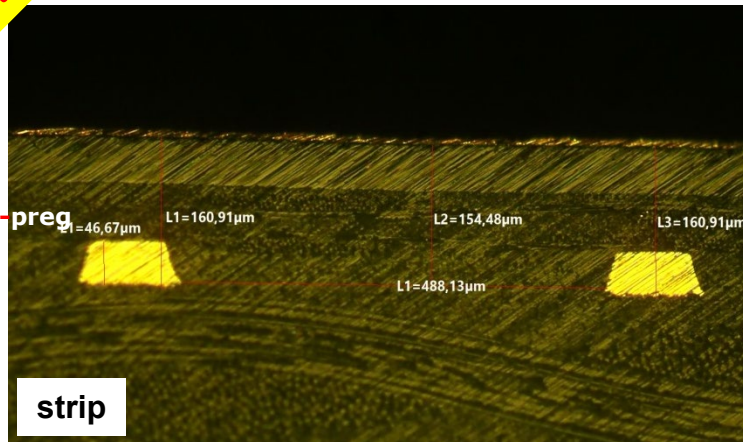
reference



16 um Cu
50 um Kapton
48 um 1xprepreg-106
36 um Cu readout pad

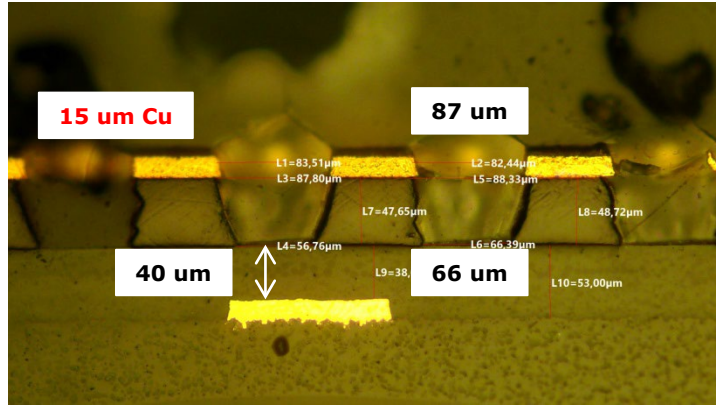
Standard ELTOS stacking

almost OK

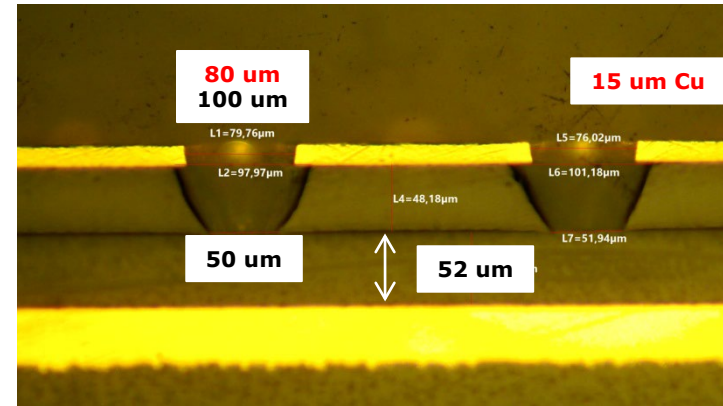


5 um Cu
50 um
58 um 2xprepreg
47 um Cu

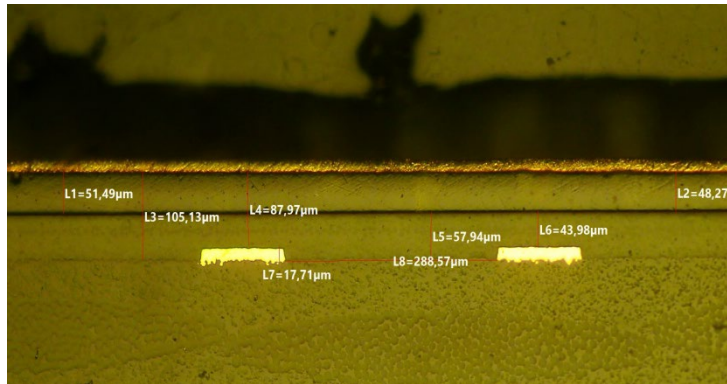
Low-rate (RDFCC) vs PEP -1 (LHCb)



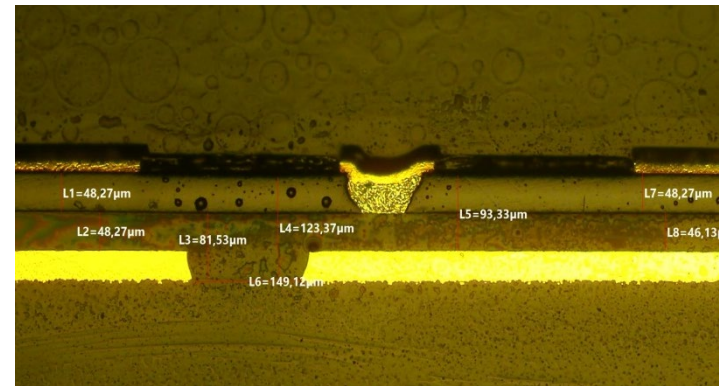
RDFCC Low-rate Ampl. Hole (CERN)



PEP - 1 Ampl. Hole (CERN)

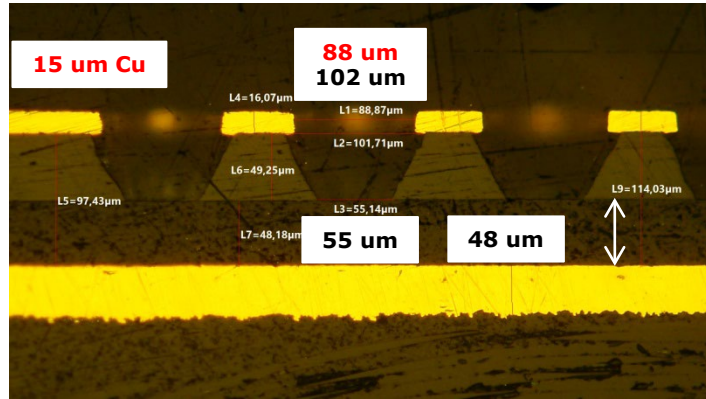


RDFCC Low-rate stackout (CERN)

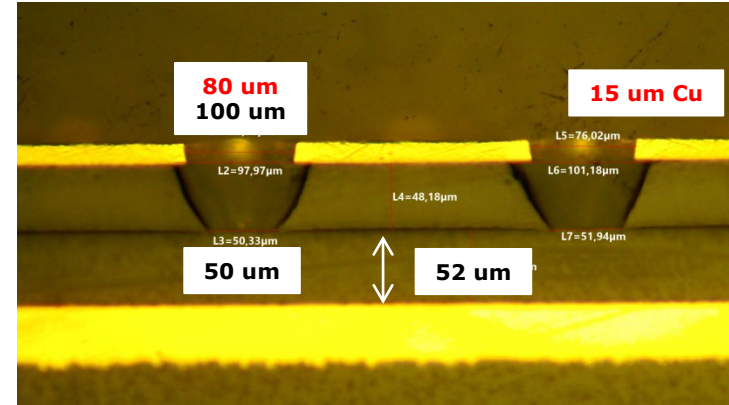


PEP - 1 stackout (CERN)

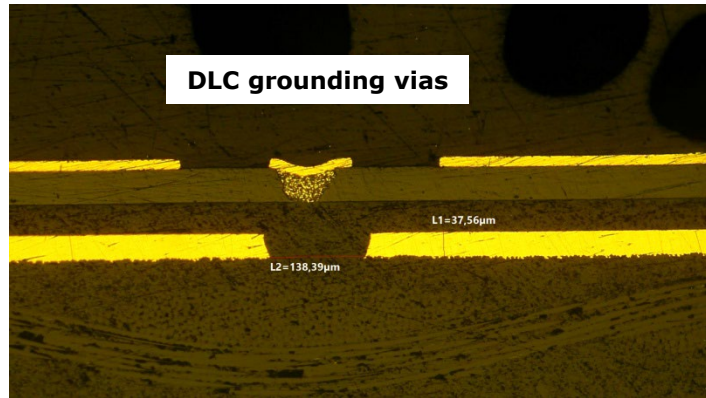
PEP-0 vs PEP-1



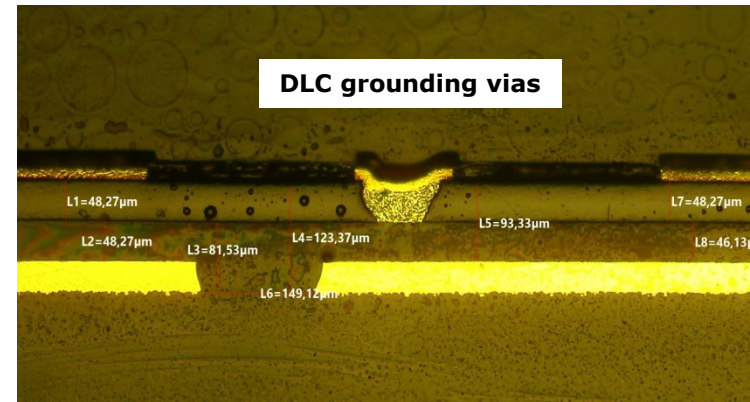
PEP-0 Ampl. Hole (CERN)



PEP-1 Ampl. Hole (CERN)

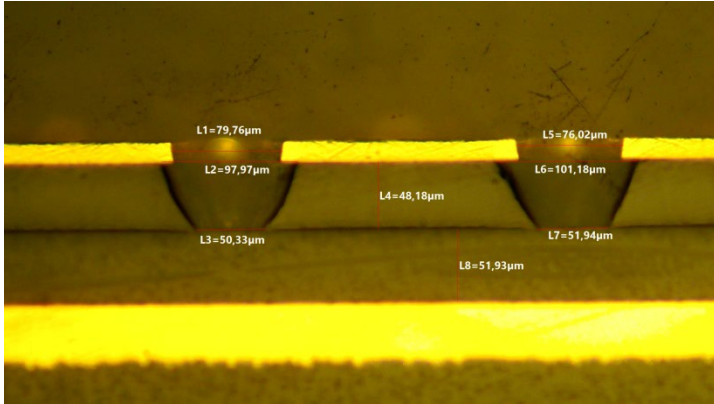


PEP-0 stackout (CERN)

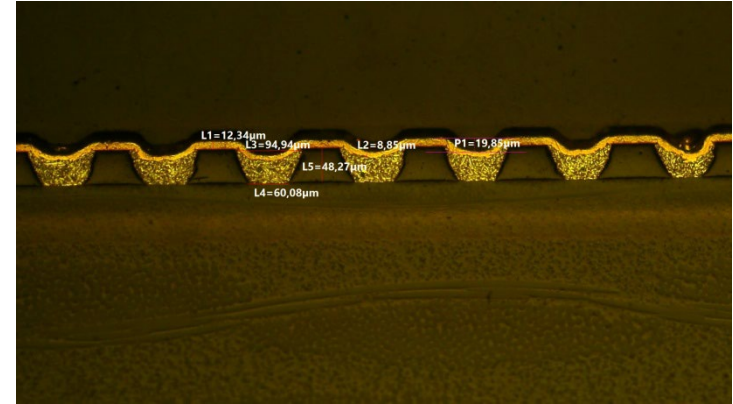


PEP-1 stackout (CERN)

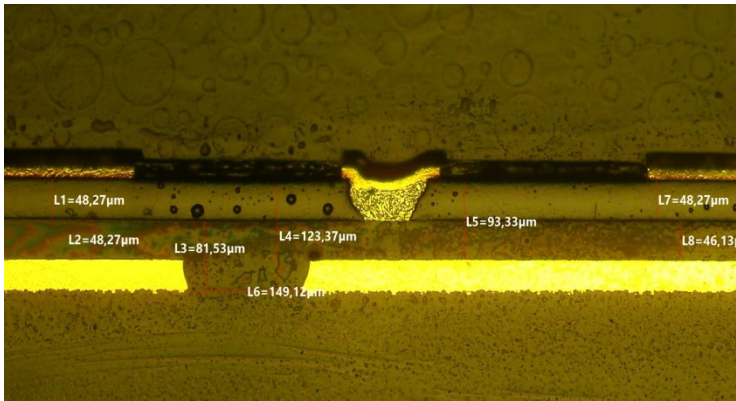
PEP-1 details



PEP-1 Ampl. Hole (CERN)



PEP-1 DLC grounding-hole plating (CERN)



PEP-1 stackout (CERN)