FATIC2

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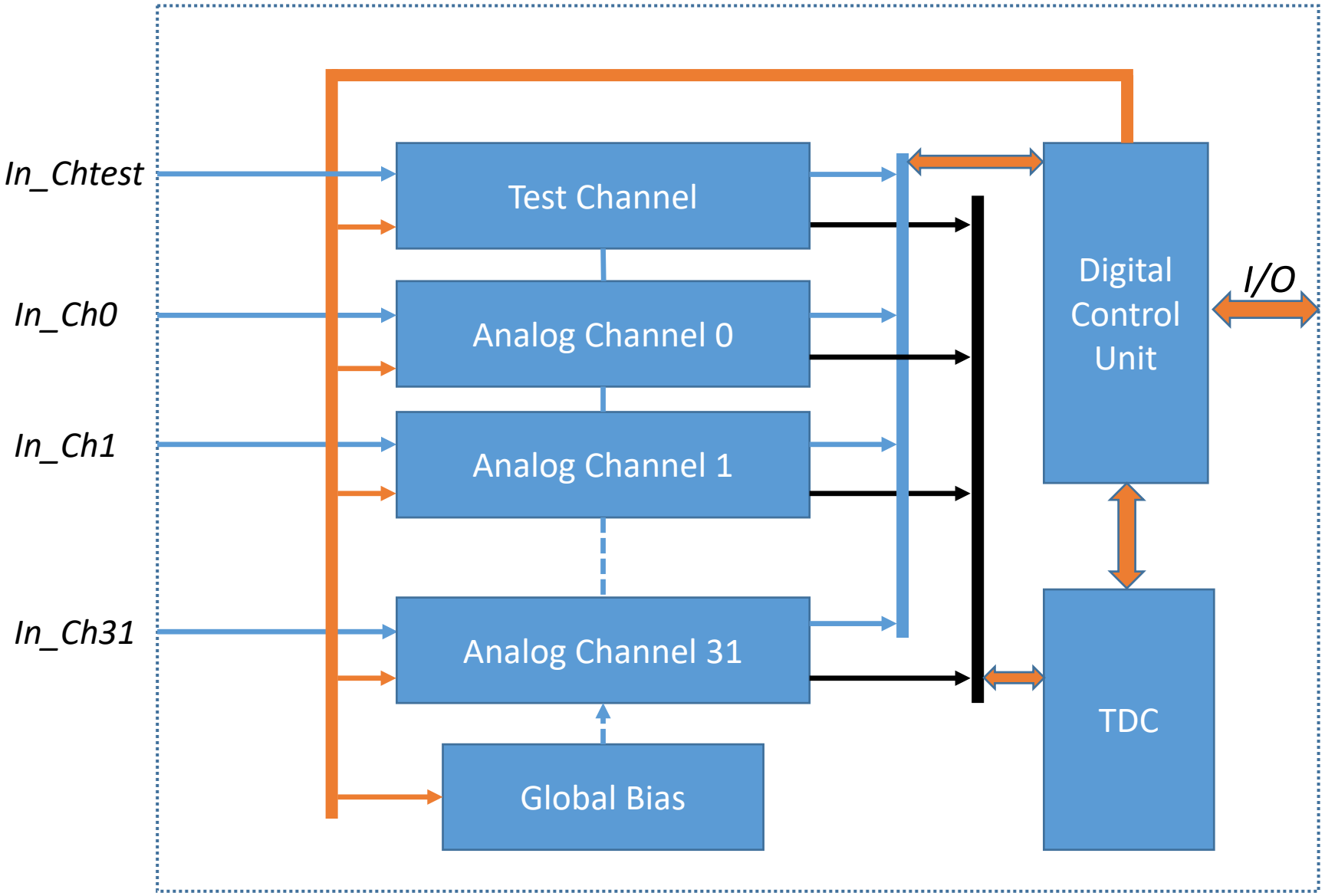
ASIC Architecture



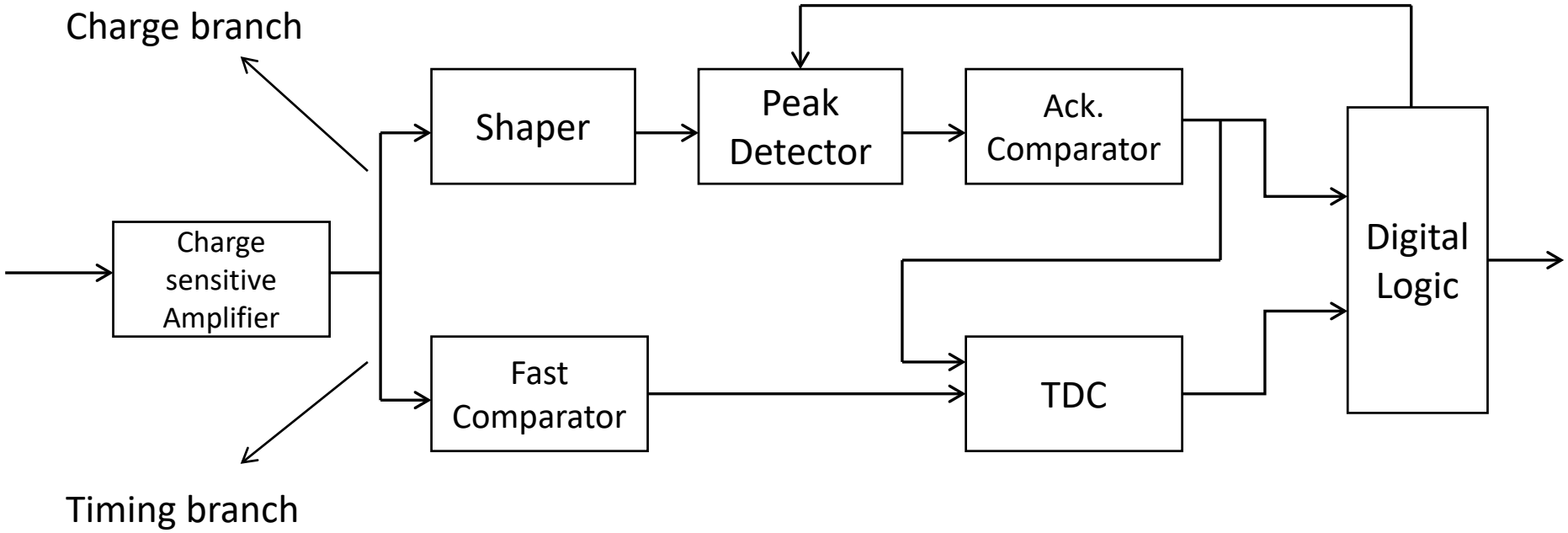
Analog Section:

- 32 Front-end channels:
  - Fast output: designed for timing measurements
  - Slow output: input signal acknowledgement and charge measurement
- Global Bias:
  - temperature and power supply independent
  - internal calibration
  - bias monitoring

Digital Section:

- Control Unit:
  - 320 MHz SLVS I/O link, GBT compatible
  - Channel & Global bias adj. bits
  - TDC control

System block diagram



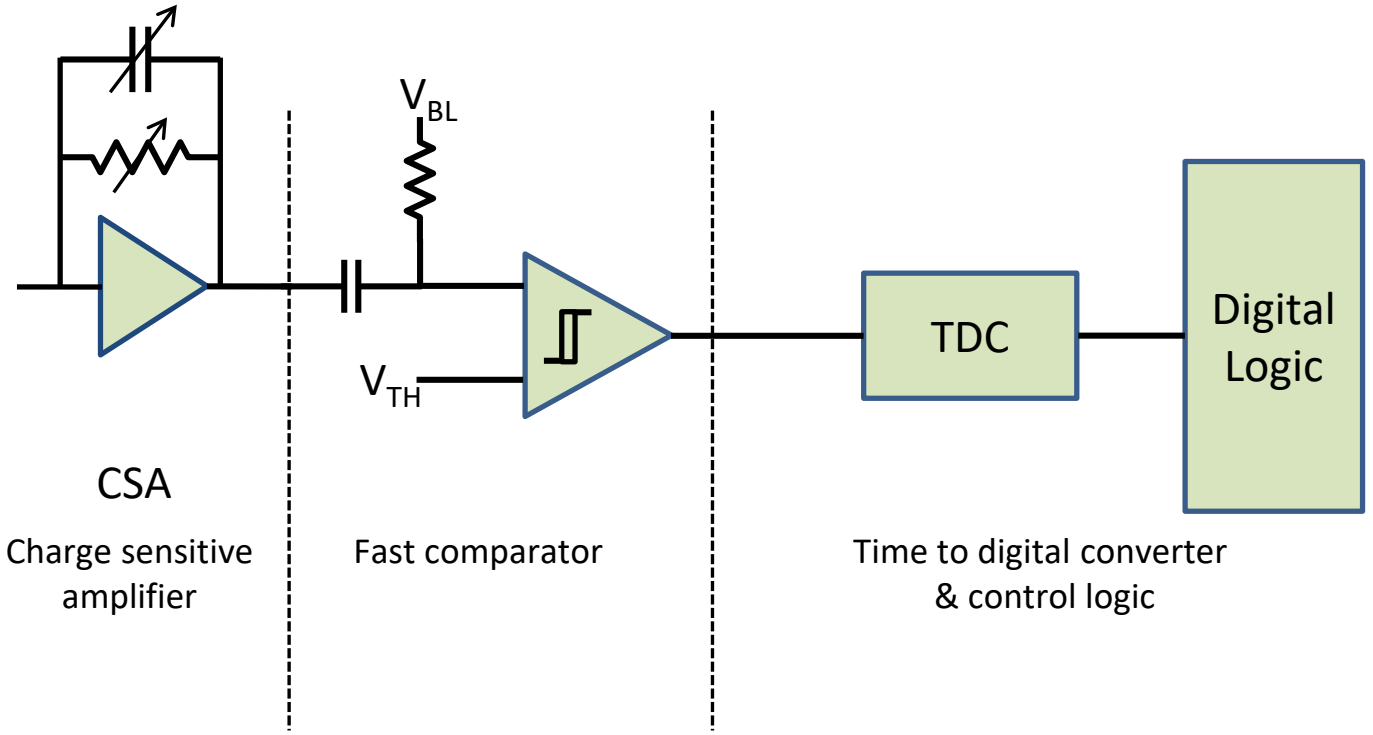
Timing branch:

- ✓ Measures the arrival time of the input signal with low jitter

Charge branch:

- ✓ Acknowledgment of the input signal and charge measurement

Timing Branch Architecture



CSA features (High gain & 15 pF input capacitance):

- Peaking time ≈ 8ns
- Time jitter s ≈ 350ps with 6180e- (1fC input charge)
- ENC ≈ 18.5e-/pF*Cin+227.5e- (505e- Cin=15pF)
- Current consumption ≈ 1mA
- Technology node: 130nm

Fast Comparator:

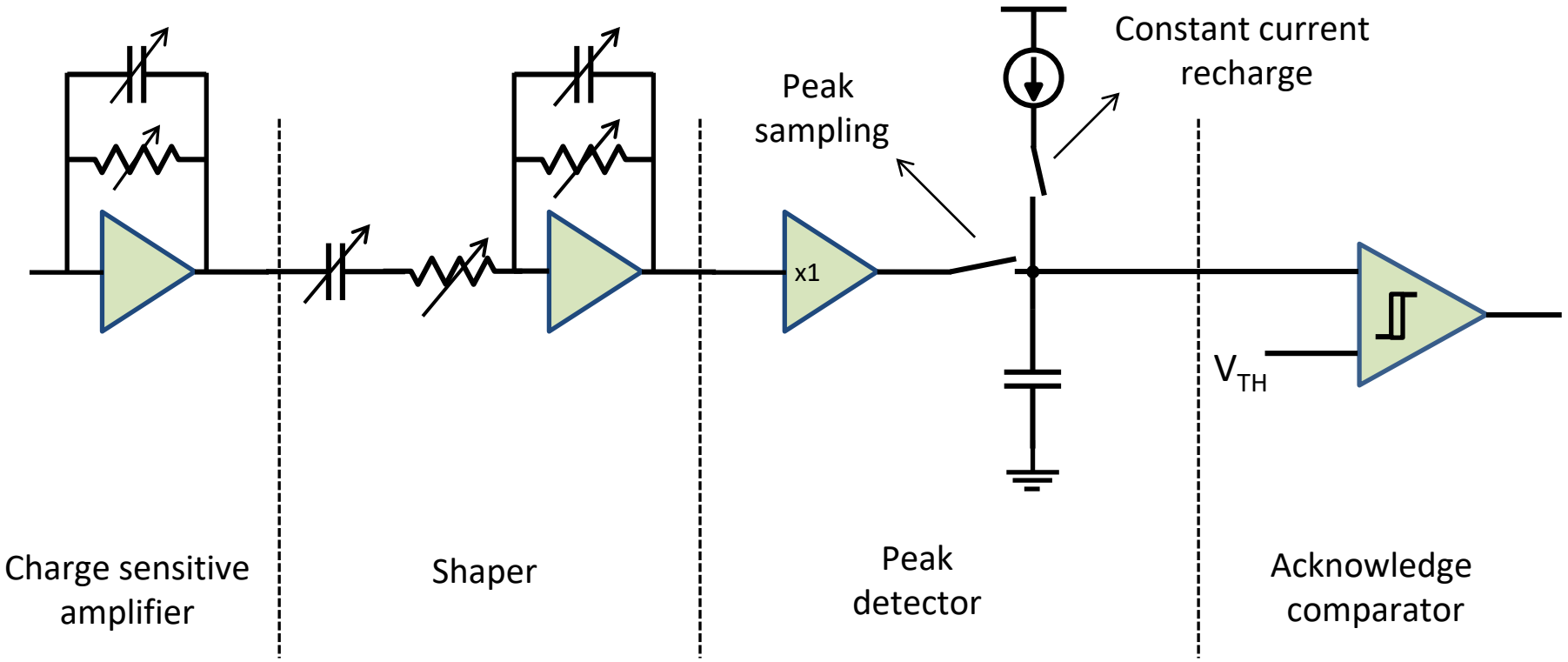
- Threshold from 0 to 76.5ke-, step 300e-

CSA settings:

- Input signal polarity: positive & negative
- Gain: High ≈ 50mV/fC, Low ≈ 10 mV/fC
- Recovery time: adjustable

TDC resolution: 100ps (5 bits fine + 16 bits coarse)

Charge Branch Architecture



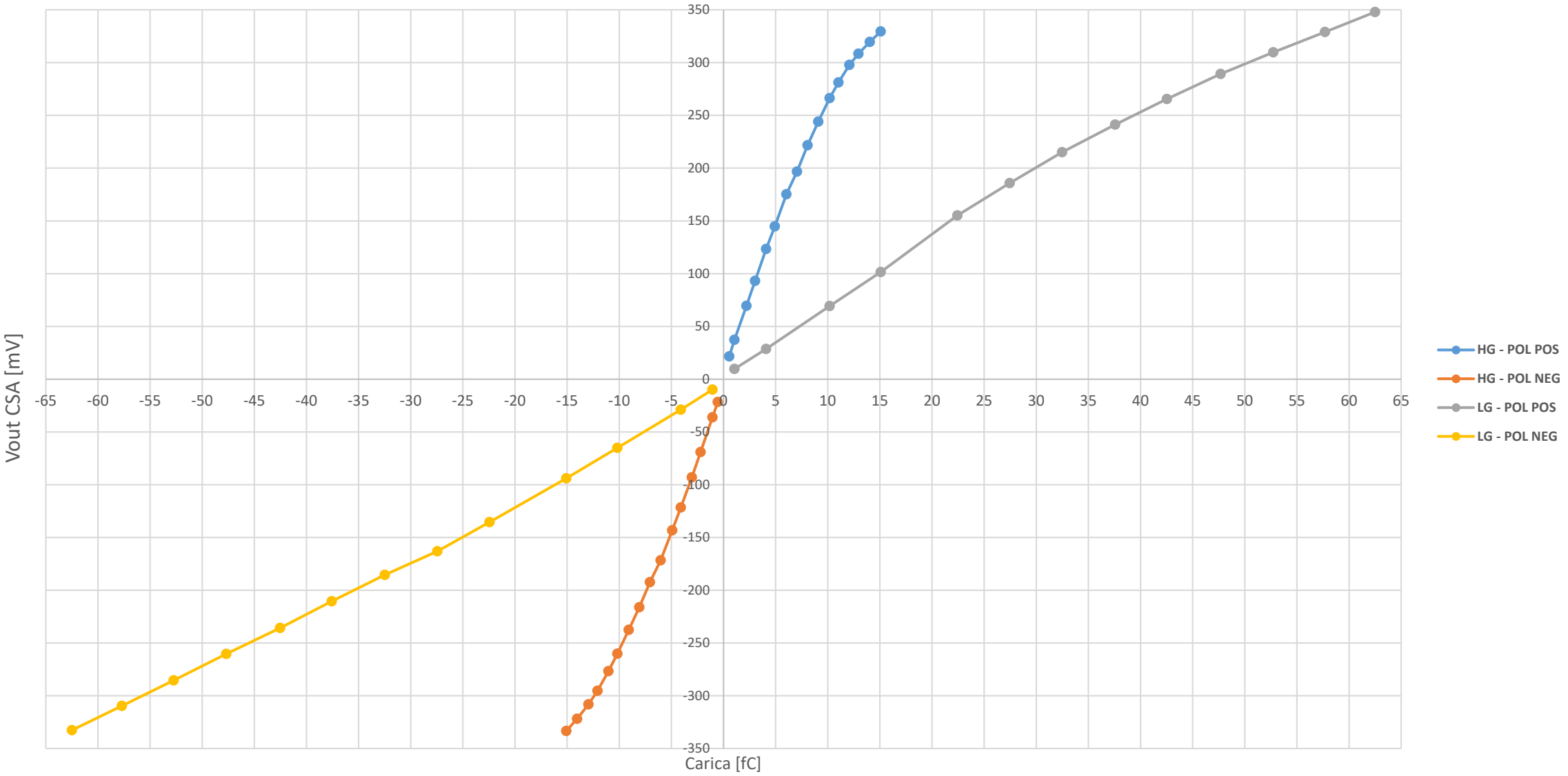
Shaper feature:

- Peaking time: 25ns, 50ns, 75ns, 100ns (polarity adj.)

Acknowledgement comparator:

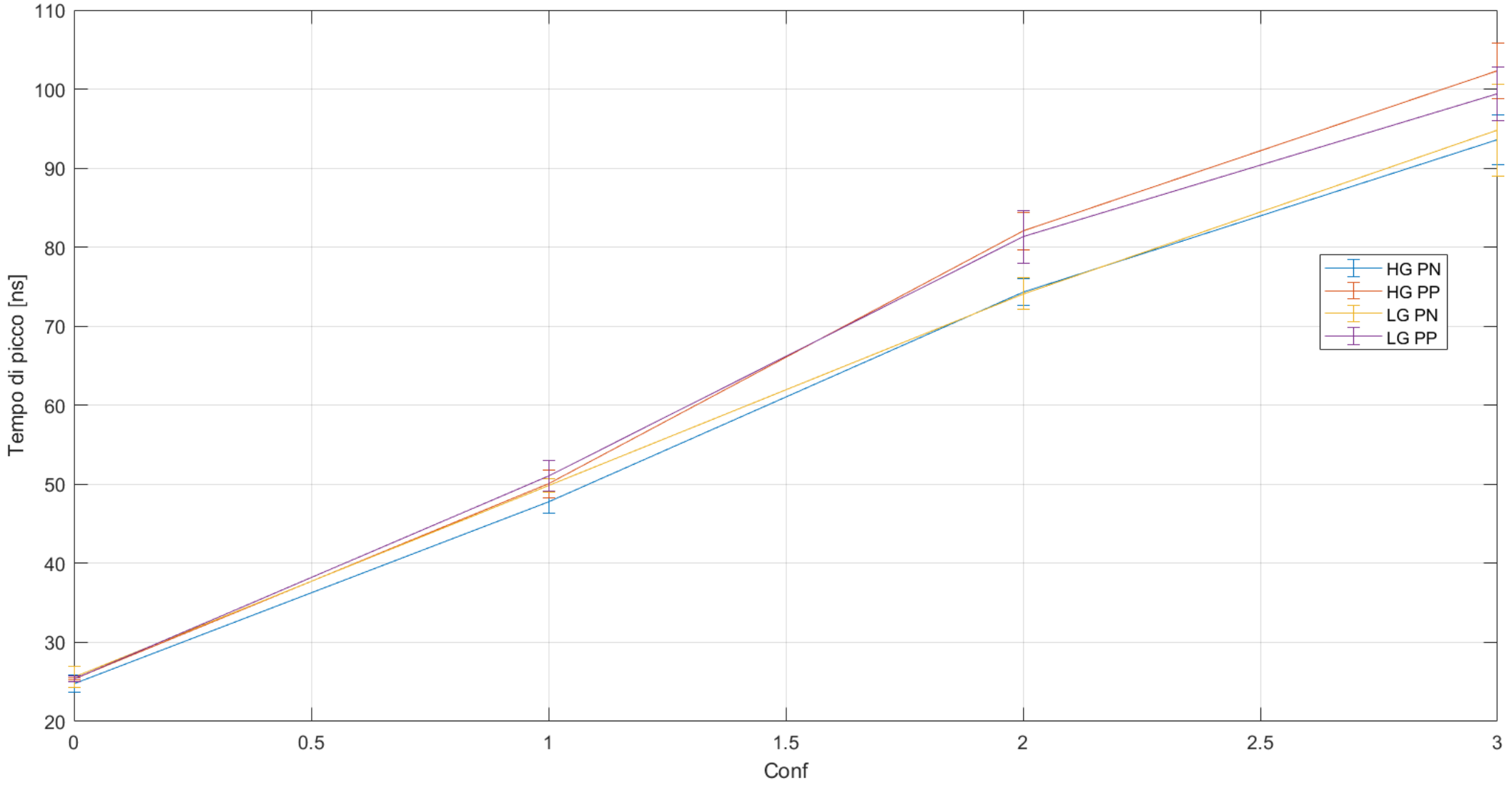
- Threshold from 0 to 58.65 ke-, step 230e-

CSA output dynamic

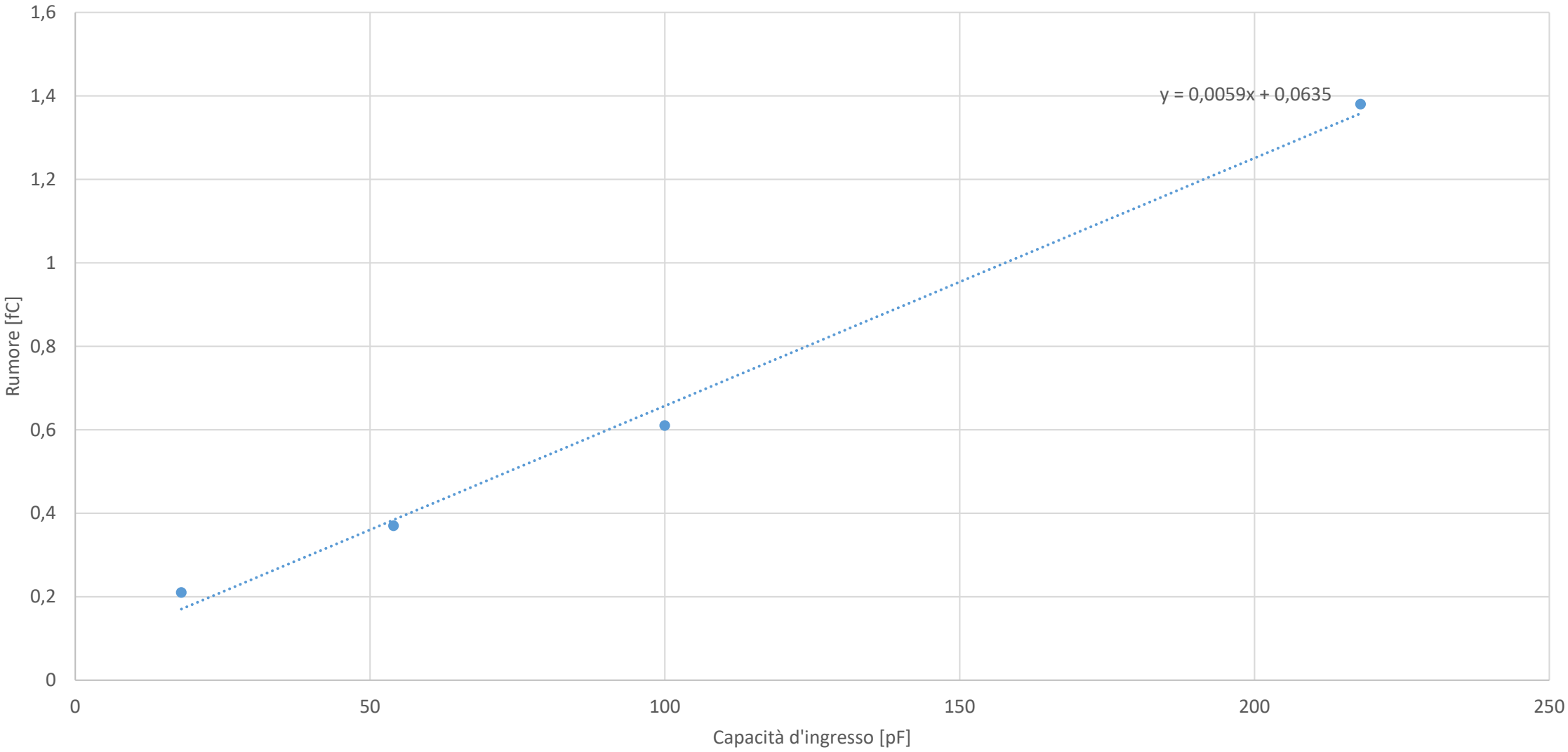


Shaper peaking time

Shaper peaking time vs configuration

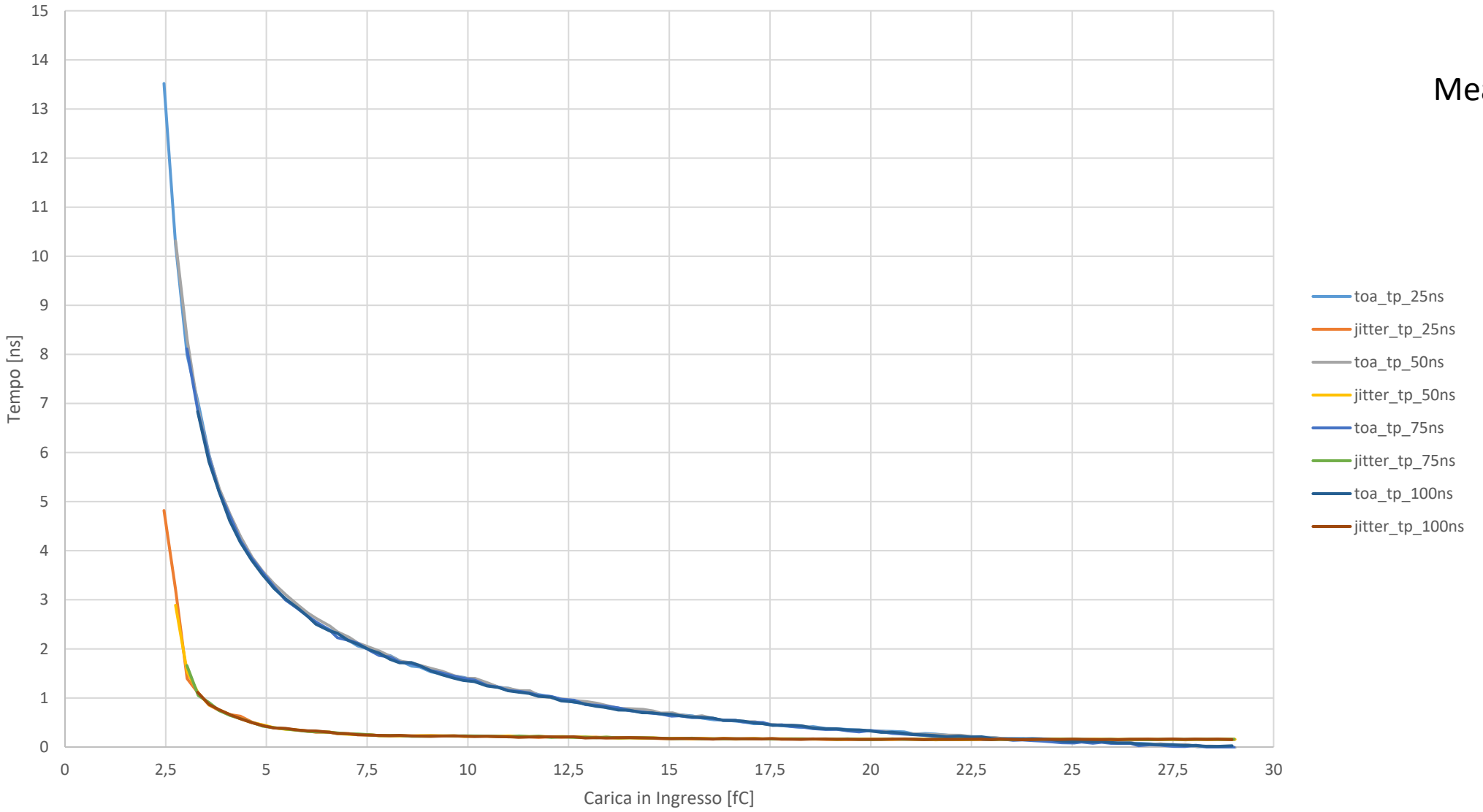


CSA Noise vs input capacitance



CSA settings: low gain, positive polarity

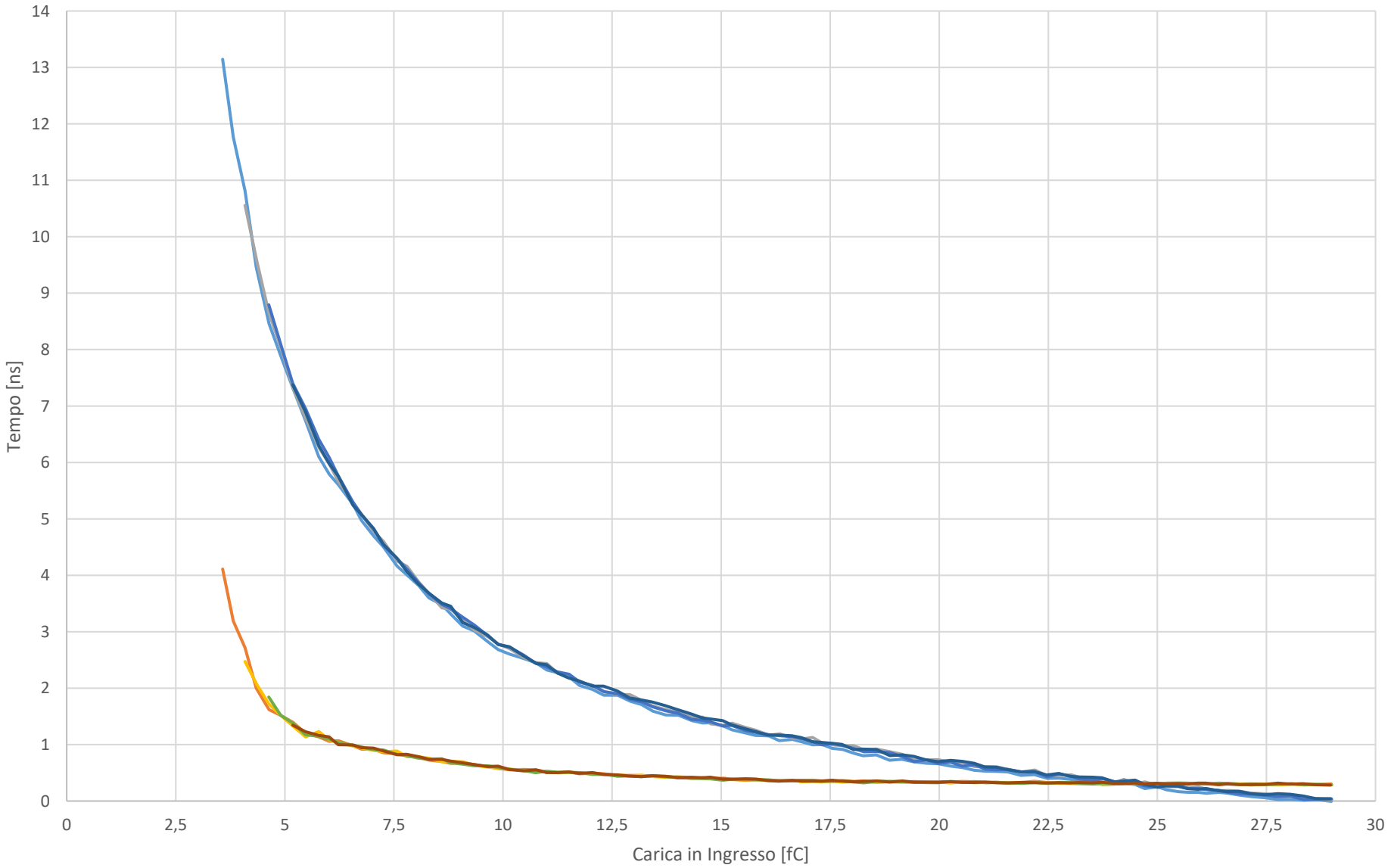
FATIC2: time jitter and time of arrival (1/4)



Measurement conditions:

- Low gain
- Positive polarity
- Cin: 18 pF

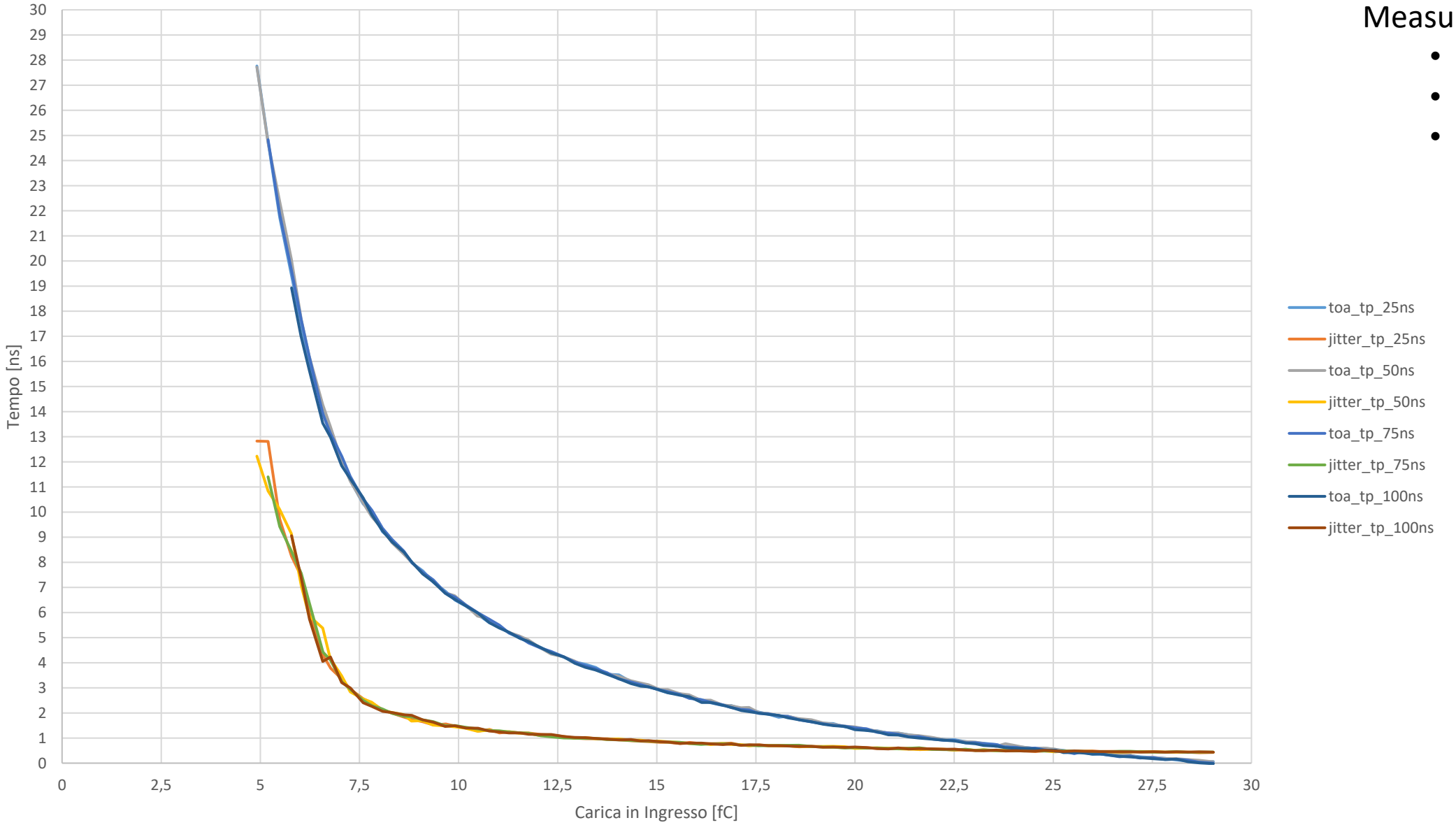
FATIC2: time jitter and time of arrival (2/4)



Measurement conditions:

- Low gain
- Positive polarity
- Cin: 54 pF

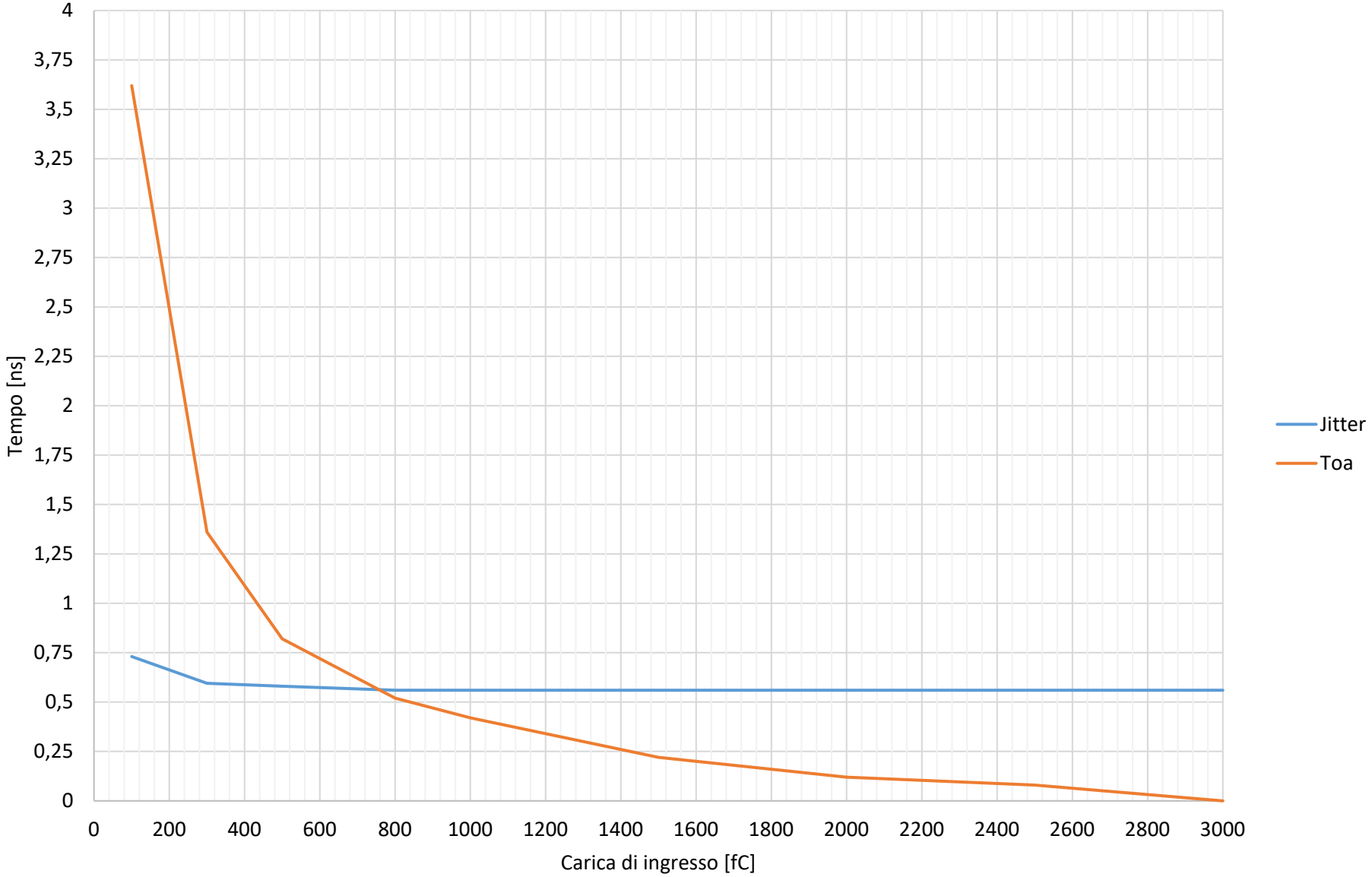
FATIC2: time jitter and time of arrival (3/4)



Measurement conditions:

- Low gain
- Positive polarity
- Cin: 100 pF

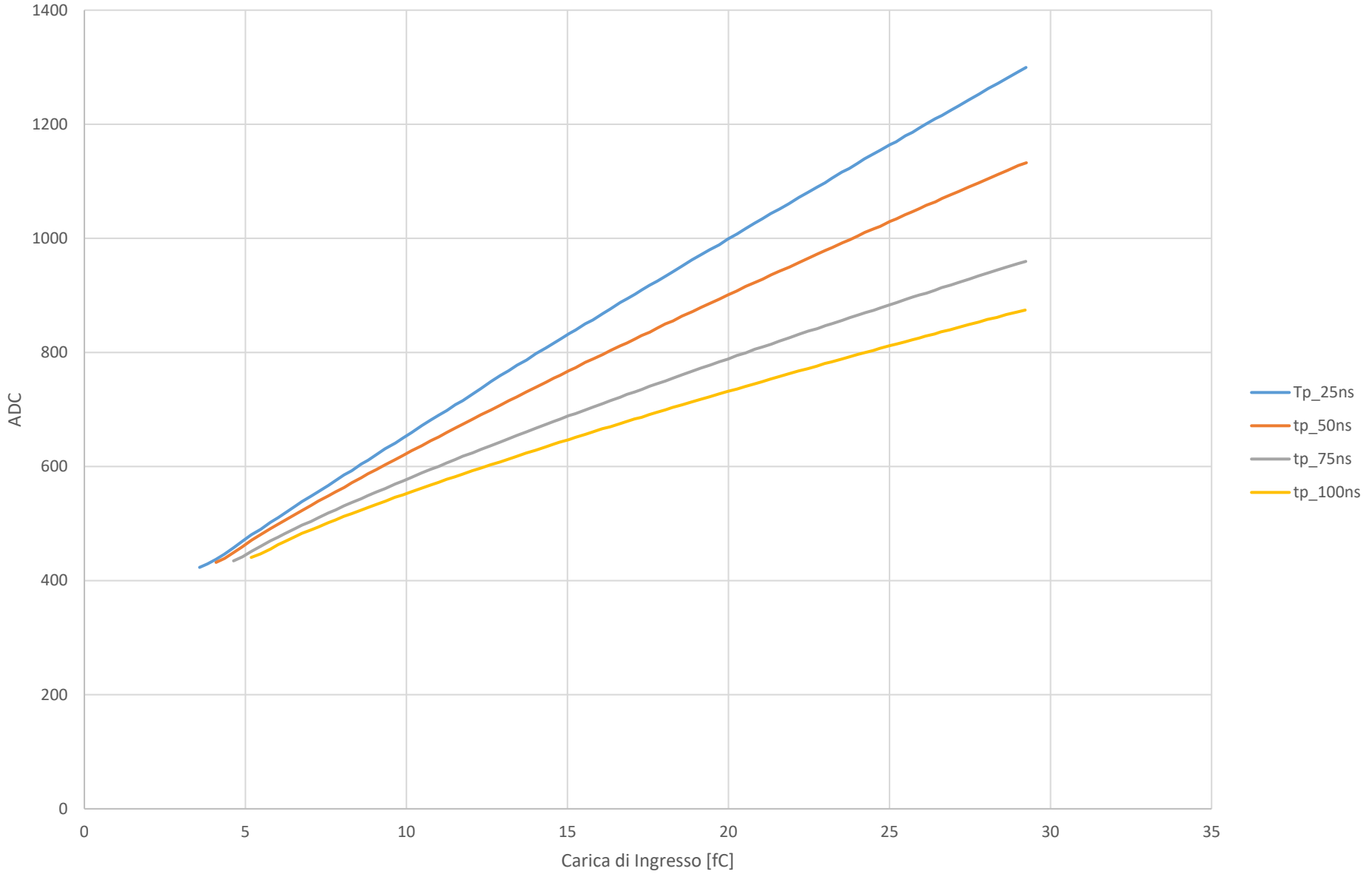
FATIC2: time jitter and time of arrival (4/4)



Measurement conditions:

- Low gain
- Positive polarity
- Peak. Time: 100 ns
- Cin: 218 pF

FATIC2: charge branch measurement



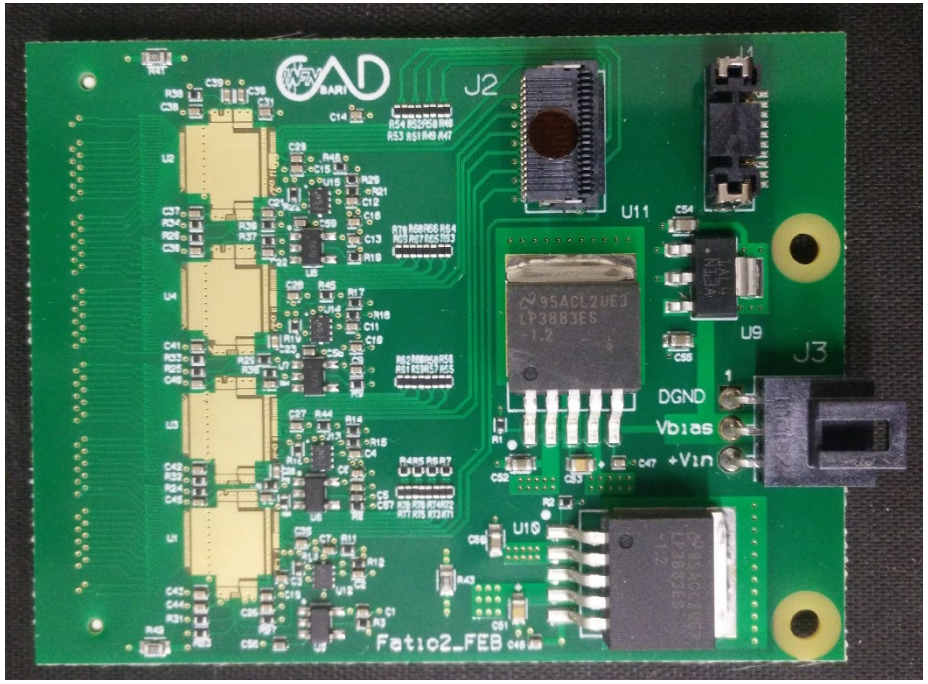
Measurement conditions:

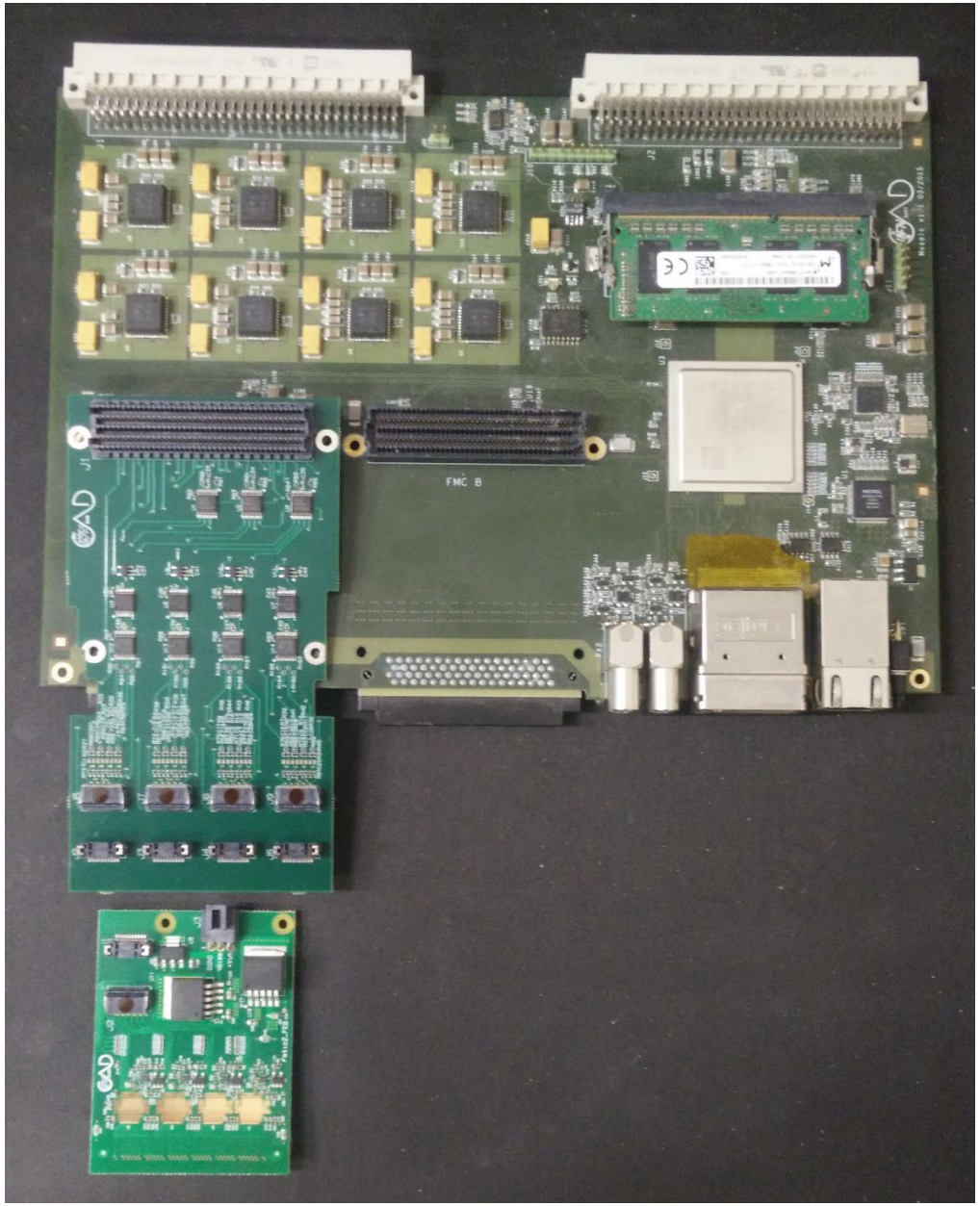
- Low gain
- Positive polarity
- Cin: 54 pF

FATIC2: Front-End Board

FATIC2 DAQ:

- FATIC2 FEB:
  - 4 FATIC2 dices bonded for a total of 128 channels
  - Fire-Fly connection HUB
- FATIC2 HUB:
  - 4 I/O ports to FATIC2 FEBs
- MOSAIC BOARD:
  - Control and Data Acquisition





Channel Settings

CSA settings:

- Input signal polarity: positive & negative
- Gain: High ≈ 50mV/fC, Low ≈ 10 mV/fC
- 8 global bits for recovery time adj.

Fast comparator:

- 8 global bits for threshold (LSB = 2,5 mV => 300 e- in HG)
- 7 local bits for threshold adj.: 6 + 1 for sign (LSB = 2 mV => 240 e- in HG)
- 6 global bits for hysteresis (LSB = 1 mV => 120 e- in HG)

Arming comparator:

- 8 global bits for threshold (LSB = 2,3 mV => 230 e- in HG)
- 7 local bits for threshold adj.: 6 + 1 for sign (LSB = 1,725 mV => 175 e- in HG)
- 6 global bits for hysteresis (LSB = 1,15 mV => 115 e- in HG)

Shaper:

- 2 global bits for peaking time: 25, 50, 75, 100 ns

Peak detector:

- 6 global bits for ToT discharge current adj. (LSB = 400 nA => 80 μV/ns)

FATIC2 specifications

- 33 analog channels: 32 for detector read-out + 1 for test purposes
- Internal calibration with voltage step
- Calibration injection capacitance and CSA feed-back capacitance measurement circuit
- Bias currents and voltage references monitoring (external ADC needed)
- 100 ps TDC: 33 inputs from analog channels + 1 external input
- 320 MHz link, LpGBT compatible
- Power supply 1.2 V
- Channel current consumption 2.8 mA
- Technology node: 130 nm