FALAPHEL: Next submission

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Problem/Opportunity

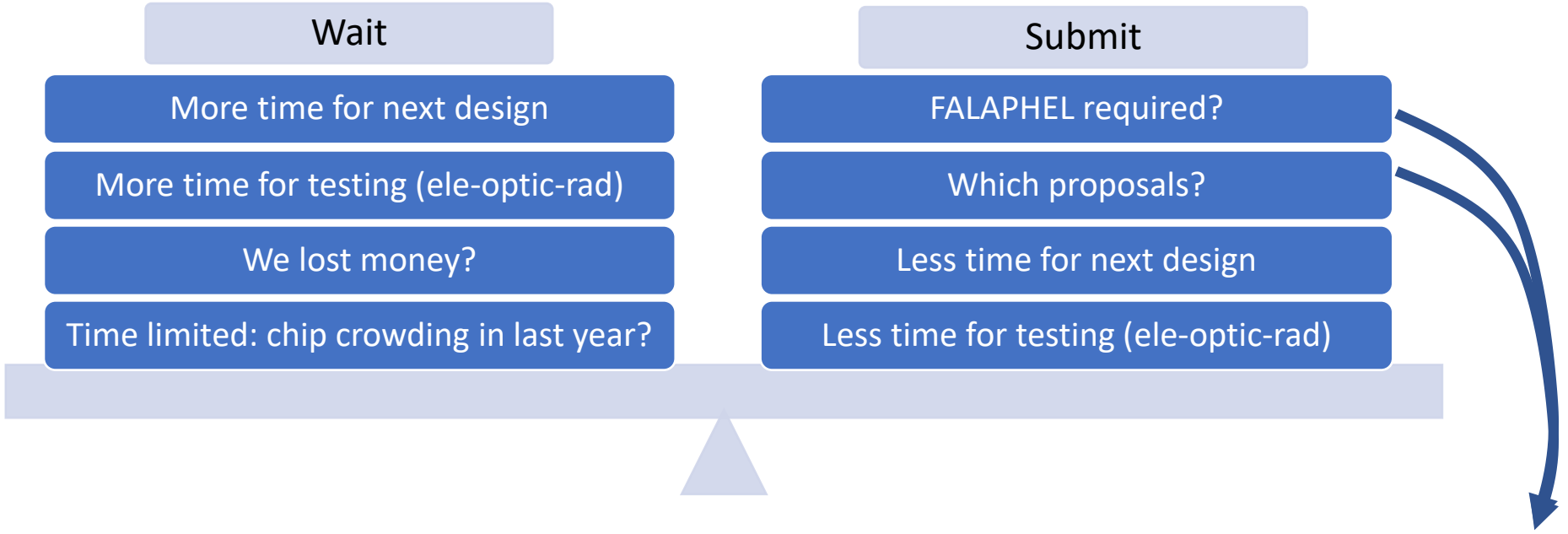
Now

TSMC mini@sic	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
TSMC 0.18µm CMOS General Mixed-Signal/RF		23 *			18			31				
TSMC 0.18µm CMOS High Voltage BCD Gen 2				6				24				
TSMC 65nm CMOS Low Power MS/RF		2		20		15			14		23	
TSMC 40nm CMOS Low Power MS/RF				27						19		
TSMC 28nm CMOS RF HPC+		2			25		27			26		
TSMC 16nm CMOS RF FinFET Compact											16	

Opportunity?

28 HPC+ (use MMWAVE PDK)	7M	lp7m_4x1y1z_alrdl	/
	8M	lp8m_5x2r_alrdl	lp8m_5x1z1u_ut-alrdl
		lp8m_5x2r_ut-alrdl	
	9M	/	lp9m_5x1y1z1u_ut-alrdl

Does it make sense to send a new design?



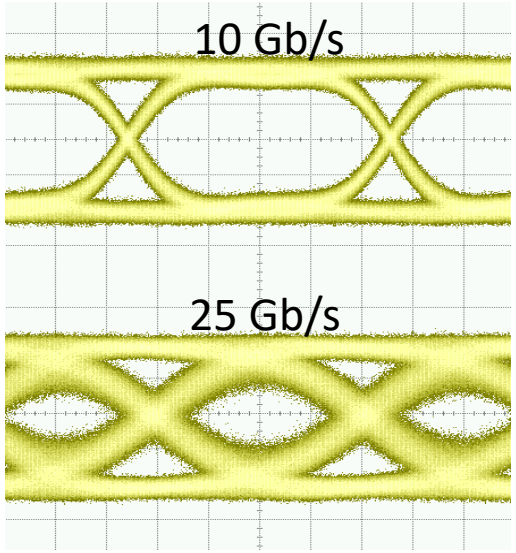
Which is the FALAPHEL status?

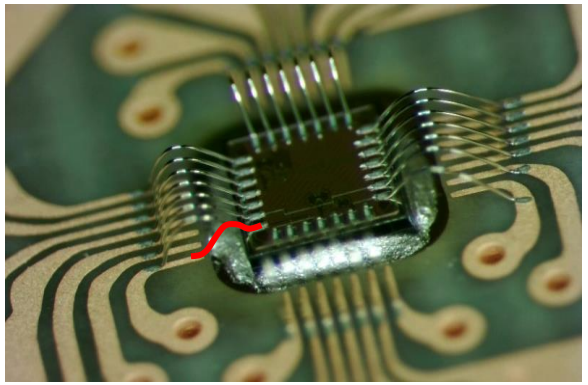
What goals have already been achieved? Are they on time?
Have the goals or timeline been re-evaluated based on the current status?

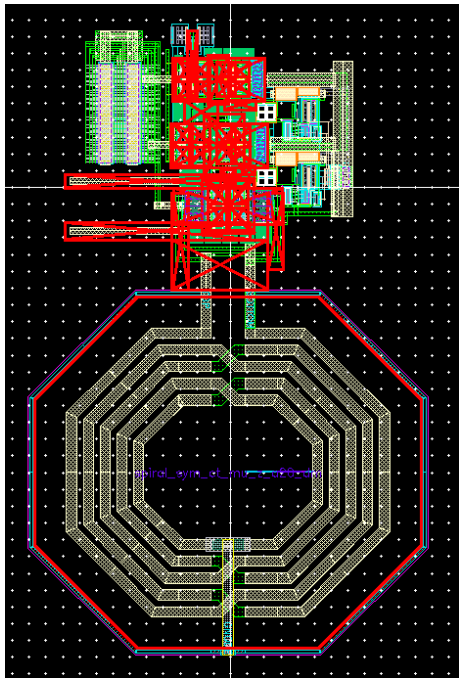
25 Gb/s Driver status (now)

We already have a driver for SiPh Ring Resonator operating up to 25 Gb/s:

- 28nm HPC technology
- 8 Metal technology
- CML stages
- Passive and Active Bandwidth enanchement techniques (inductors)





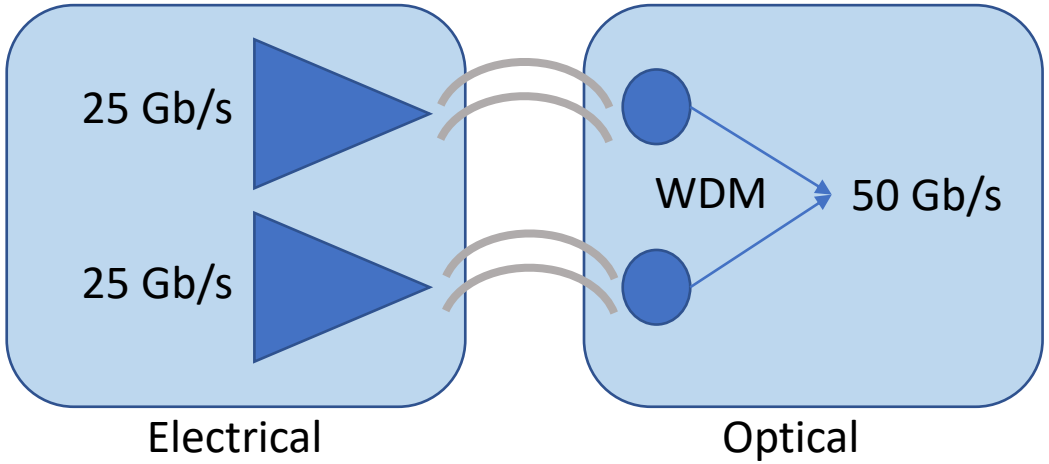


Layout of the 25 Gb/s driver in 28 nm

Only preliminary electrical tests

Radiation and optical tests: waiting

Proposal 1: two drivers



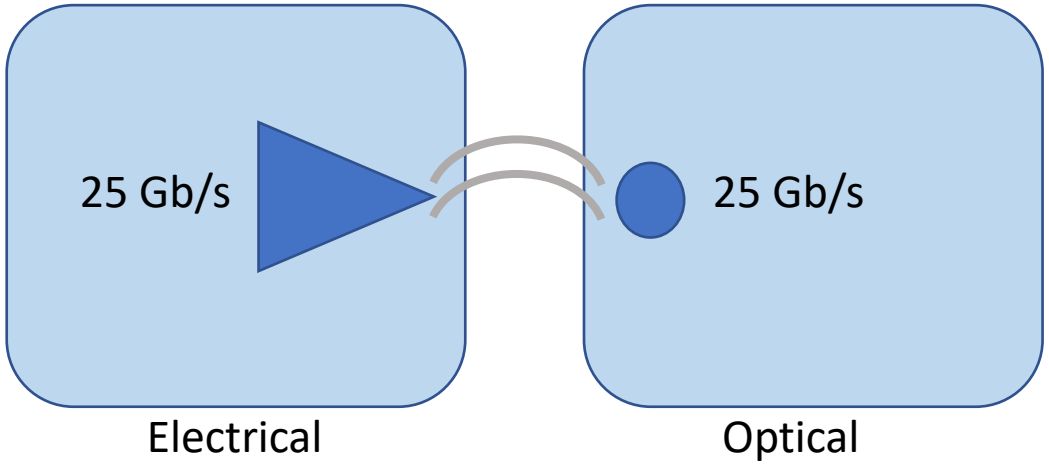
Pros:

- Intermediate step before FALAPHEL goal (4 drivers)

Cons:

- New technology from HPC to HPC+ (for 25 Gb/s), issues?
- New technology from 8M to 9M, issues?
- No inductors available, custom design, few experience
- No accurate ring model available now
- Only electrical test doesn't make sense
- No optical chip available for that test in next months
- Next optical chip available maybe Q4-2023 (if submission Q3-2022)

Proposal 2: one driver



Pros:

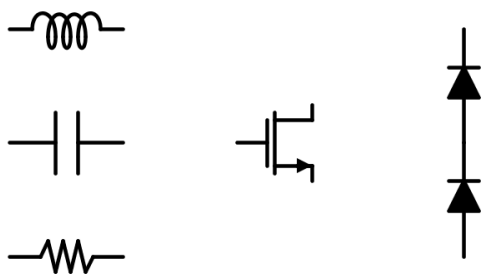
- Explore new technology from HPC to HPC+ (for 25 Gb/s)
- Explore new technology from 8M to 9M

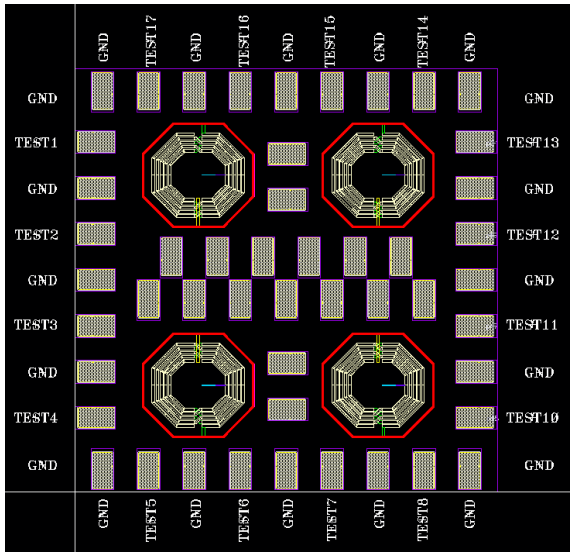
Cons:

- Already a 25 Gb/s 28nm HPC drive, few novelty
- Current driver is not fully electrically tested
- Current driver is not optically tested
- Current driver is not exposed to radiation
- No inductors available, custom design, few experience
- No accurate ring model available now, no novelty

Proposal 3: testing structures

Passive and elementary active devices





Pros:

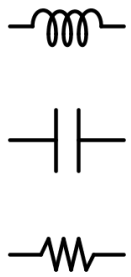
- Inductors know-how
- TID effects on MOSFETs also at RF
- TID effects on passives devices
- Bases for next rad-hard design
- No optical test required

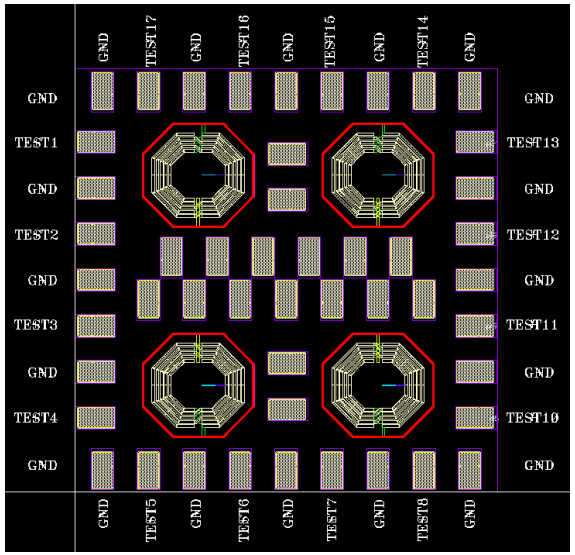
Cons:

- Not explicitly required in FALAPHEL
- Only few devices, not enough to generate simulation models

Proposal 4: testing structures

Passive devices:





Pros:

- Inductors know-how
- TID effects on passives devices
- Bases for next rad-hard design
- No optical test required

Cons:

- Not explicitly required in FALAPHEL
- Few devices, but more than previous solution

Possibility to submit only backend (metals) to reduce cost? Investigating…

Proposal N: mix solutions

Ideas?

To be noted:
Pads and inductors limit the available area