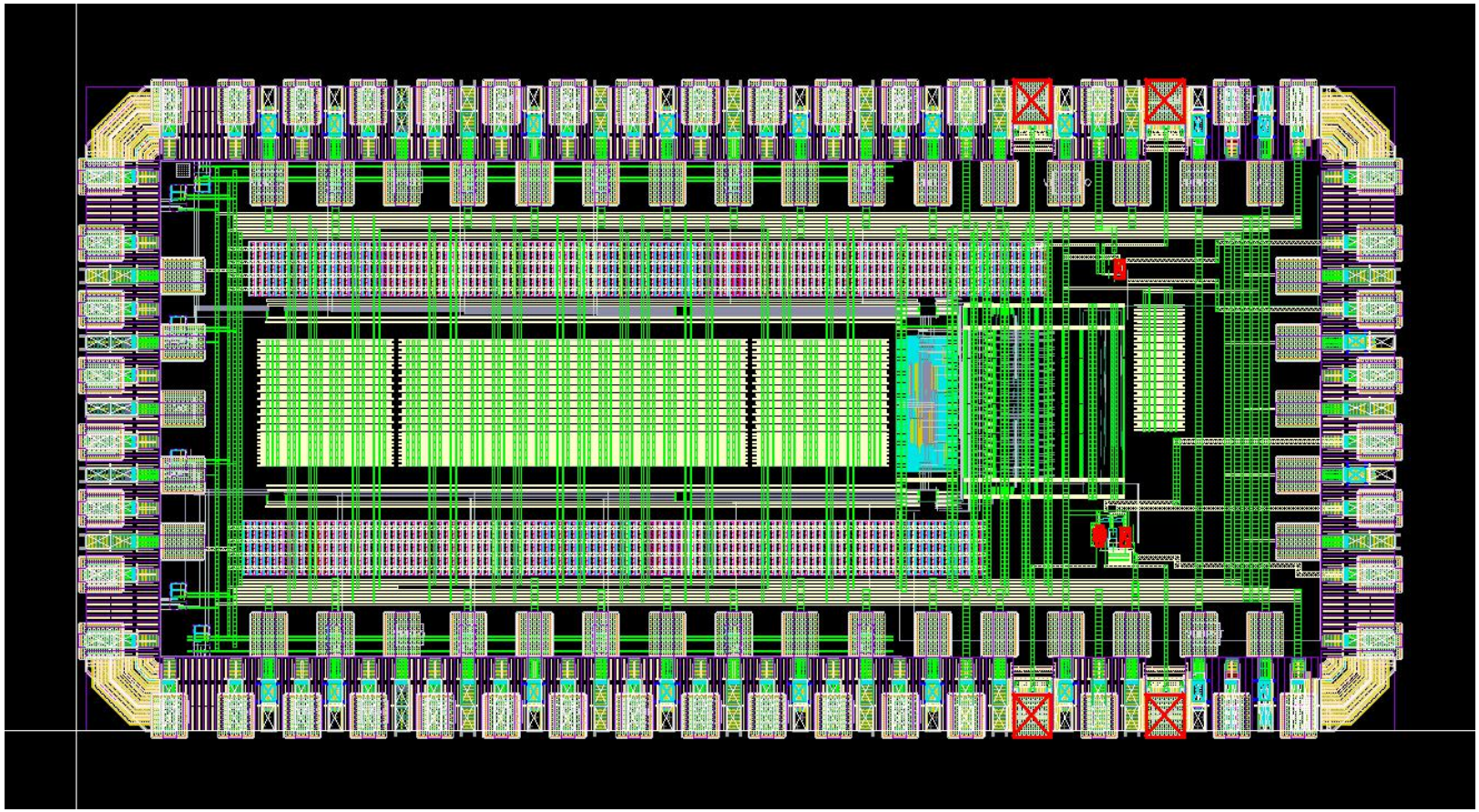
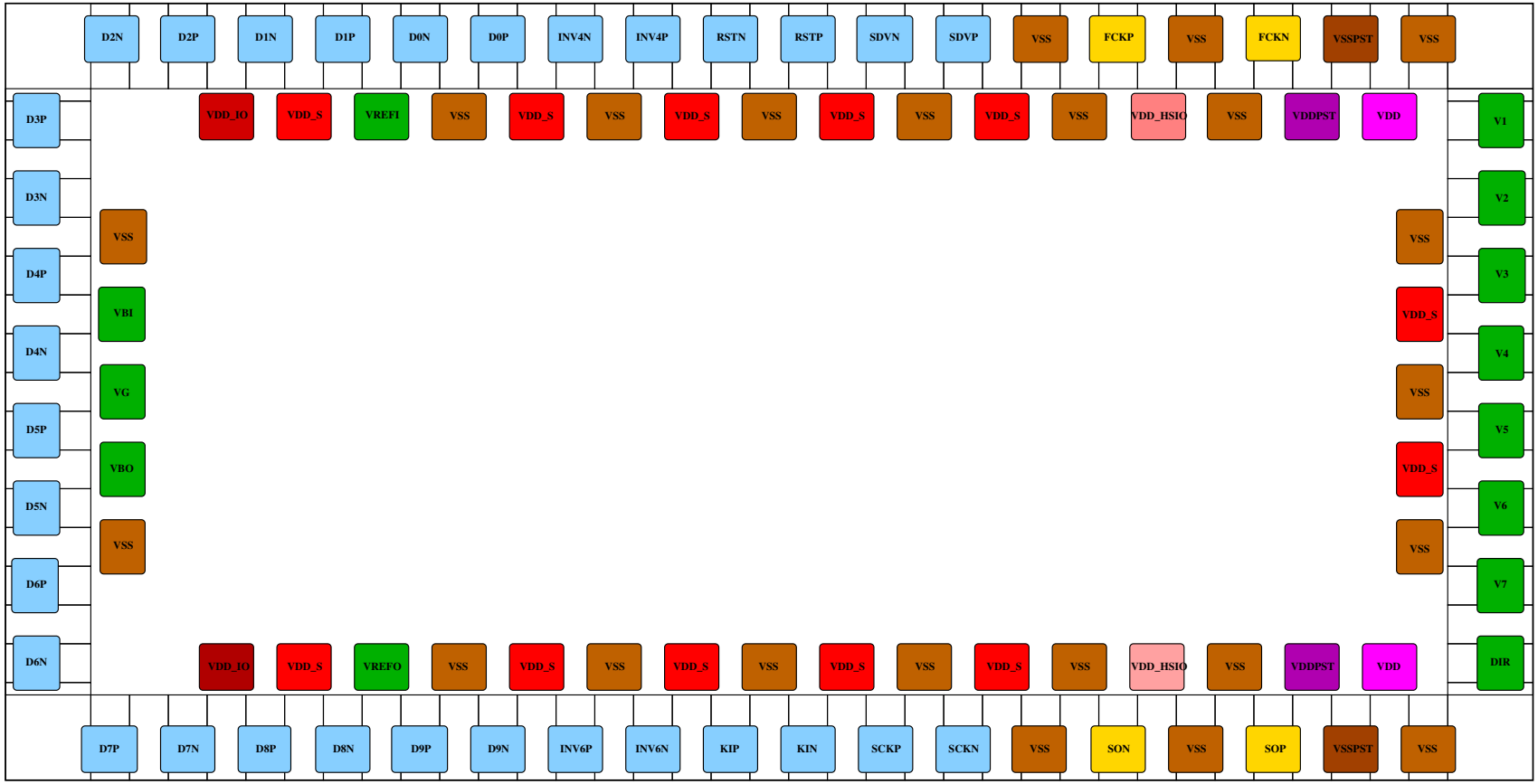


SER28_V1 submitted the 20th of May – Submission finalized the 6th of June (2-weeks process)



Final Pad Ring => 94 pads (52 in the outer ring, 42 in the innr ring)
PWR/GND => 25 GND, 2VDD_IO, 2 VDD_HSIIO, 2VDD_BIST, 12 VDD_SER)
Signals => 12 LVDS I/O, 4 LVDS_IN, 1 CML IN, 1 CML OUT, 13 Analog I/O

Some lessons

- Integration is a big deal => 4-6 weeks
  - Pad Ring generation (in coordination with wire bonding expert)
  - Signal buffering (driven by post layout simulations)
  - Power routing (!!!)
  - Correction triggered by IMEWC feedbacks (2 weeks!)
- Digital on top is more efficient? Maybe we have to move to it! But … what about component development and characterization (a guess? 3-4 weeks for the SER)
- The designer of (a large part of) the core could have problems in taking care of the chip integration and of the development of his design at the same time => do we need an “integration engineer”
- Post-layout simulations are a critical problem (I estimated a simulation time of at least 2 weeks to simulate in different corners and different operating conditions