

28nm AFE developments

BG/PV group

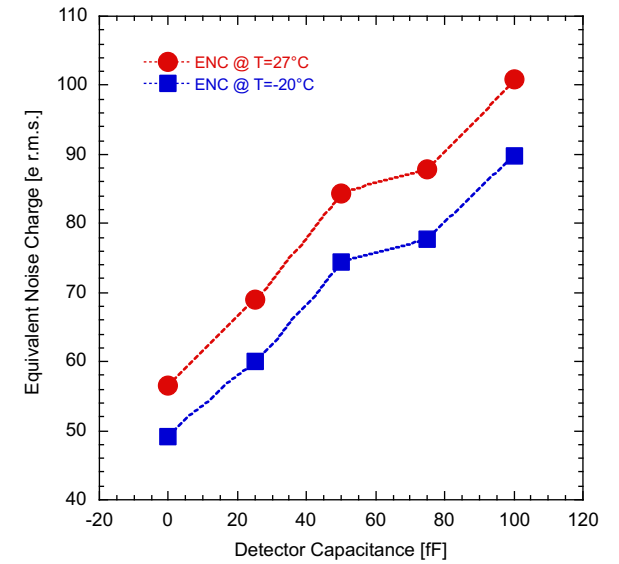
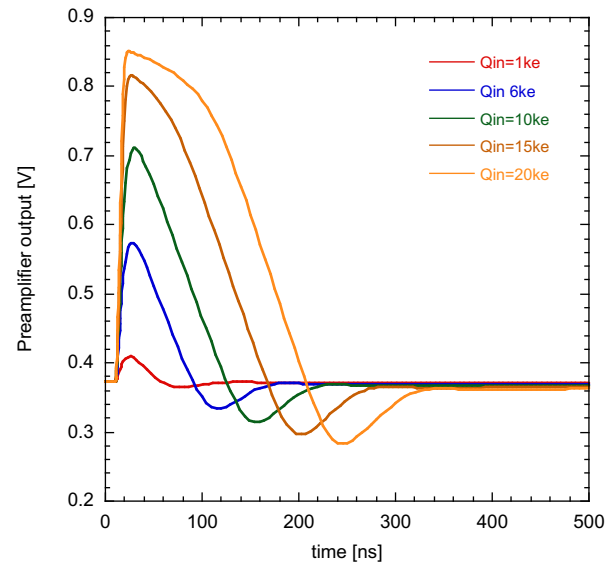
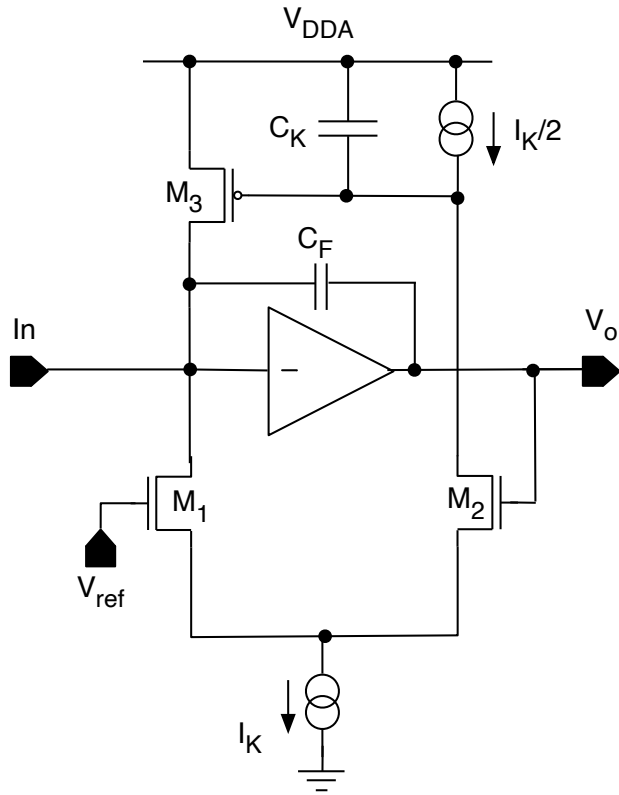


Falaphel general meeting - Jun 8, 2022

Front-end design

- Two different **analog front-end designs** are being investigated:
- **Time-over-Threshold (ToT)** based front-end → charge sensitive amplifier (CSA) + DC coupled comparator, with ToT A/D conversion of the signal + threshold tuning DAC
- **Flash ADC** based front-end → CSA + AC coupled bank of auto-zeroed comparators implementing the flash A/D conversion

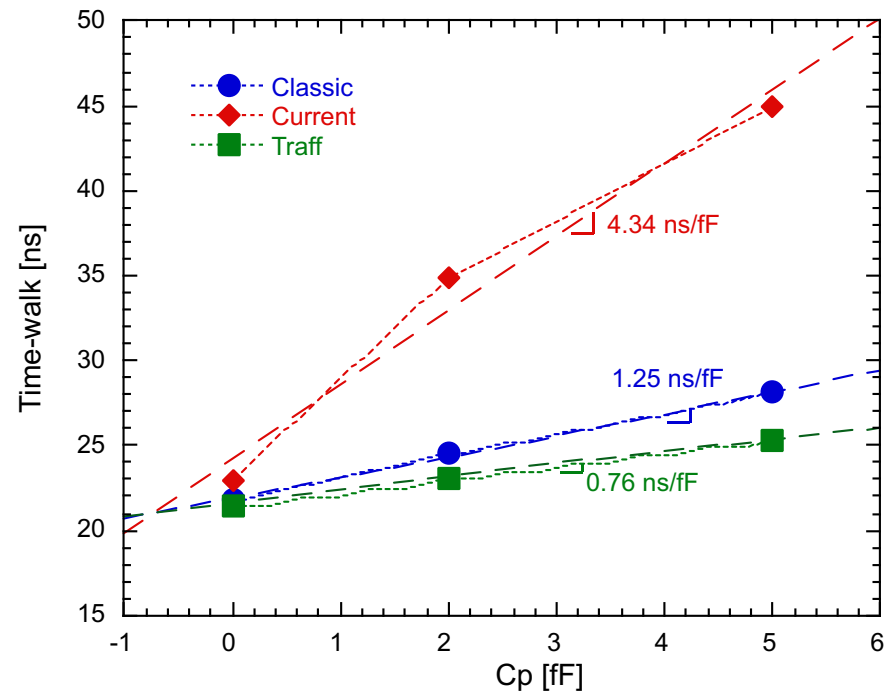
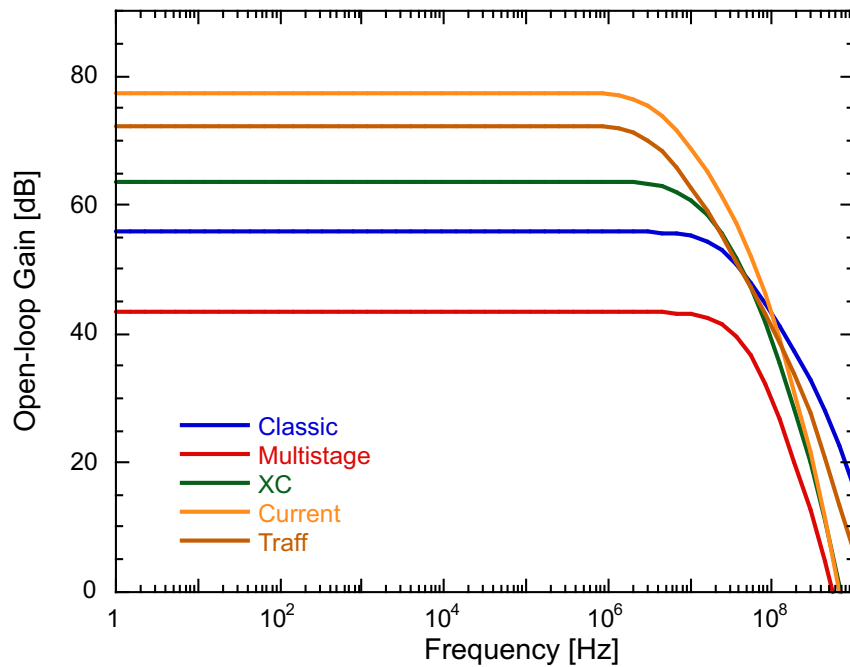
ToT-based front-end: CSA



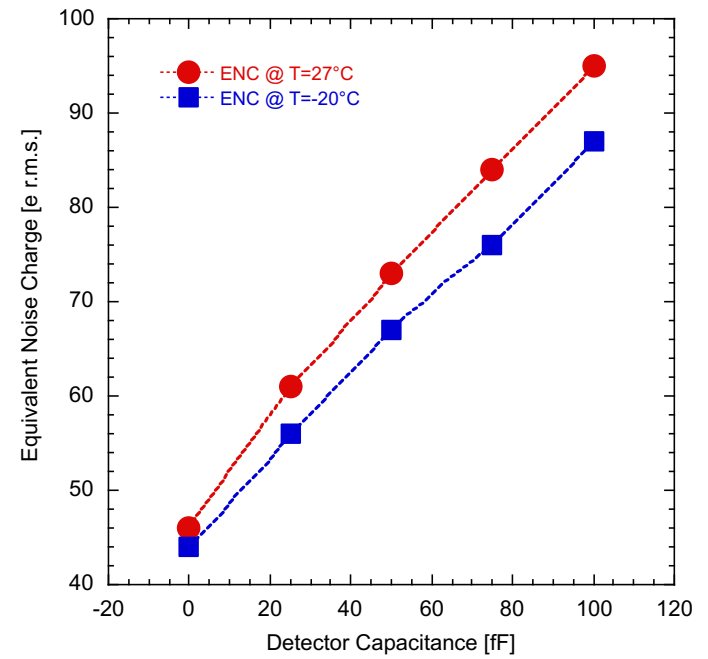
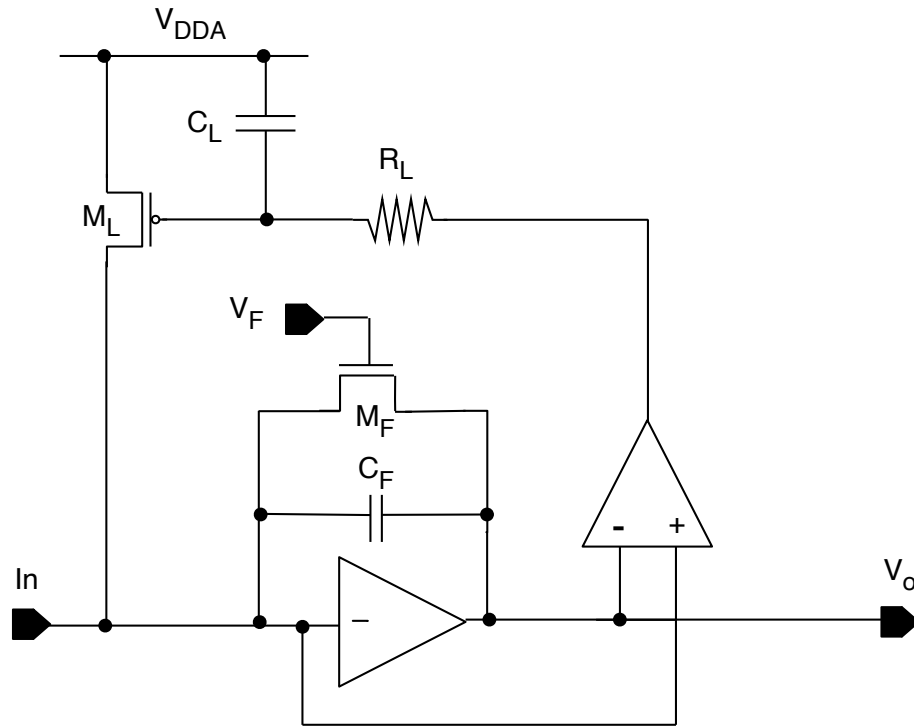
- Preamp with Krummenacher feedback network

ToT-based front-end: comparator

- Different architectures are being investigated
- **Time-walk** for a sub-set of architectures (~500 el. input, ~25 mV/ke- charge sensitivity)
 - Schematic-level simulations (**ideal preamp with 20 ns peaking time**)
 - **Parasitic capacitance** (C_p) added at "main nodes" of the comparators

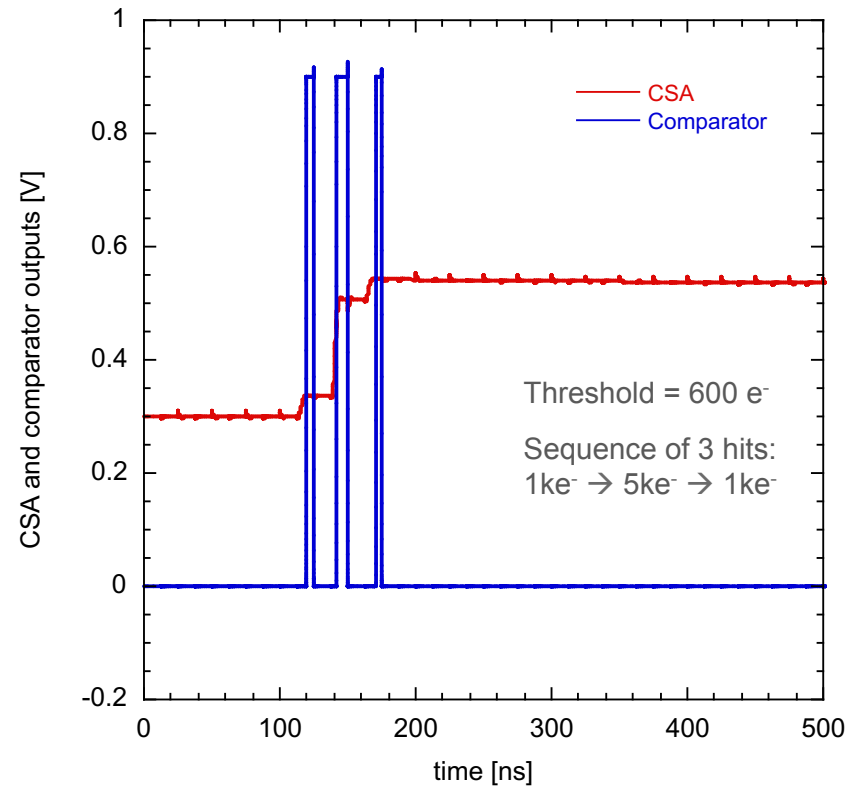
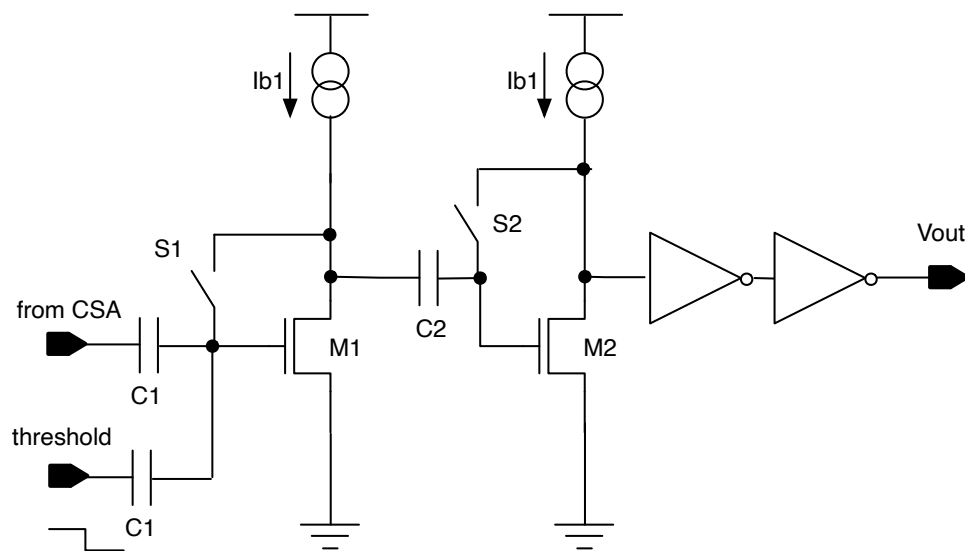


Flash ADC-based front-end: CSA



- Preamp with additional opamp in the feedback network

Flash ADC-based front-end: comparator



- Clocked, **auto-zeroed** comparator featuring low power consumption (700nW)
- **Zero dead-time**, low threshold dispersion ($< 35 e$ r.m.s.)

Conclusions

- **Two different AFEs** are begin investigated in the Falaphel project in a 28 nm CMOS technology:
 - **ToT** A/D conversion
 - **Flash** A/D conversion)
- More **compact** (wrt Linear AFE) preamp forward gain stage used in the Falaphel project
- **Noise** performance very similar to the one obtained for the Linear AFE
- **Layout** of the Flash-ADC based front-end ready. **Integration** in progress.
- **Submission:** mini@asic run in October. 4x4 matrix with simple digital readout + standalone channels with analog test points routed to PADs.
- **Bandgap:** submitted in December 2021. Prototype fabricated, waiting for test board and chip. Measurement setup based on Genesys2 board. Temperature characterization in Bergamo and TID measurements at CERN.