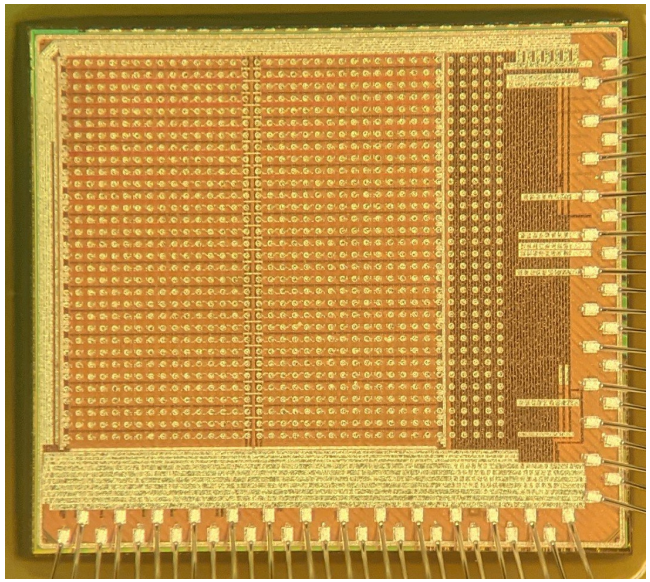
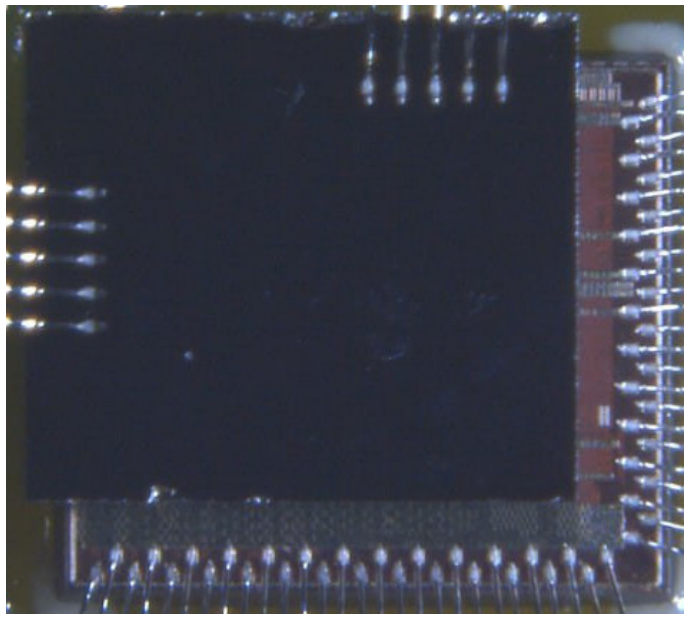
The TimeSPOT1 ASIC

a 28 nm CMOS timing front-end ASIC



TimeSPOT1 ASIC



TimeSPOT1 Hybrid

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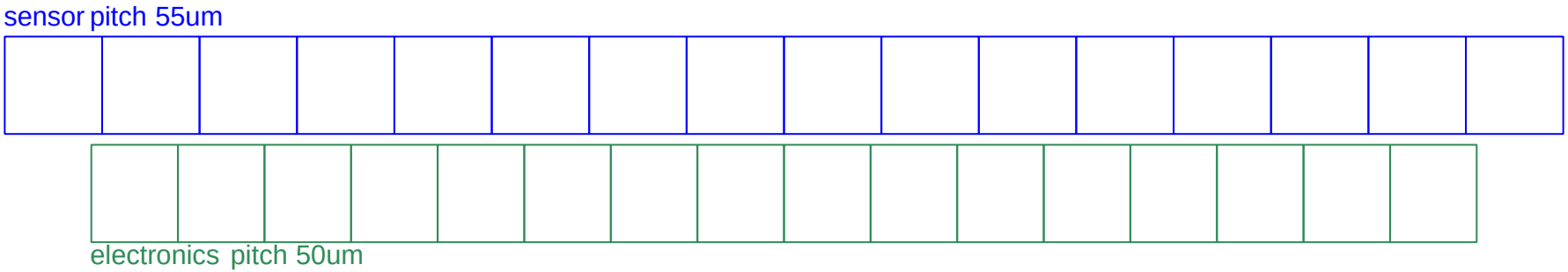
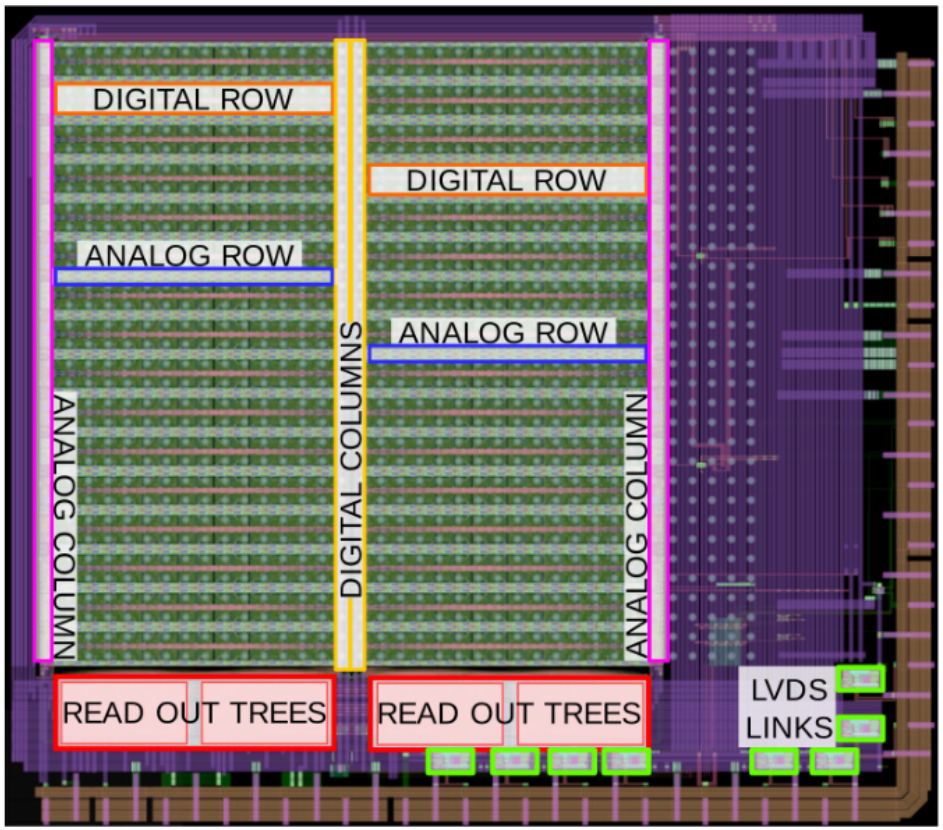
INFN workshop on Future Detector, IFD2022
17 October 2022

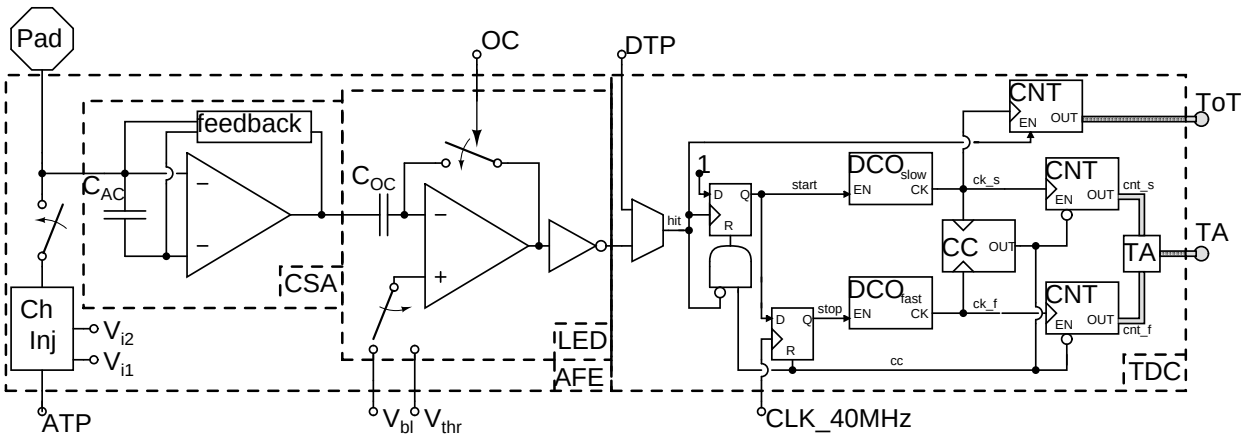
The ASIC



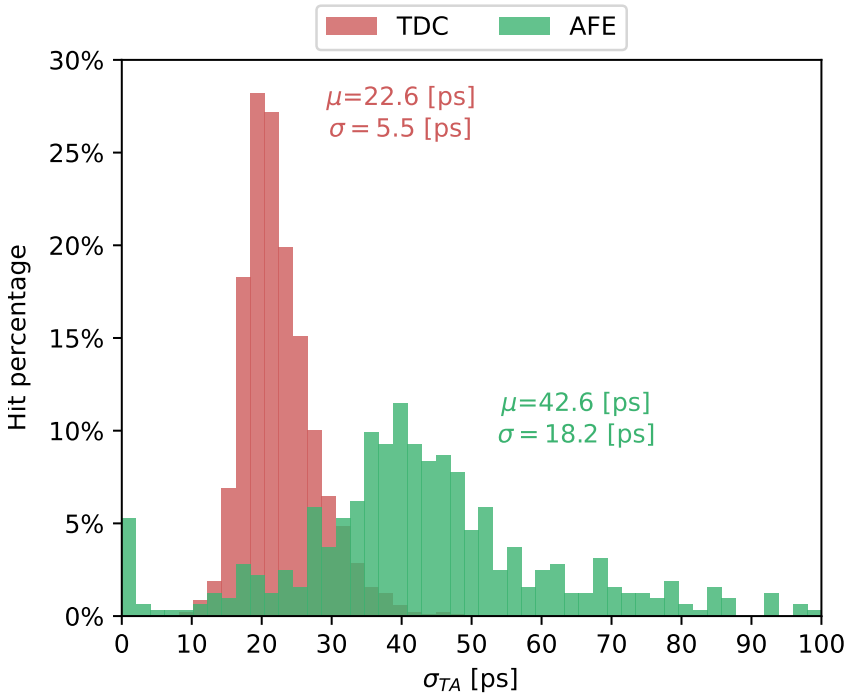


- 1024 channels organized in a 32×32 matrix of $55\,\mu m \times 55\,\mu m$ pixels ($2.6\,mm \times 2.3\,mm$)
- electronics pitch reduced in the horizontal direction ($50\,\mu m$) $\rightarrow$ insensitive area reduction
- Local timing measurement $\rightarrow$ 3 MHz peak hit rate per channel, 200 kHz average.
- Power consumption under $1.5\,W/cm^2$

Timing Performance



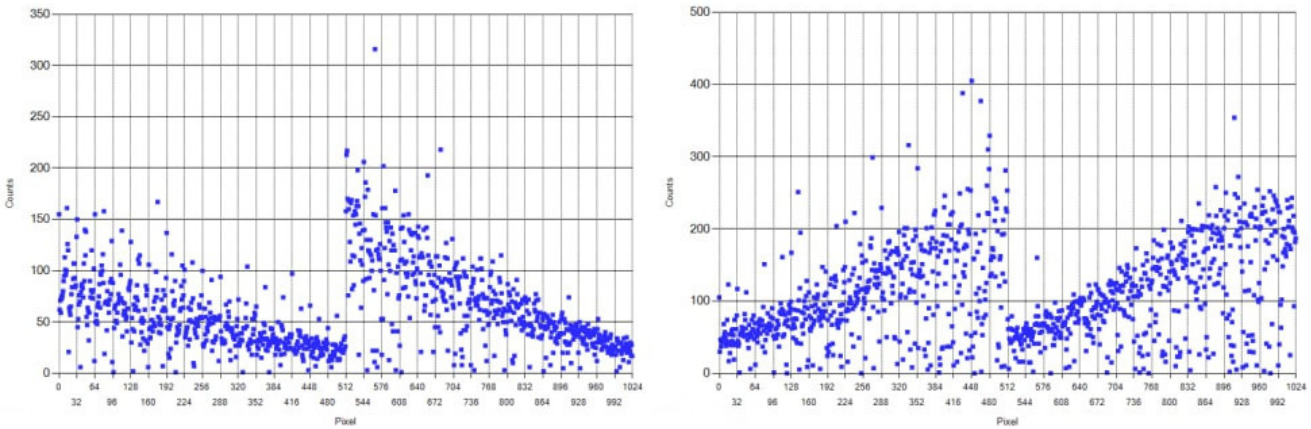
pixel architecture



Timing performance (electrical tests):

- CSA $\rightarrow$ < 20 ps
- Analog FE $\rightarrow \sim 50$ ps (Discriminator Issue)
- TDC $\rightarrow \sim 23$ ps

Future Prospects



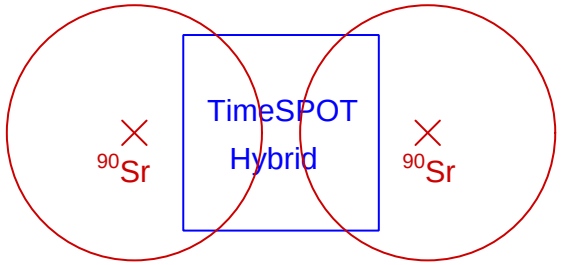
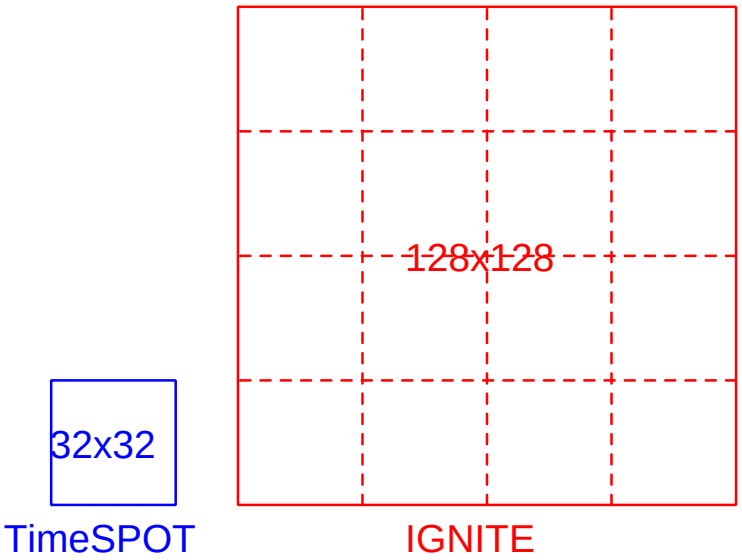


Figure: Hybrid test: off center ^{90}Sr source



- Hybrid tests: laser, radiation sources, test beam.
- New Version → IGNITE:
  - Scheme improvement and fixes → 20 ps resolution
  - x16 scale-up ($\sim 7\,\text{mm} \times 7\,\text{mm}$)
  - 3D integration (TSV)