ARCADIA

an INFN Design and Production Platform for Fully Depleted MAPS with a 110-nm CMOS Process

ARCADIA

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on behalf of the ARCADIA Collaboration

INFN
Istituto Nazionale di Fisica Nucleare

AIDA innova

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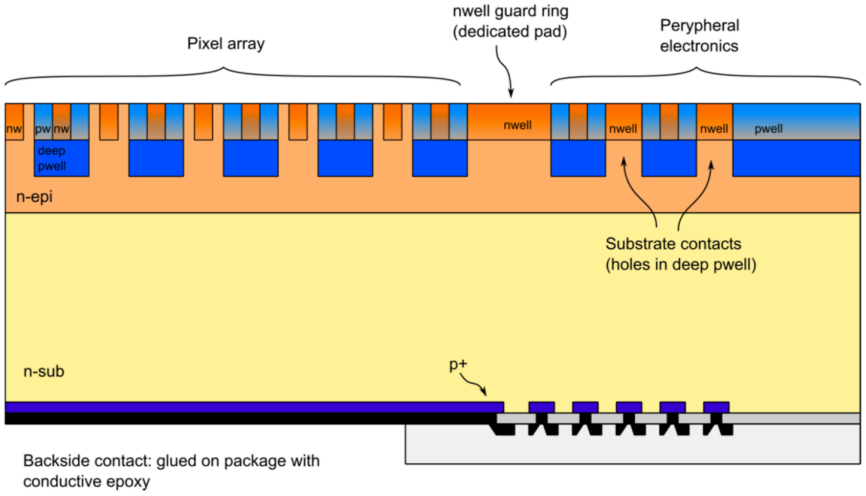
ARCADIA (INFN CSNV Call Project)

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

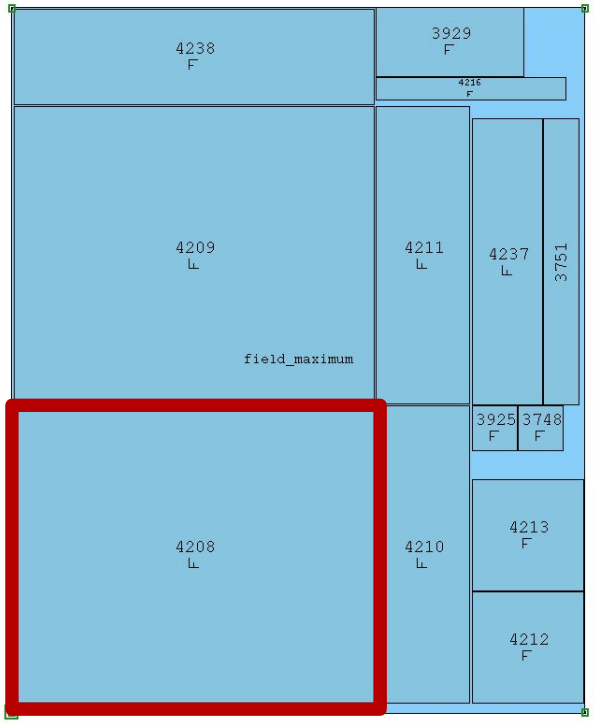
Fully Depleted Monolithic Active Pixel CMOS sensor technology platform allowing for:

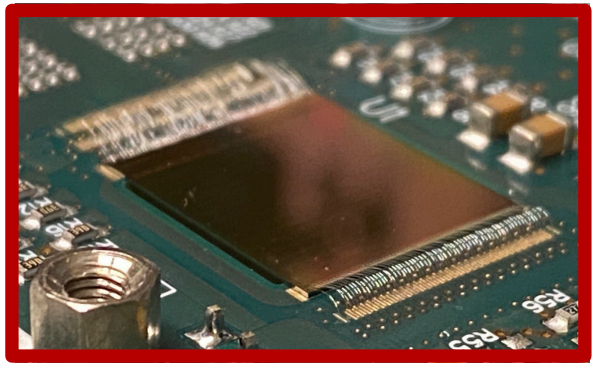
- Active sensor thickness in the range 50 µm to 500 µm or more;
- Operation in full depletion with fast charge collection by drift, small collecting electrode for optimal signal-to-noise ratio;
- Scalable readout architecture with ultra-low power capability (O(10 mW/cm2));
- Compatibility with standard CMOS fabrication processes: concept study with small-scale test structure (SEED), technology demonstration with large area sensors (ARCADIA)
- Technology: 110nm CMOS node (quad-well, both PMOS and NMOS), high-resistivity bulk
- Custom patterned backside, patented process developed in collaboration with LFoundry



"Fully Depleted MAPS in 110-nm CMOS Process With 100–300-µm Active Substrate," in IEEE Transactions on Electron Devices, June 2020, doi: 10.1109/TED.2020.2985639.

ARCADIA Technology demonstrators

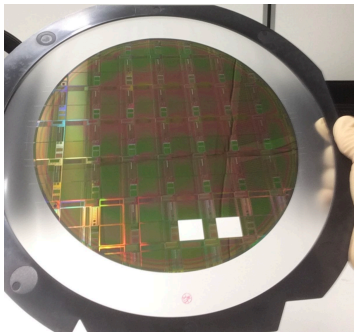


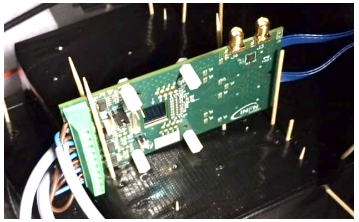


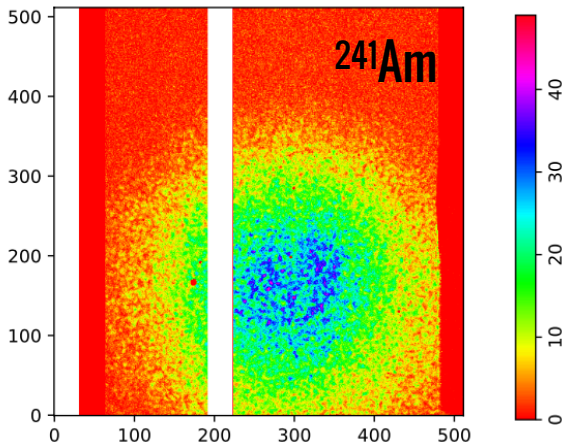
- **ARCADIA-MD1a**/b Main Demonstrator
- ARCADIA-miniD (debug)
- ARCADIA-miniD with on-chip LDOs for large-scale yield management
- MAPS and test structures for PSI (CH)
- MATISSE Low Power (ULP front-end for space instruments)
- pixel and strip test structures down to 10um pitch
- ASTRA 64-channel mixed signal ASIC for Si-Strip readout
- 32-channel monolithic strip and embedded readout electronics
- (LC2) MATISSE_TIMING: VFE for fast timing (R&D for ALICE3 timing layers)
- (LC3) Small-scale demonstrator of a X-ray multi-photon counter
- (LC3) Wafer splits with timing layer, new R&D towards <<100 ps timing performance: test structures and multi-pixel active demonstrator chip

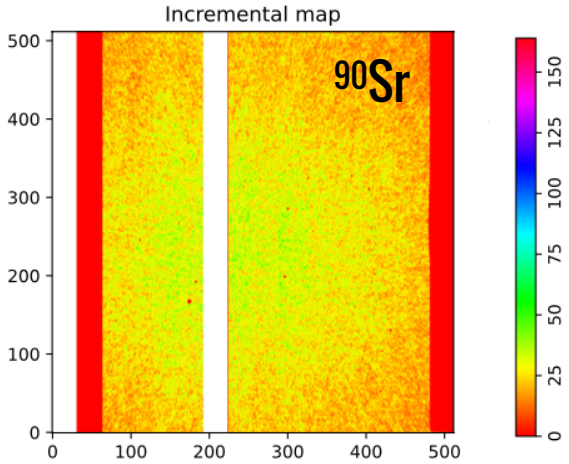
ARCADIA Design and Test Platform

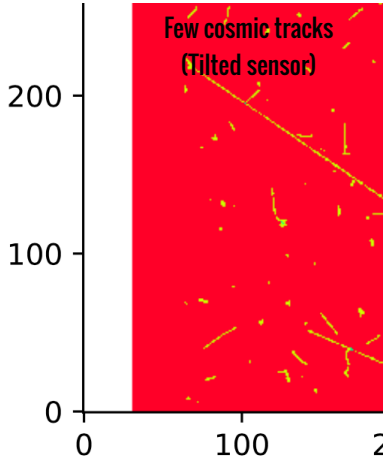
- **ARCADIA:** CMOS sensor design and fabrication platform with several groups working on:
  - Sensor R&D and Technology
  - CMOS IP Design and Chip Integration
  - Data Acquisition for electrical characterisation and beam tests with multi-chip telescopes
  - Radiation Hardness qualification
  - System-level characterisation for Medical (pCT), Future Leptonic Colliders and Space
- Allocated budget ≈ 1.4MEur (INFN and external funds) for 3 full SPW runs (2020-2022), 52 Members from 7 INFN Divisions. Moving from a CSN5 Call into RD_FCC, AIDAinnova, ALICE3.











Outlook: ARCADIA… or CMOS DMAPS in general

- **Monolithic active pixel sensors** are now ubiquitous in **HEP** trackers and are making their inception into (low-power) **space**, (high-rate) **medical** applications. Cost effective reticle scale sensors, compatible with standard CMOS fabrication, could pave the way to very large area tracking and timing detectors
- CMOS Depleted monolithic pixel (and strip) sensors are now a strong candidate both for future low material budget silicon trackers and for timing layers, with investment and R&D mostly focusing on:
  - very low-power architectures O (20 mW/cm^2)
  - process engineering for better time resolution O (100 ps) or better
  - larger and thinner chips towards all/only-silicon inner trackers
- We need to foster access to advanced technologies and foundries, and make a good use of the most advanced integration and industry standard wafer stacking/bonding techniques
- The federation of the activity on sensors and microelectronics, working alongside experts on detector, system integration and analysis will dramatically increase our scientific impact factor.