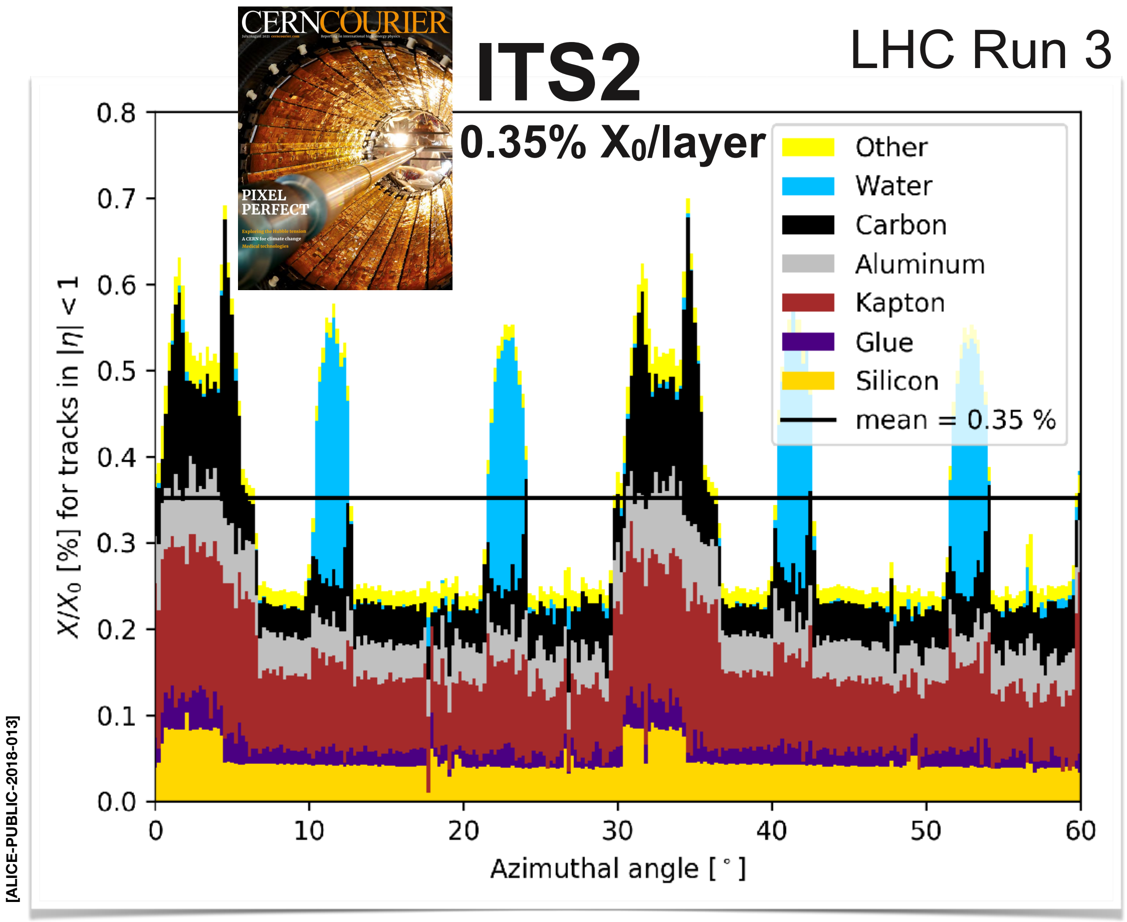
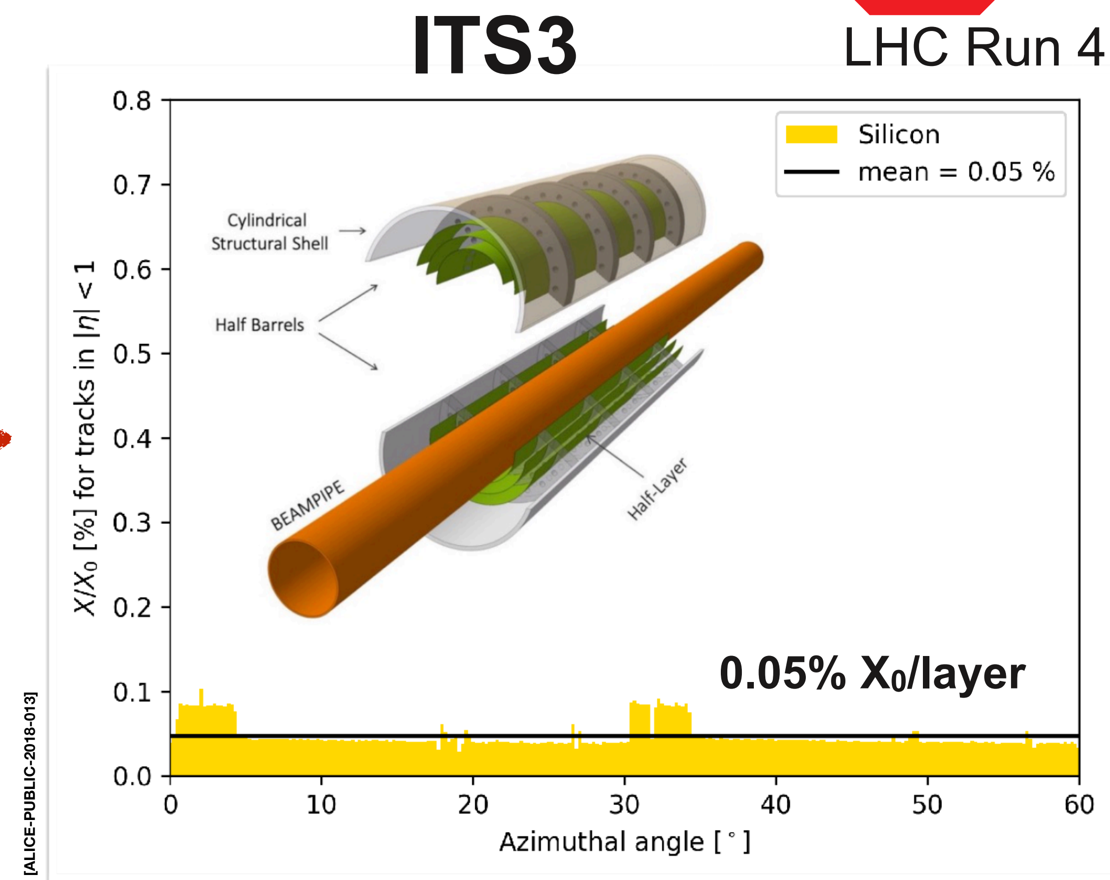
ALICE ITS3: motivation and detector concept





Requirements

» *Removal of water cooling*
  → **possible** if power consumption stays below 20 mW/cm^2
  → move to (low flow) air cooling system

» *Removal circuit board* (power+data)
  → **possible** if integrated on chip

» *Removal of mechanical support*
  → **benefit** from increased stiffness by rolling Si wafers

Key ingredients

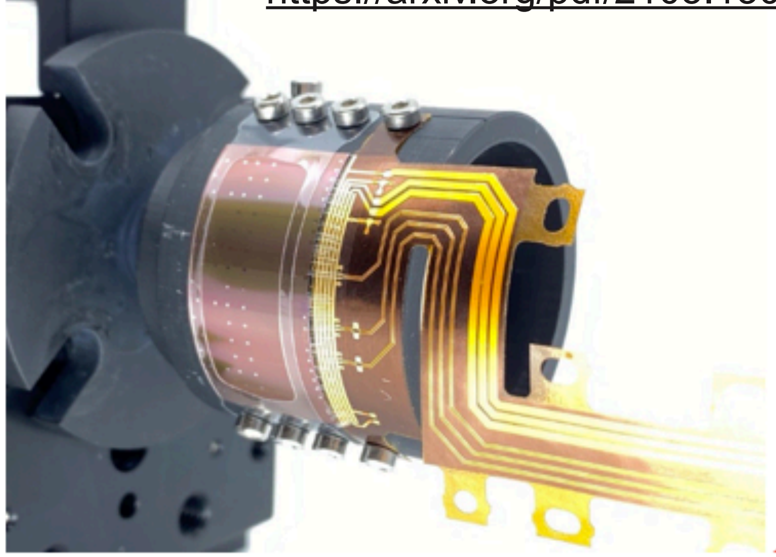
» Wafer-scale sensor fabricated using *stitching*
» Sensor thickness 20-40 μm
» Chips bent in cylindrical shape at target radii
» Si MAPS sensor based on 65 nm technology
» Carbon foam structures
» Smaller beam pipe diameter and wall thickness (0.14% X_0)

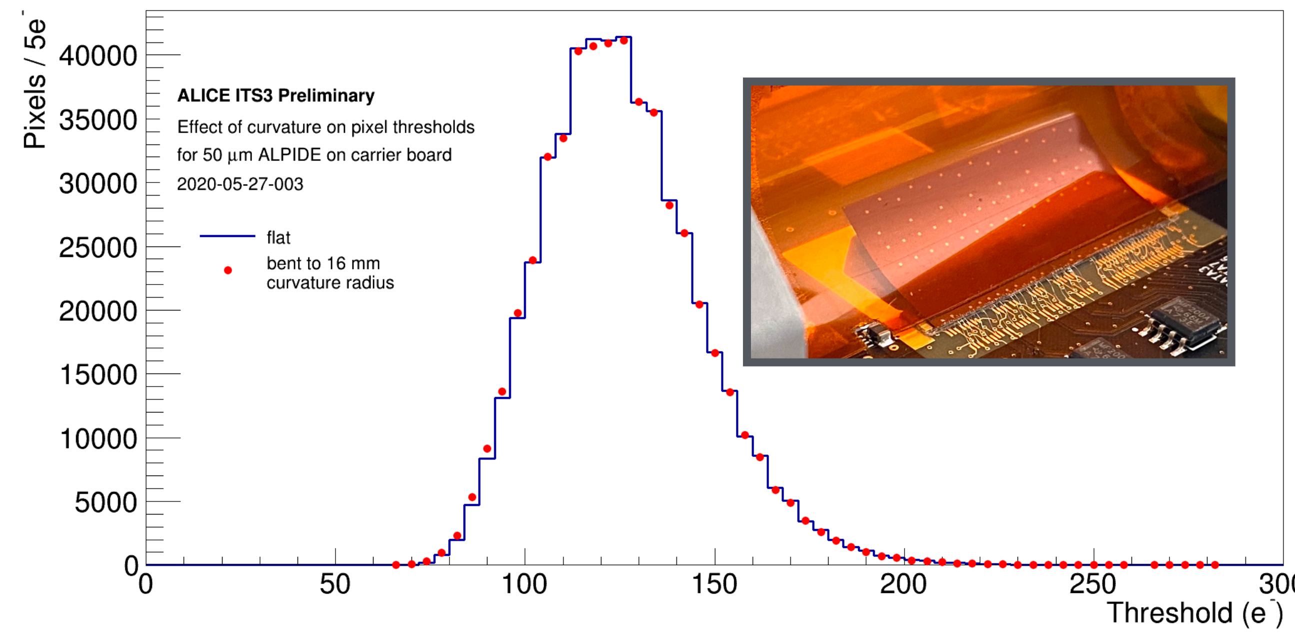
ALICE ITS3: R&D lines - Bent sensor performance

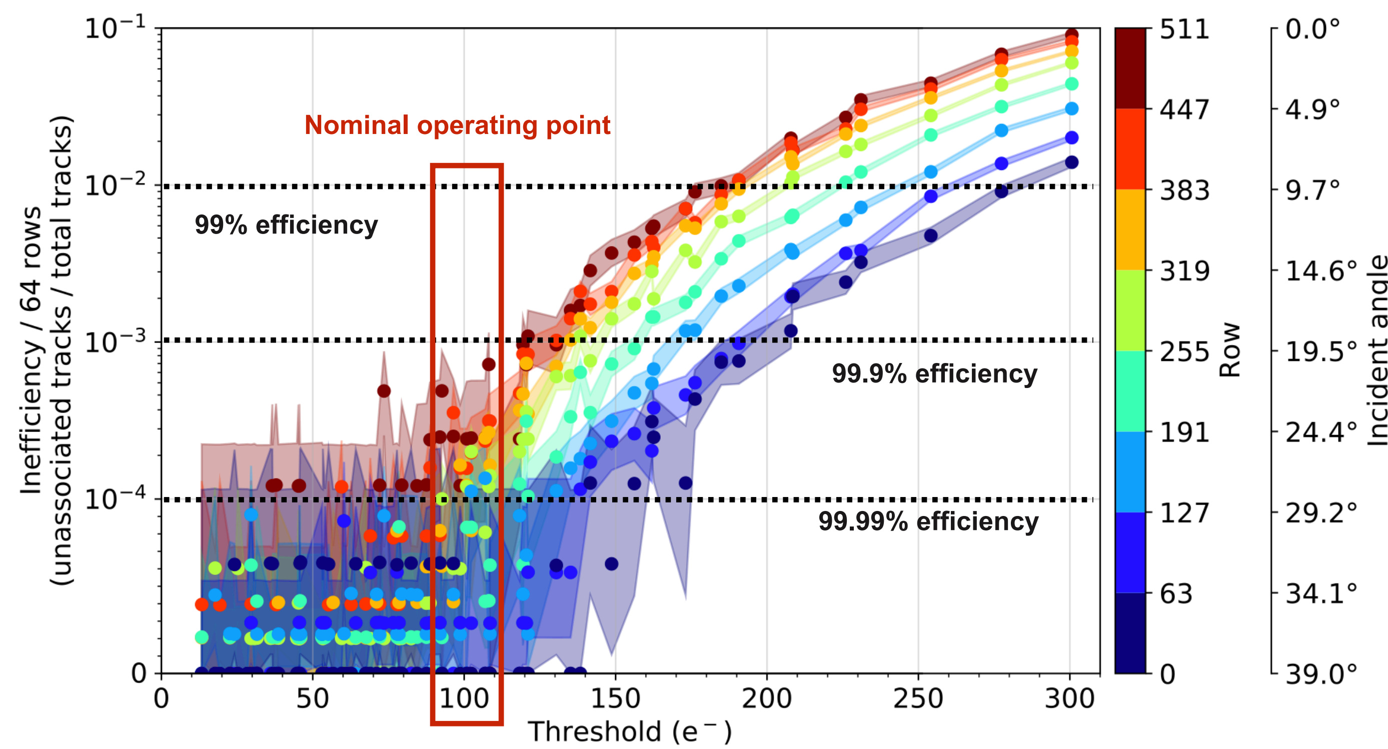
Bent ALPIDE

(MAPS used to assembly ITS2)

https://arxiv.org/pdf/2105.13000.pdf



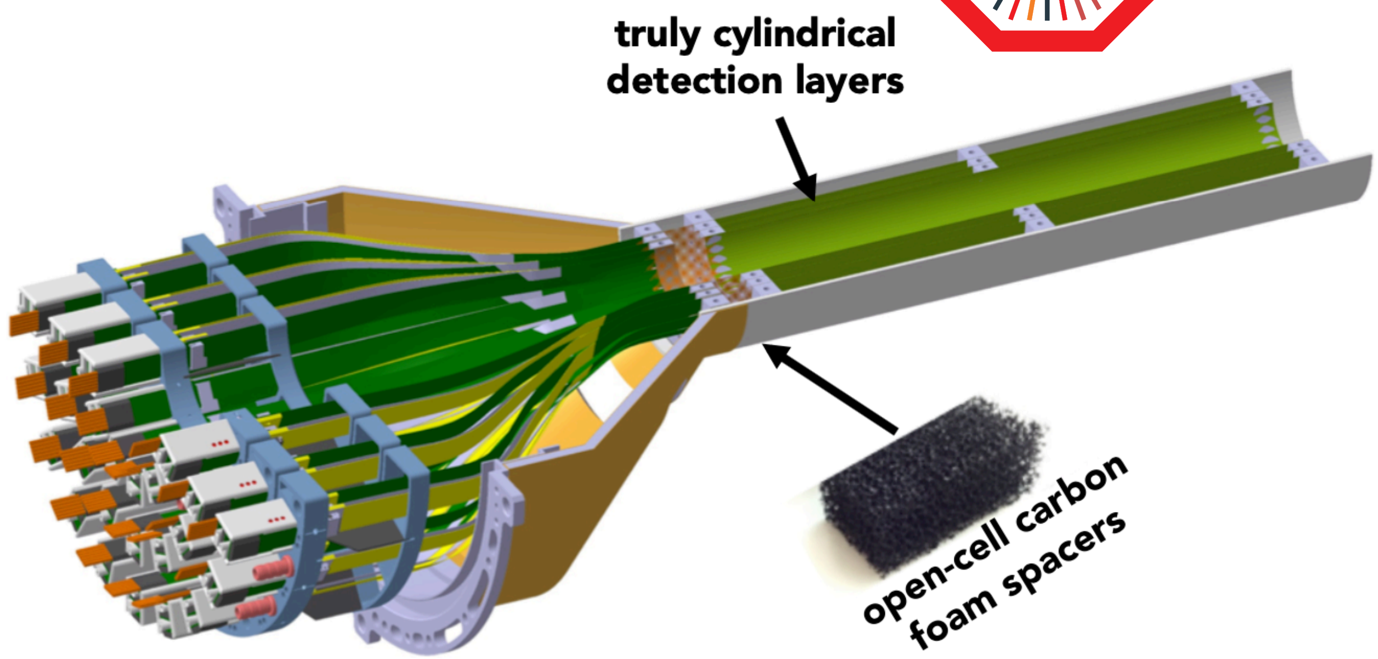




- **Sensor performance doesn't change after bending**
  - Pixel matrix threshold distribution does not change
  - Efficiency above 99.9% at a threshold of 100 e⁻ (nominal operating point)

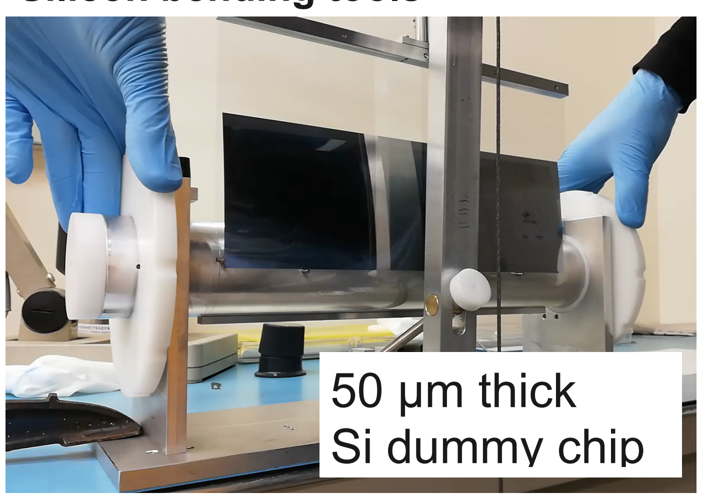
ALICE ITS3: R&D lines - Detector Integration

Beam pipe inner/outer radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length of sensitive area (mm)	300.0		
Number of sensors per layer	2		
Pixel size (µm²)	O (10 x 10)		

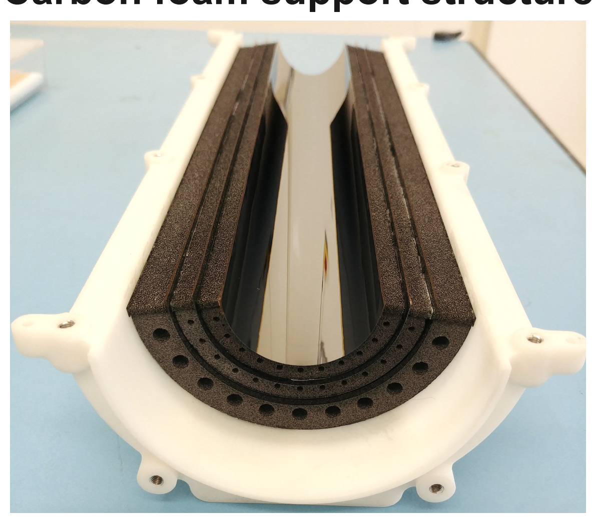


The whole detector will comprise six chips and barely anything else!

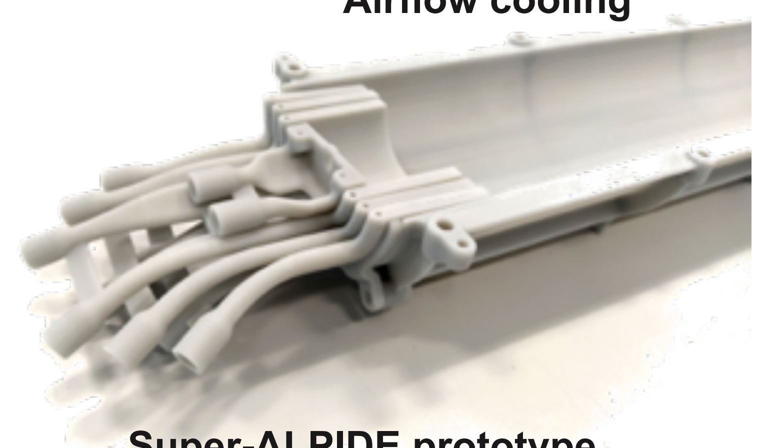
Silicon bending tools



Carbon foam support structure

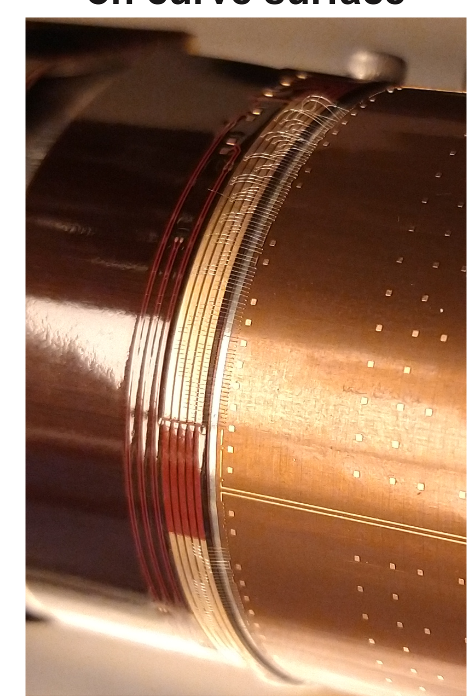


Airflow cooling



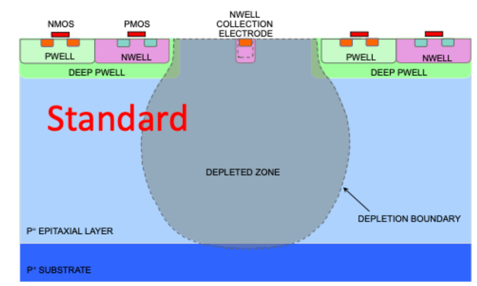
Super-ALPIDE prototype

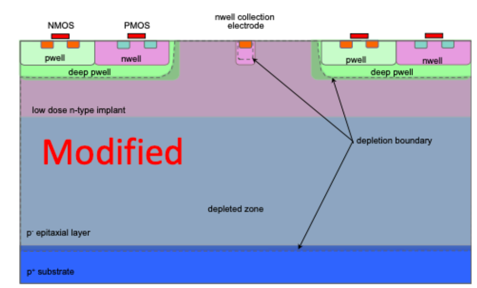
Wire-bonding on curve surface

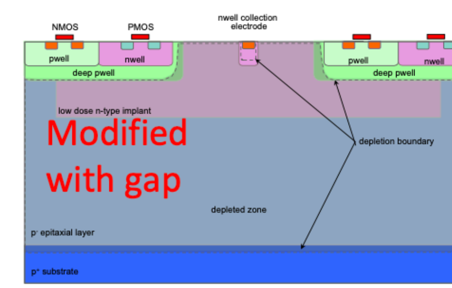


ALICE ITS3: R&D lines - Sensor design

» Tower Semiconductor (TPSCo) 65 nm CMOS IS technology
- TPSCo 65 nm continuation of the TowerJazz 180 nm (ITS2)
- scoped within CERN EP R&D WP1.2, significant drive from ITS3
- 300 mm wafers → 27 × 9 cm^2
- 7 metal layers
- Process modifications for full depletion:
  - Standard (no modifications)
  - Modified (low dose n-tope implant)
  - Modified with gap (low dose n-type implant with gaps)

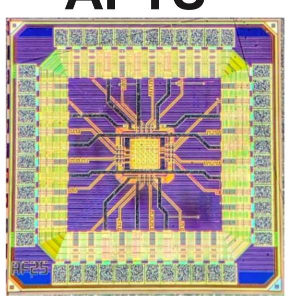






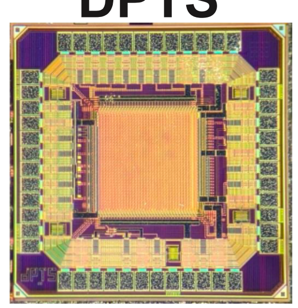
» **MLR1**: first test submission
- Main goals: learn technology features, characterise charge collection, validate radiation tolerance
- Submitted Dec. 2020 - Received Jul. 2021

APTS



Two output drivers:
- Traditional source follower (SF)
- Very fast OpAmp (OP)

DPTS



- 32 × 32 pixel matrix
- Asynchronous digital readout
- Tunable power vs time resolution

» **ER1**: first stitching implementation
- MOSS : focus on technology options, power distribution, signal routing, yield
- MOST : focus on yield with high density layout parts and fine power segmentation