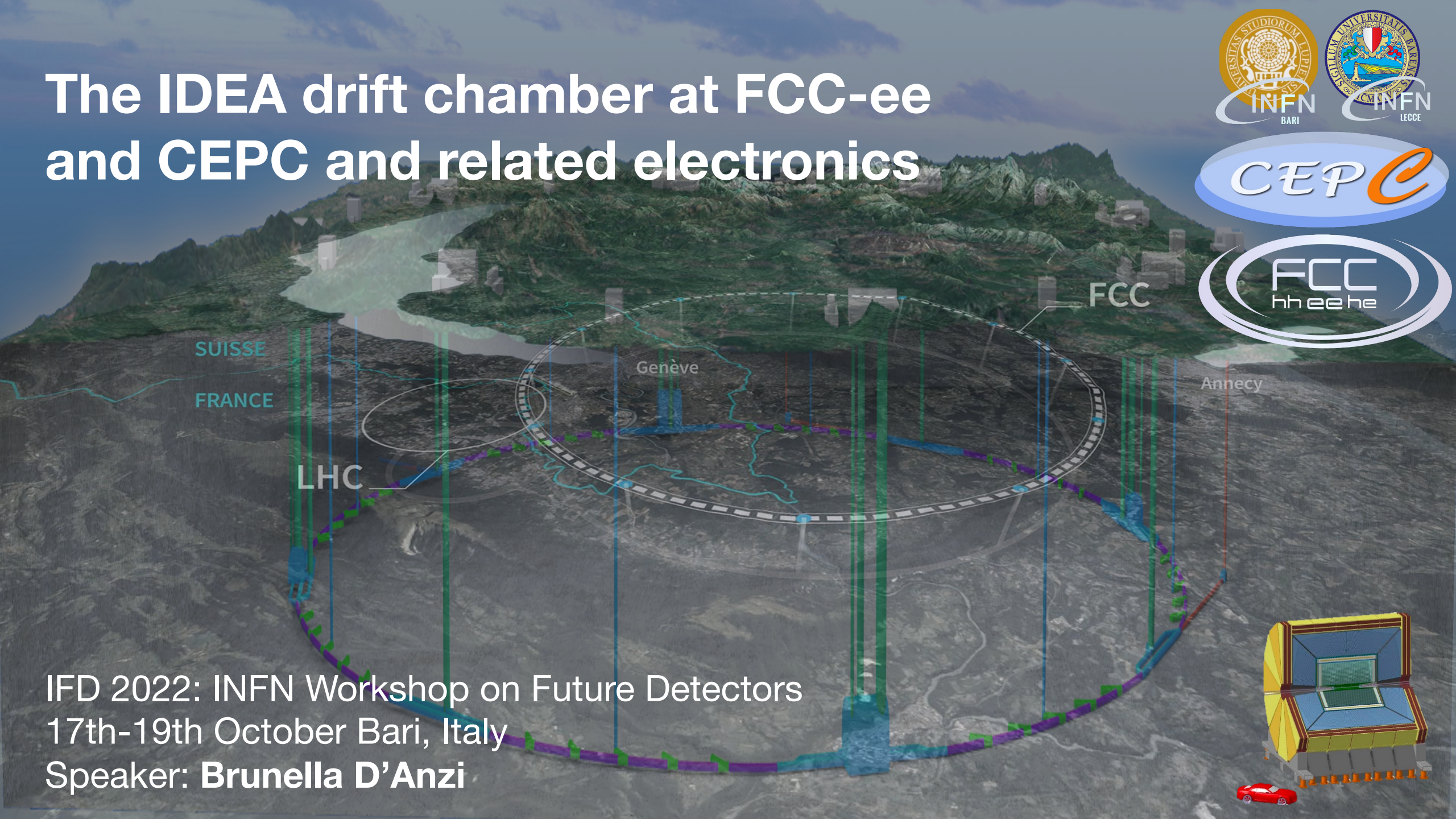
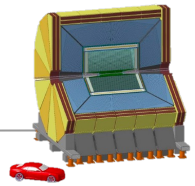
The IDEA drift chamber at FCC-ee and CEPC and related electronics



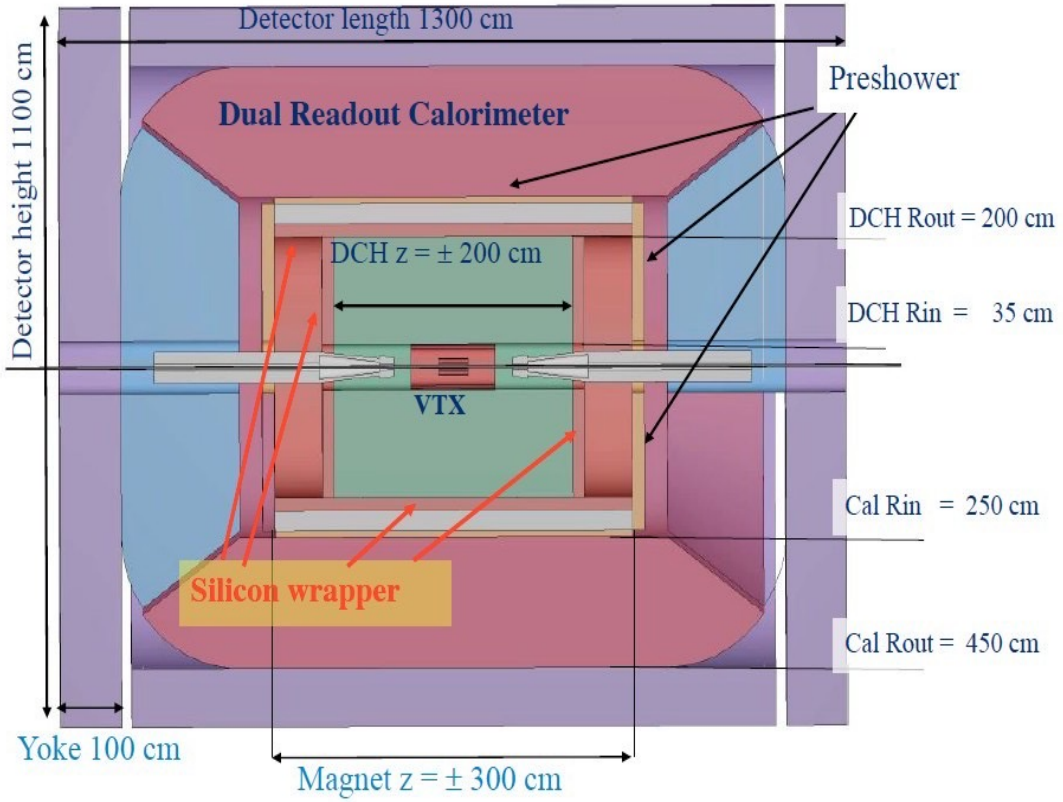
IFD 2022: INFN Workshop on Future Detectors
17th-19th October Bari, Italy
Speaker: **Brunella D'Anzi**

The detector concept IDEA

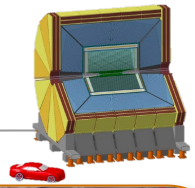


- The **IDEA** (**Innovative Detector for E+e- Accelerator**) **general-purpose detector concept** has been designed to study **electron-positron collisions** in a wide energy range provided by a very large (~**100 km**) circular leptonic collider (e.g. **FCC-ee** at **CERN, CEPC** in **China**) for **high luminosity Higgs**, **precision electroweak physics** at the **Z pole** and **flavour physics**.
- Its detectors sub-systems (**inside-out**) are:

  - **Silicon pixel vertex** detector
  - Large-volume, extremely-light, high transparency, high granularity **drift wire chamber (DCH)**
  - Surrounded by a layer of **silicon micro-strip detectors**
  - A thin low-mass **superconducting solenoid coil**
  - A preshower detector based on **μ-WELL technology**
  - A **Dual Read-out calorimeter**
  - Muon chambers inside the magnet return yoke, based on **μ-WELL technology**
  - Low field detector solenoid (optimized at 2 T) **to maximize luminosity**

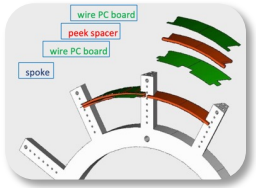


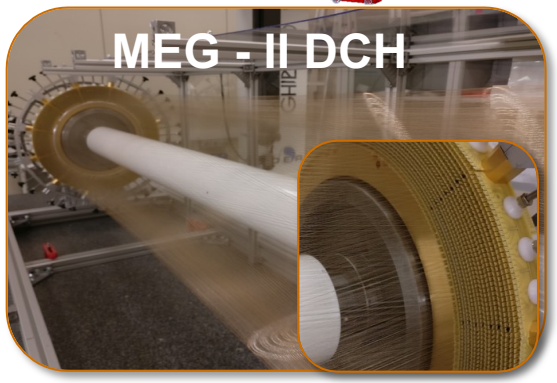
The IDEA drift chamber (DCH)

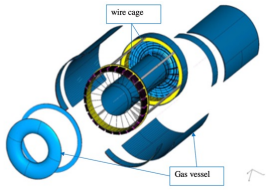


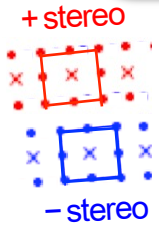
Goal: efficient tracking + high precision momentum measurement + excellent particle identification by applying the **Cluster Counting (CC) technique** (more details in the Talk *The cluster counting/timing techniques in drift chambers*).

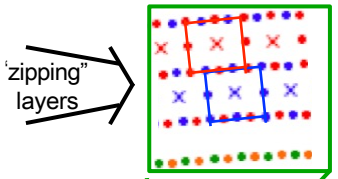
- New **concept of construction** allows to reduce material to **≈ 10^{-3} X_0** for the **barrel** and to a **few x 10^{-2} X_0** for the **end-plates.**
- The **wire net** created by the combination of + and - orientation generates a **more uniform equipotential surface.**
- High wire number requires a **non standard wiring procedure** and needs a **feed-through-less wiring system** already developed for the construction of the ultra-light MEG-II drift chamber.

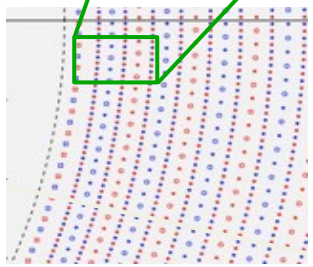




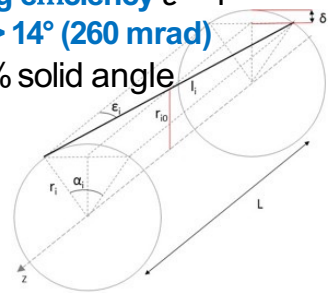


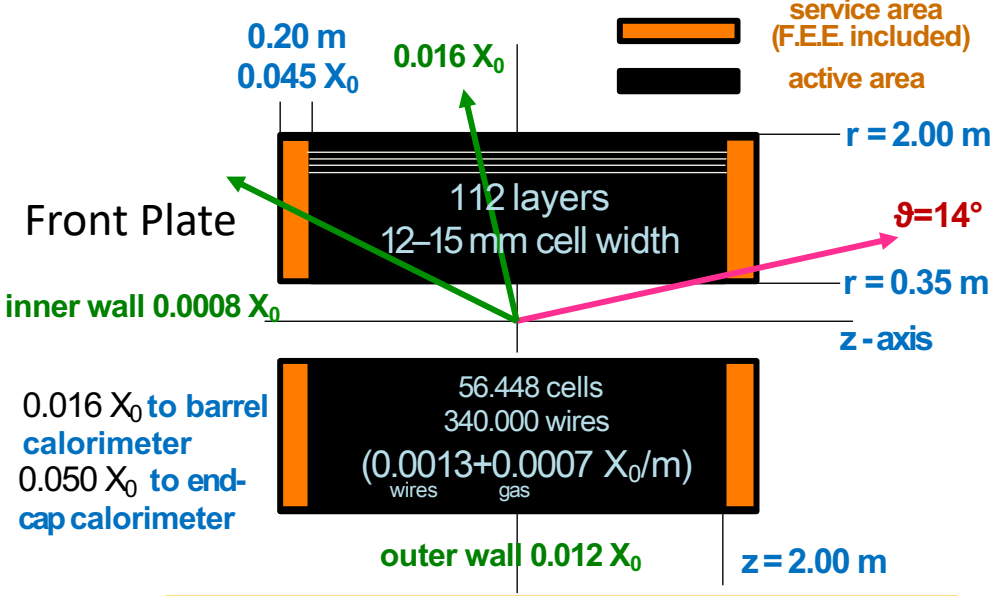






tracking efficiency ε ≈ 1 for $\vartheta > 14°$ (260 mrad) 97% solid angle



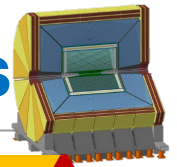


sense wires: 20 mm diameter W(Au) => 56.448 wires
field wires: 40 mm diameter Al(Ag) => 229.056 wires
f. and g. wires: 50 mm diameter Al(Ag) => 58.464 wires
► **343.968** wires in total

IDEA DCH parameters

- **Gas mixture:** Helium-based
- 12 ÷15 mm wide **square cells** 5:1 field to sense wires ratio
- 4 m long, a_{xy} < 100 μm, a_z < 1 mm, **drift length (time)** ~1 cm (150 ns), **rise time signals** ~1 ns
- 14 co-axial super-layers, 8 layers each (**112 total**) in 24 equal azimuthal (15°) sectors ($N_i = 192 + (i - 1) \times 48$)
- **alternating sign stereo angles** ranging from 50 to 250 mrad

Data reduction and pre-processing of DCH signals



High speed digitization (2 GSa/s) for CC ⟹ Transfer rates in excess of TB/s at the Z–pole running

- **Data reduction strategy:** transfer, for each hit drift cell, only the minimal information relevant to apply the **Cluster Counting/Timing (CCT) techniques**, i.e. the **amplitude** and the **arrival time of each peak** associated with **each individual ionization electron** ⟹ **CCT algorithms!**

  ► Use of a **FPGA** for the **real-time data analysis** of drift chamber signals **digitized by an ADC.** Acquire the signals converted ⟹ process with cluster counting algorithms (aimed also at **reducing the data throughput**) ⟹ send the processed information to a back-end computer via an Ethernet interface.

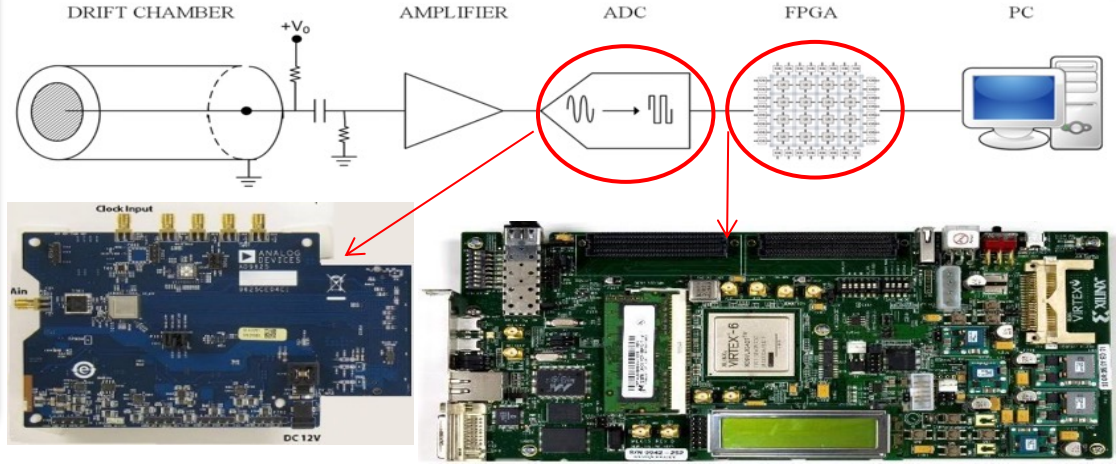
- A fast read-out CCT algorithm has been developed as **VHDL/Verilog** code implemented on a **Virtex 6 FPGA** (**maximum input/output clock switching frequency** of **710 MHz**). The hardware setup includes also a **12-bit monolithic pipeline sampling ADC** at conversion rates up to **2.0 GSPS.**

Goal

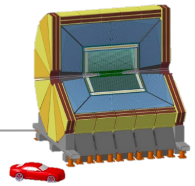
To implement on FPGA more sophisticated peak finding algorithms for the **parallel pre-processing** of **many ADC channels**:

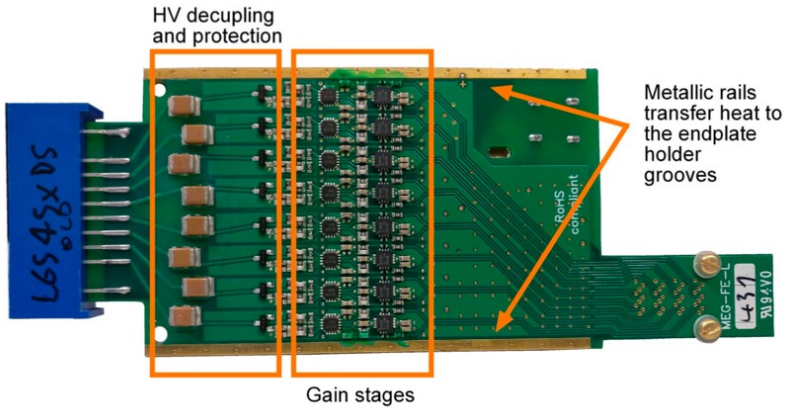
- **reduce costs** and **system complexity**
- **gain on flexibility in determining proximity correlations** among hit cells for track segment finding and triggering purposes.

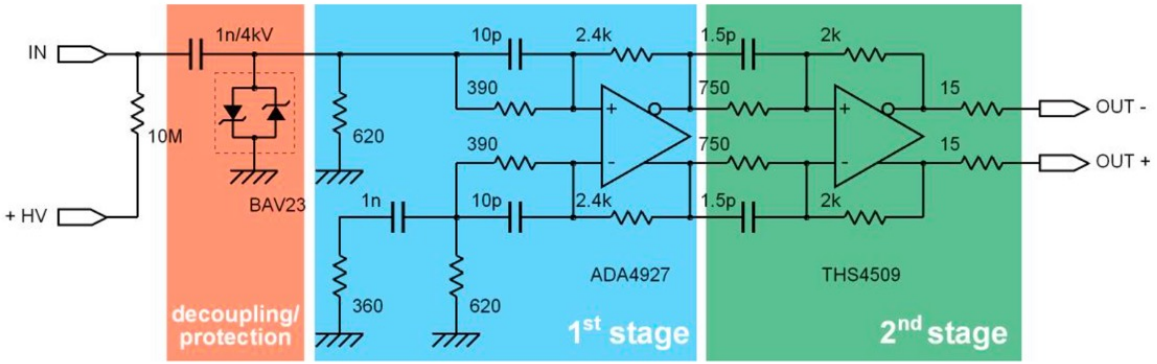
Implemtend using a **single channel ADC**



The read-out for DC (1/2)





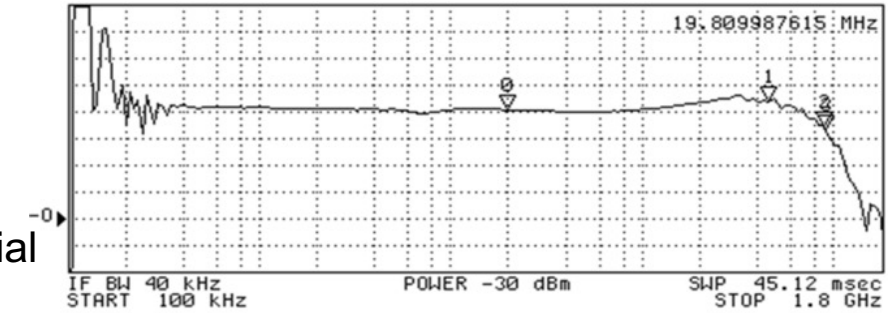


Amplifier used in MEG-II Cylindrical DCH

- **Two stage amplifiers** based on commercial devices:
  - **ADA4927 (AD) Ultralow distortion** current feedback
  - **THS4509 (TI)** Wideband **low noise** fully differential amplifier (driver for the ADC)

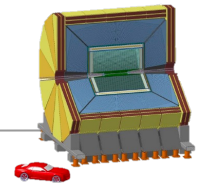
- **Pre-emphasis implemented** on both stages to balance the attenuation of output cable
- High overall bandwidth (F.E. input to DRS WD input): **~1 GHz**
- Low power: **50 mW @ ±2V**

Gain and Bandwidth after cable



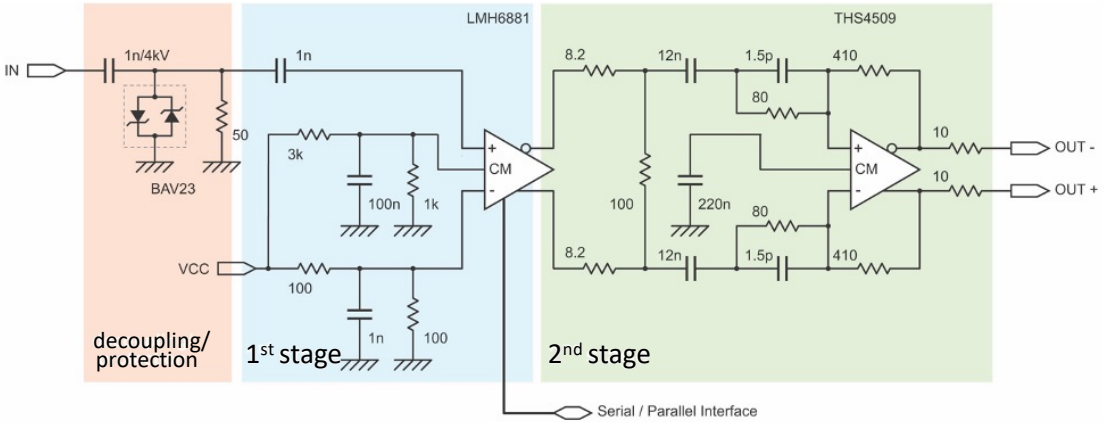
N	SWP PARAM	VAL
0	19.809987615 MHz	20.279 dB
1	456.600249532 MHz	21.773 dB
2	884.527480154 MHz	17.094 dB
3	899.750691731 MHz	16.686 dB

The read-out for DC (2/2)

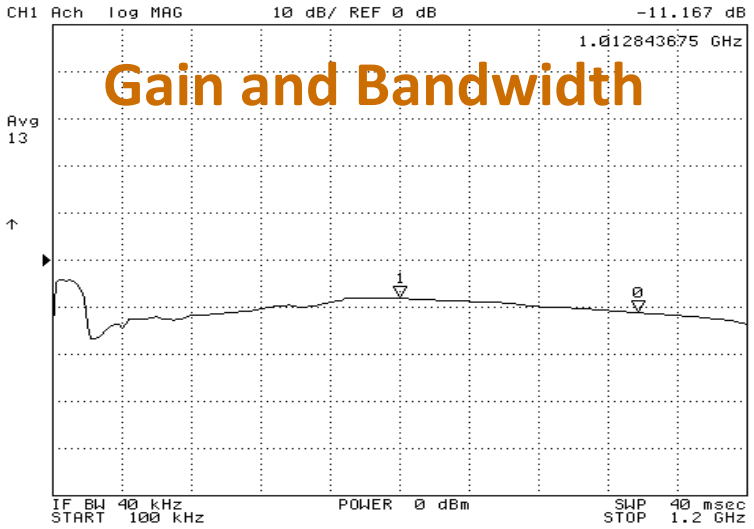


New Amplifier

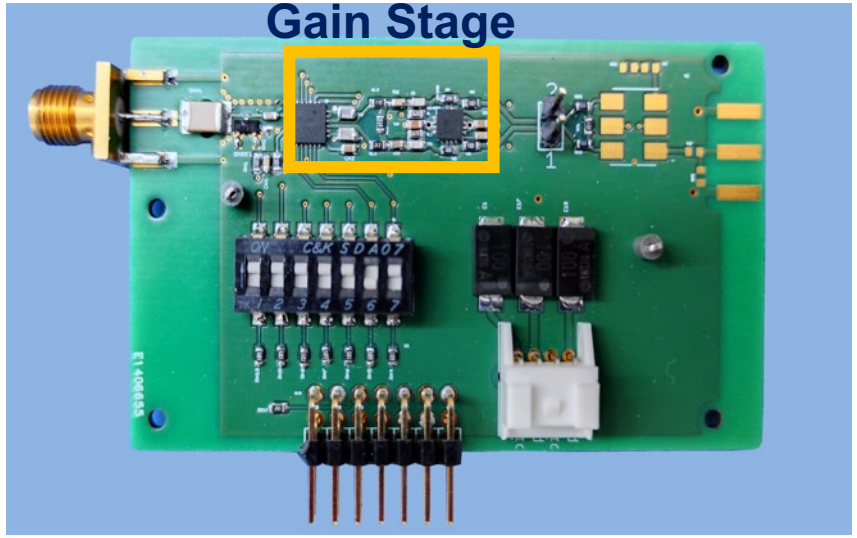
- Two stage amplifiers based on commercial devices:
  - **Variable gain LMH6881** is a high-speed, high-performance fully differential programmable amplifier (remote control via SPI)
  - **THS4509 (TI)** Wideband low noise fully differential amplifier



- The gain stage supports **gain settings** up to about **50 dB** with small accurate **0.25 dB gain steps**. The VGA can be also parallel programmed.



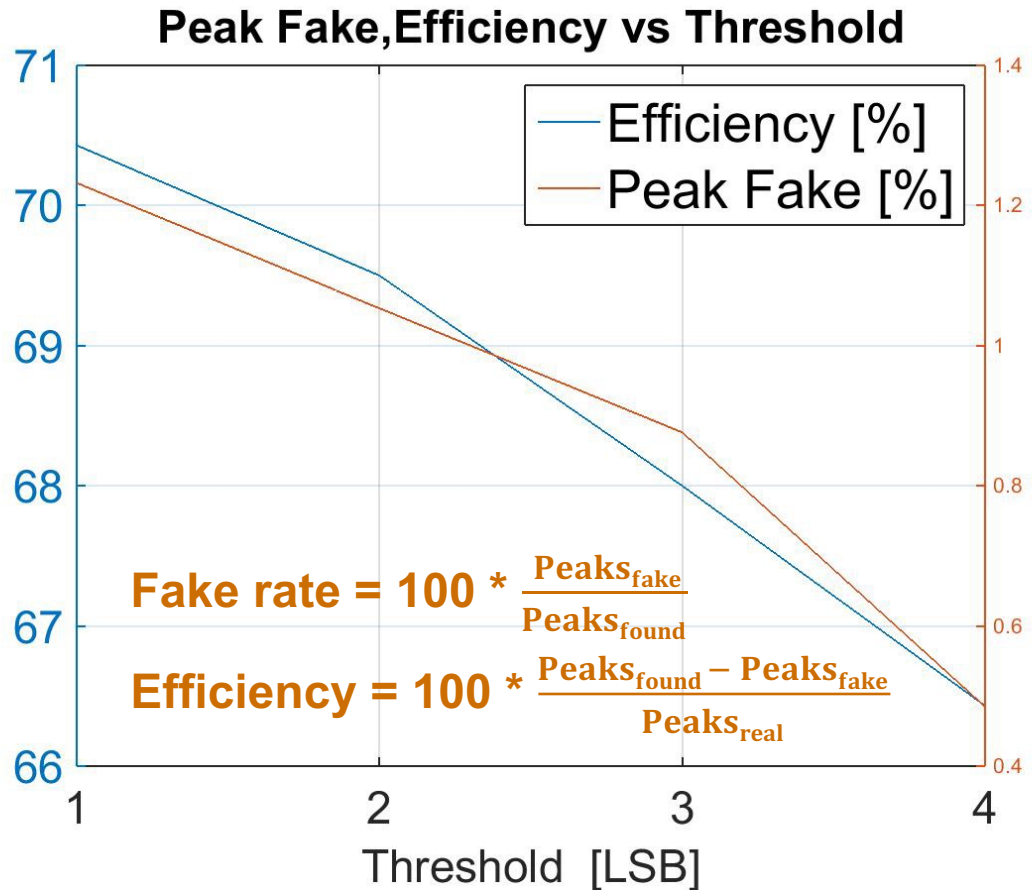
Prototype PCB



Mode/Gain programming. Through these dip switches it is possible to select the way to **control the gain of the first stage**, serial or parallel, in the **20 dB ÷ 49 dB** range.

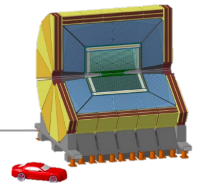
Single-channel ADC results

The CCT algorithm (DERIV) performances on FPGA

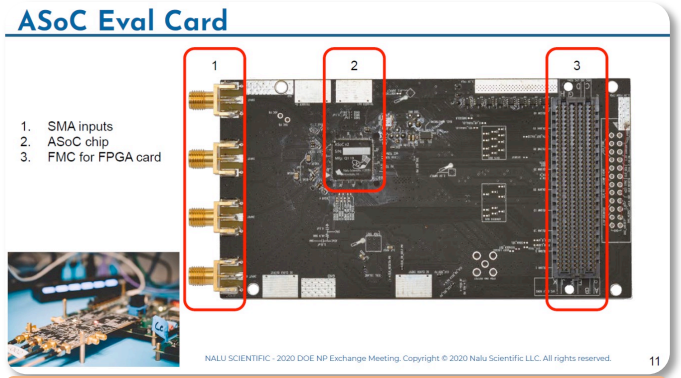


- Efficiency can be improved by using a **higher resolution ADC**
  - To recognize **smaller peaks.**
  - To increase the signal to noise ratio by filtering and amplifying the analog input signal.
- Using an **FPGA** with **better** performances (**temporal and powering**) allows us to reduce the **processing time** and manage **multichannel ADCs**.

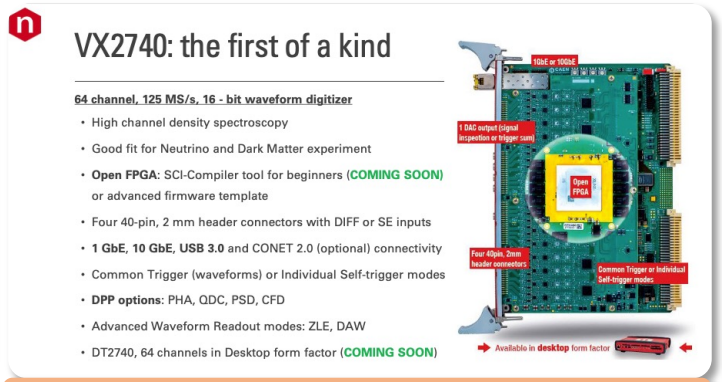
Conclusions and future strategy



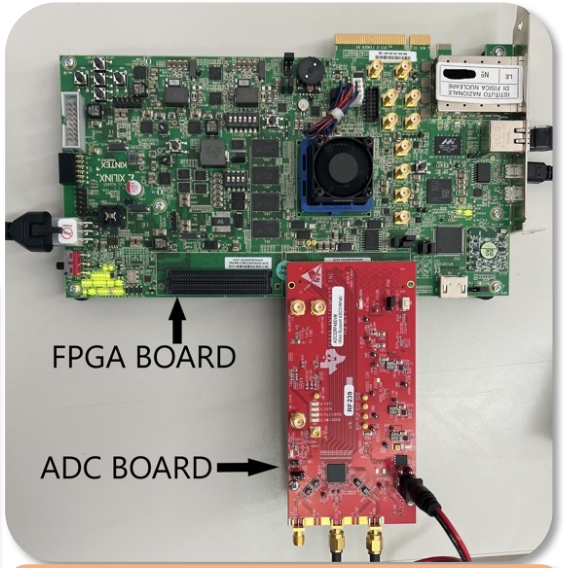
- We implemented successfully the CCT technique on **a single-channel ADC**
- To implement the **multi-channel DCH signals** reading, different digitizers are under test:
  1) ADC TEXAS INSTRUMENT **ADC32RF45**
  2) CAEN **digitizer**
  3) NALU SCIENTIFIC **ASoCv3**



4 Channel and Analog Bandwidth 850 MHz



OPEN FPGA system

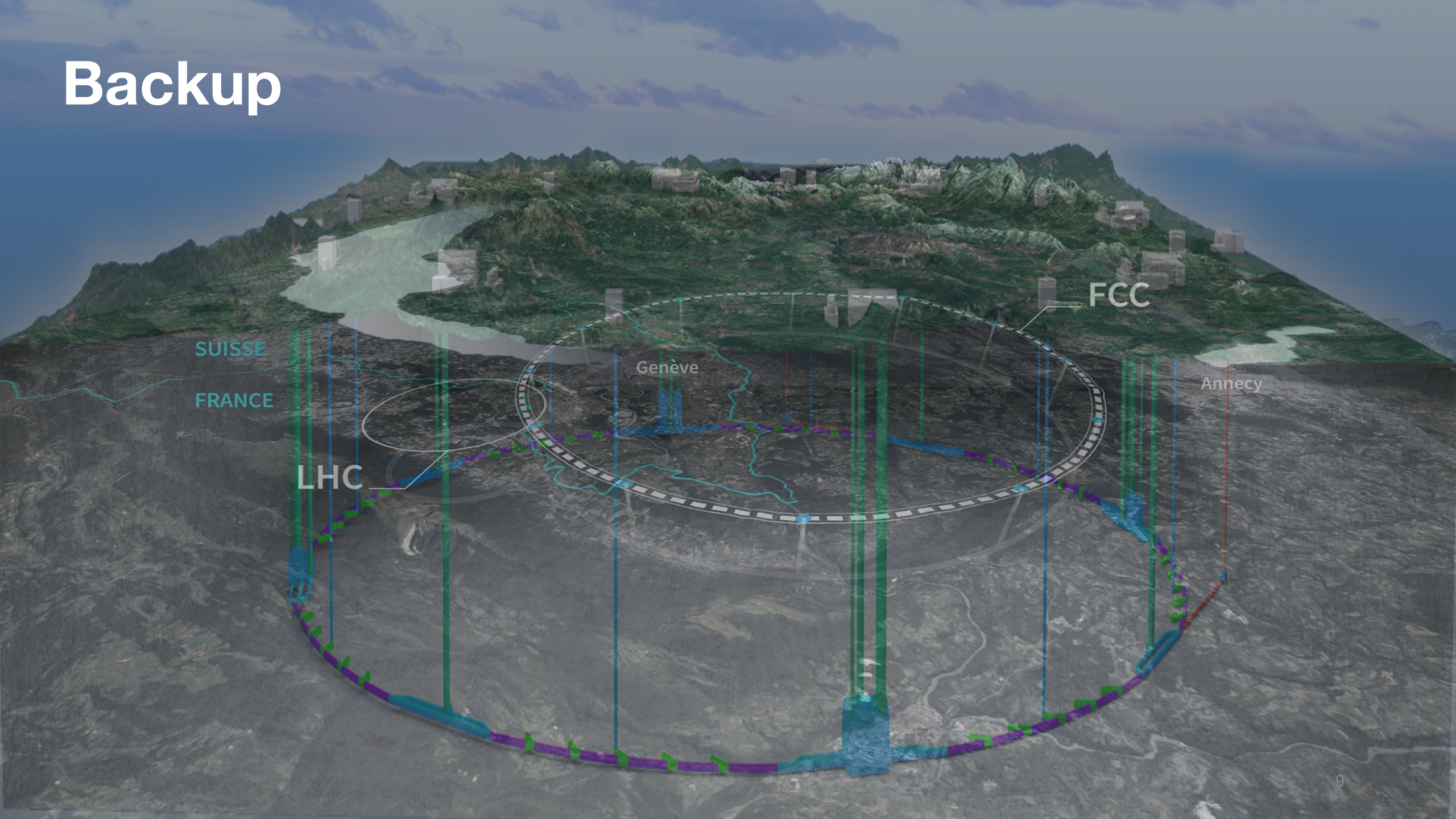


Xilinx Kintex UltraScale **FPGA** KCU105 Evaluation Kit **+ ADC dual channel** ADC32RF45EVM

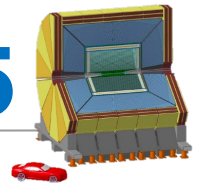
- Understand how to best implement the data transfer to the DAQ, using **optical fiber with SFP + connectors** or **SFP + to RJ45 adapters** to use the new **10Gbit/s standard** (especially for (1) and (2)).

- Investigate the best way **to save information before the transfer** (we need it if a bottleneck during the transfer happens).

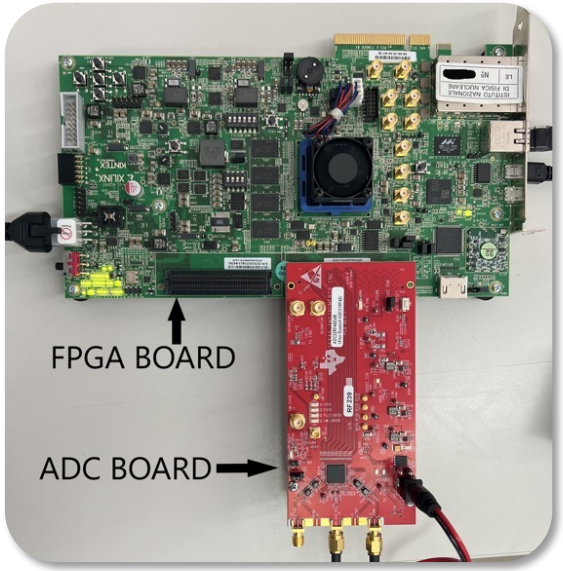
Backup



ADC TEXAS INSTRUMENT ADC32RF45



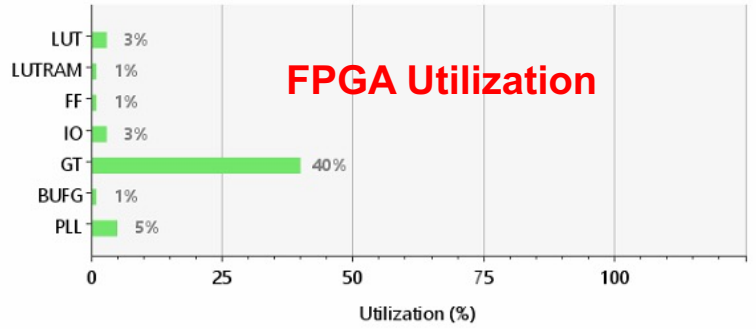
- The new hardware to test the algorithm is:
  - **Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit**
  - **ADC dual channel ADC32RF45EVM**



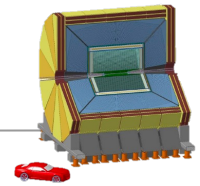
- The choice of the FPGA and ADC was made by choosing the **ADC** that ensured **good resolution** and **transfer capacity**.

- The new FPGA allows to have **better time constraints**.

- The ADC has a **higher resolution** than the previous one and also it allows the reading of **two channels simultaneously.**

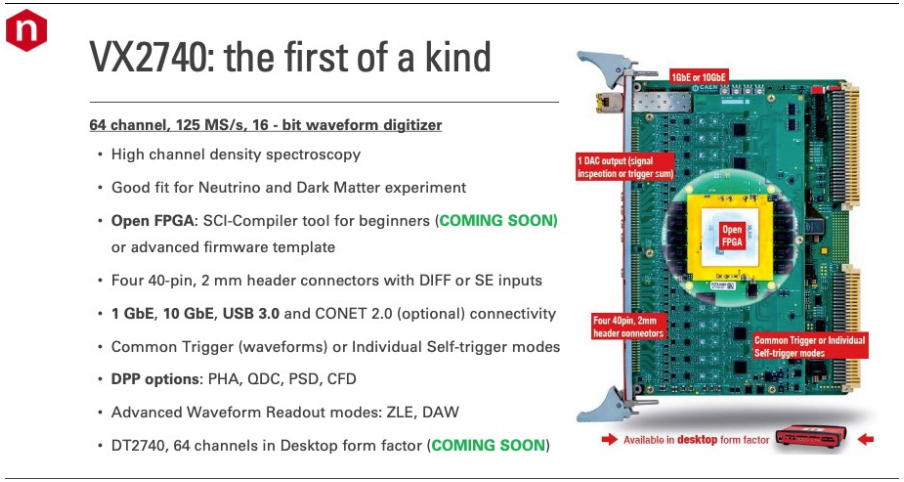


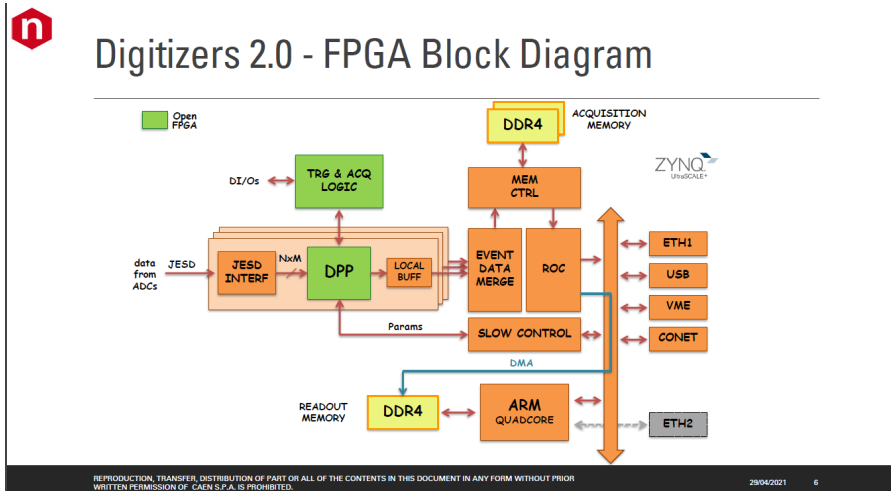
CAEN digitizers



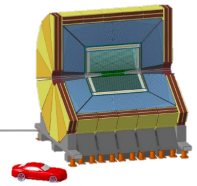
- Test with the **new high performance CAEN digitizers**:
  - start testing their **lower performance digitizer VX2740** (waiting for the **board VX2751**)
  - Use the **"OPEN FPGA" system**

- Using the CAEN HW we do not have access to the **whole firmware infrastructure** but only in the **green areas** (in the figure), where we will implement the cluster counting algorithm.





Contact with Caen



Model	# channels	MS/s	# bit	Applications
x2740	64	125	16	64 MCAs for high channel density spectroscopy Good fit for Neutrino and Dark Matter exp.
x2745 Advanced version of x2740	64	125	16	Variable gain input stage Designed for Si detectors readout
x2725/x2730	32	250/500	14	Medium-fast detectors Sub-ns timing combined with high energy resolution Optimal trade off between cost and performances
x2751	16	1000	14	Ultra-fast detectors (diamond, MPCs, SiPMs) with ps timing application Potential upgrade to higher sampling rate
x2724	32	125	16	Spectroscopy & MCA Advanced Front-End (gain, shaping, AC/DC coupling …) Semiconductor detector (HPGe, Clover, SDD ,…) Typically connected to charge Sensitive Preamplifier

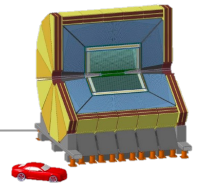
available

COMING SOON

Target Digitizer

Birdseye view – what's coming

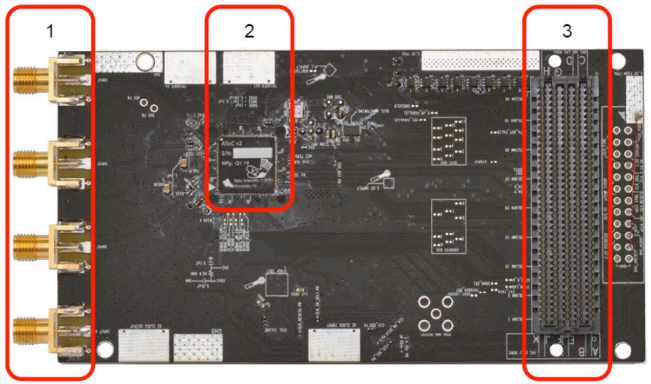
Naluscienfic ASoCV3 (1/2)

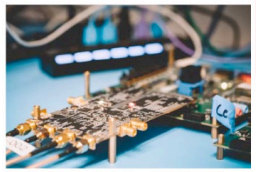


- Naluscientific is providing us the card with the **ASoCV3 chip**:
  - **4 channel**
  - **Analog Bandwidth 850 MHz**

ASoC Eval Card

1. SMA inputs
2. ASoC chip
3. FMC for FPGA card





NALU SCIENTIFIC
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ASoC V3 DESIGN DETAILS

Compact, high performance waveform digitizer

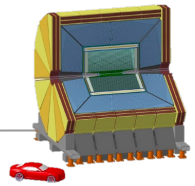
- High performance digitizer: 3+ Gsa/s
- Highly integrated
- Commercially available, low cost, patented design
- 5mm x 5mm die size

Parameter	Spec
Sample rate	2.4-3.6GSa/s
Number of Channels	4
Sampling Depth	16kSa/channel
Signal Range	0-2.5V
Number of ADC bits	12 bits
Supply Voltage	2.5V
RMS noise	~1.5 mV
Digital Clock frequency	25MHz
Timing resolution	<25ps (see below for details)
Power	120mW/channel
Analog Bandwidth	850MHz
Serial interface	Up to 500 Mb/s***

- Calibration memory access
- PLL on chip
- Isolated analog/digital voltage rings
- Serial interface
- Self triggering
- Completed DOE Phase II SBIR
  - Eval cards avail
  - Custom boards under dev

IEEE NSS 2021

Naluscienfic ASoCV3 (2/2)



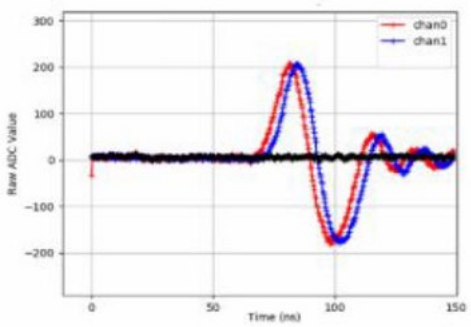
- Some **performances of the tests** made by Naluscientific on the **old-version chip V2**

NALU SCIENTIFIC
ENABLING INNOVATION

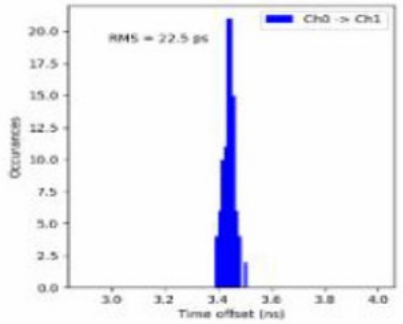
ASoC V2* MEASUREMENTS

*V3 under test

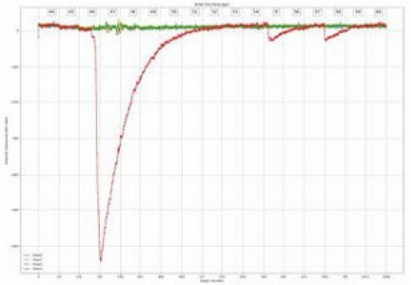
Live demo at IEEE NSS-MIC 2019



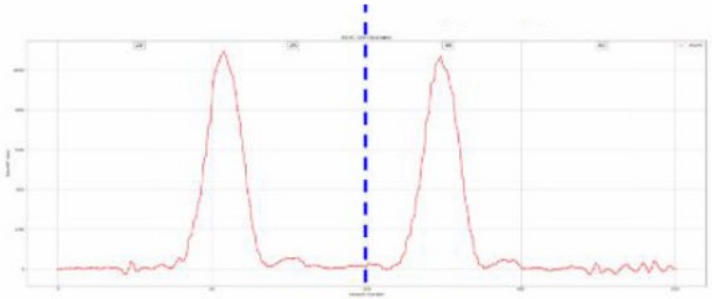
Timing resolution: 22ps

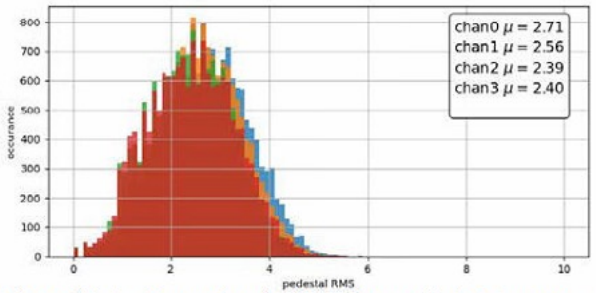


SiPM waveform readout



ROI Readout





Noise residuals after pedestal subtraction - typical ~2.5 counts = 1.0mV