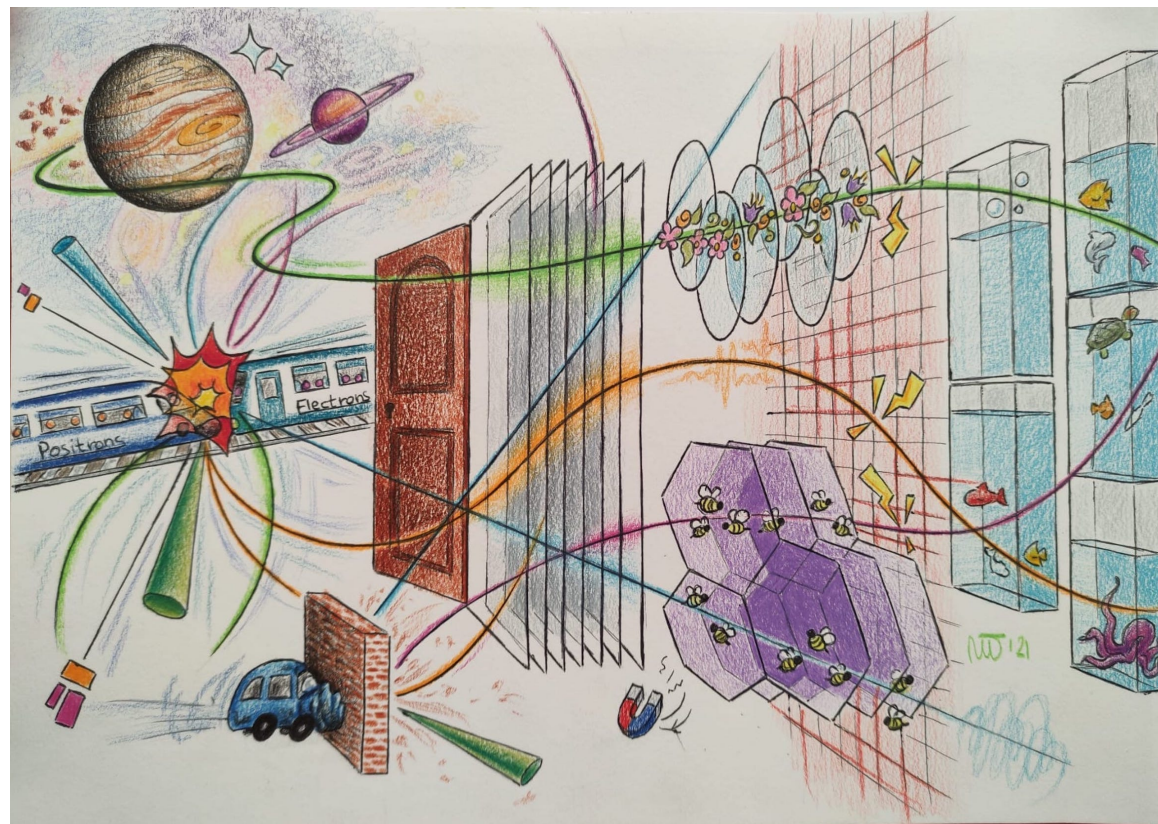


Solid State detectors for particle tracking

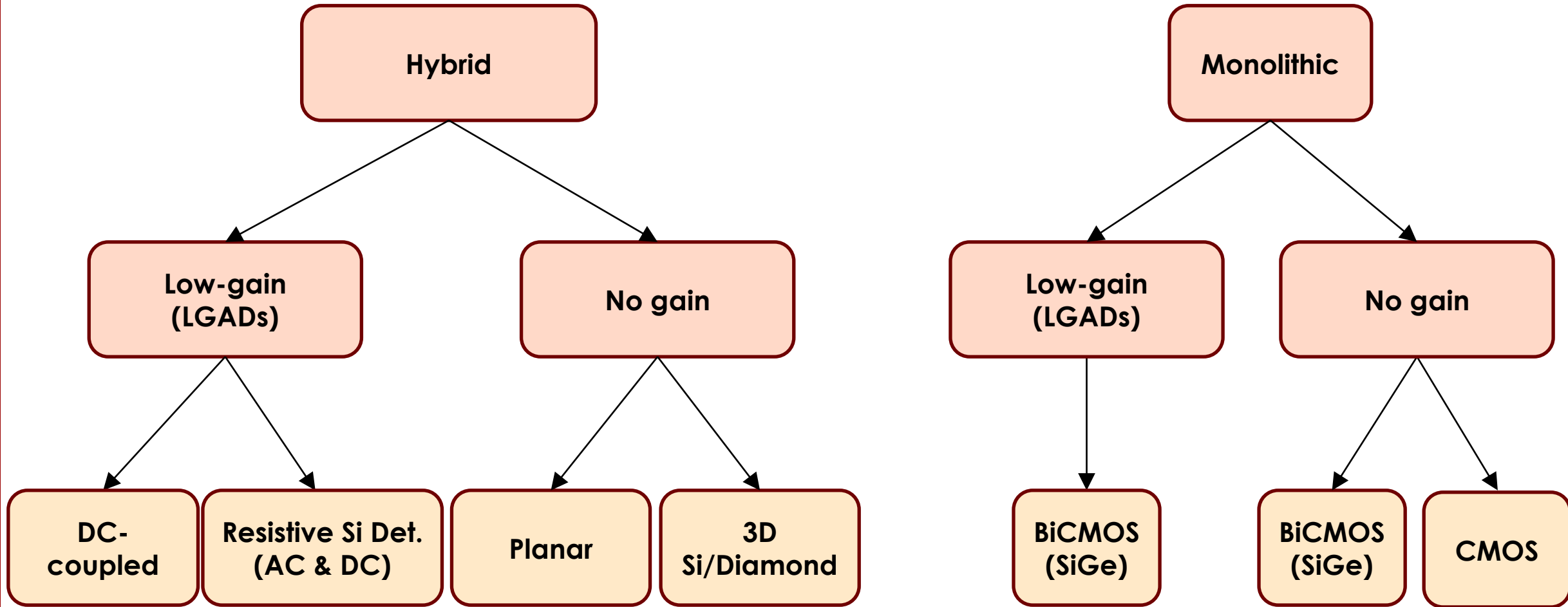


IFD 2022

G. Ambrosi, N. Cartiglia, C. Gemme, A. Lai, G. Paternoster



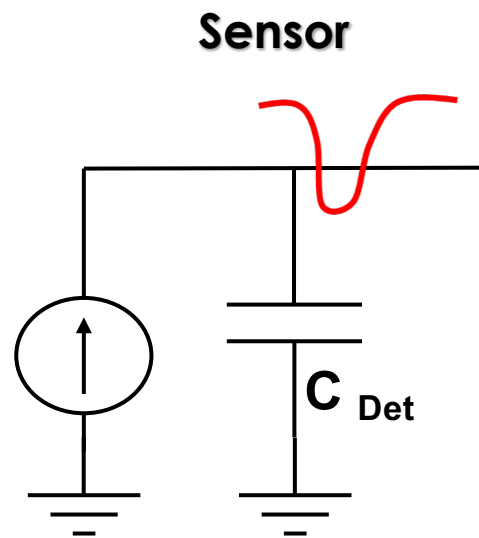
A pictorial overview of silicon detectors





Sensor – ASIC interaction

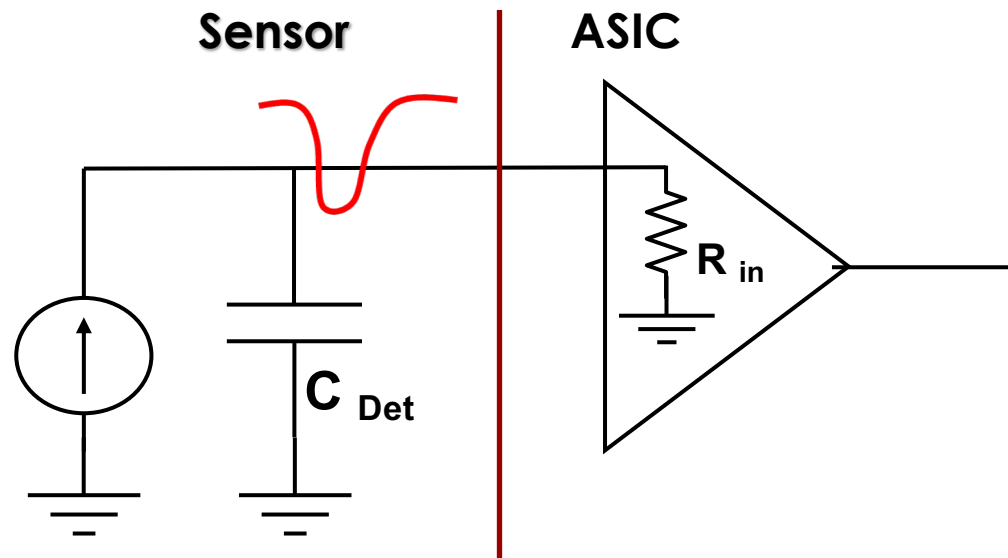
- Sensors produce a current pulse
 - ASICs measure the time of arrival
- ==> Sensors and ASICs are two parts of a single object





Sensor – ASIC interaction

- Sensors produce a current pulse
 - ASICs measure the time of arrival
- ==> Sensors and ASICs are two parts of a single object



Developing ASIC requires a critical mass in terms of people and money far superior than what is needed for the sensors.

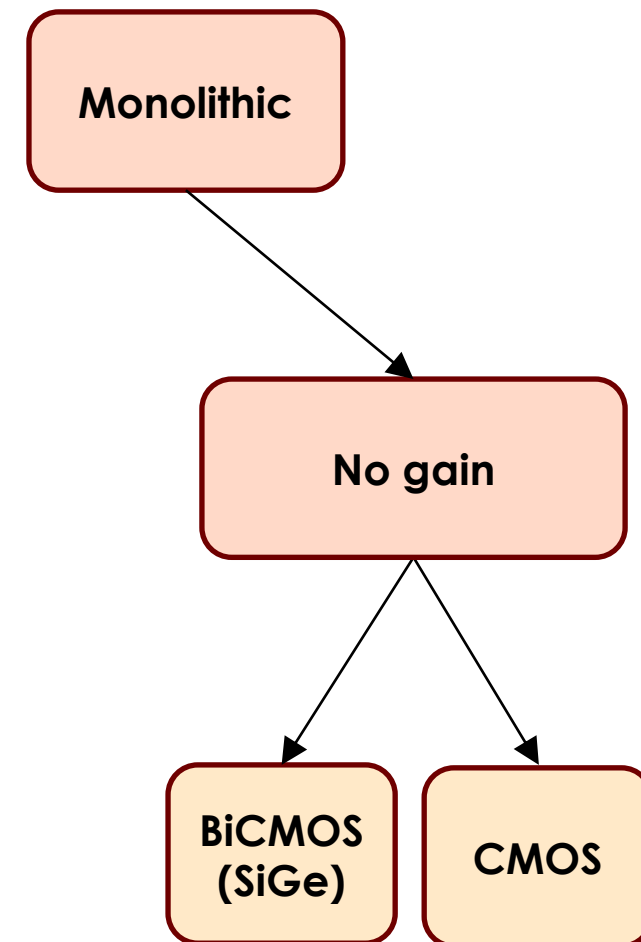
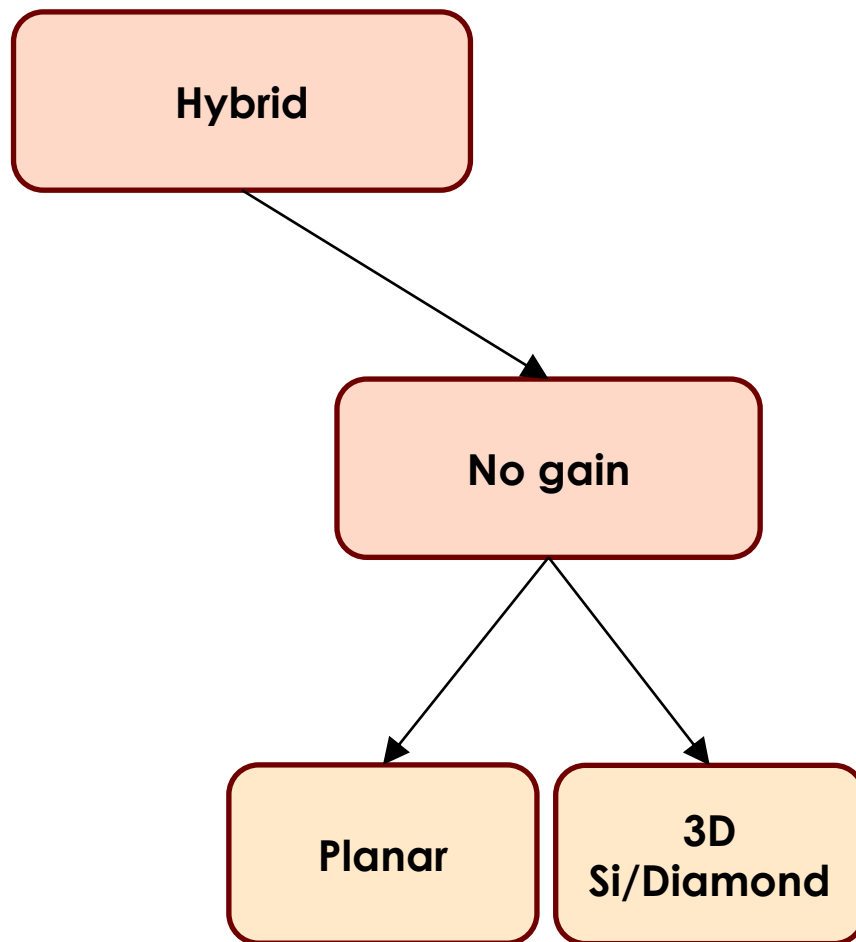
Presently, we have a large sensors offer and not enough ASIC to read them



Alcuni esempi di R&D fatti nell'ente

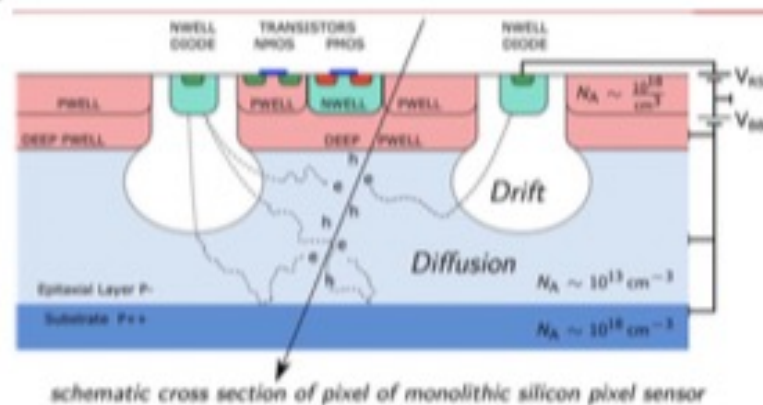
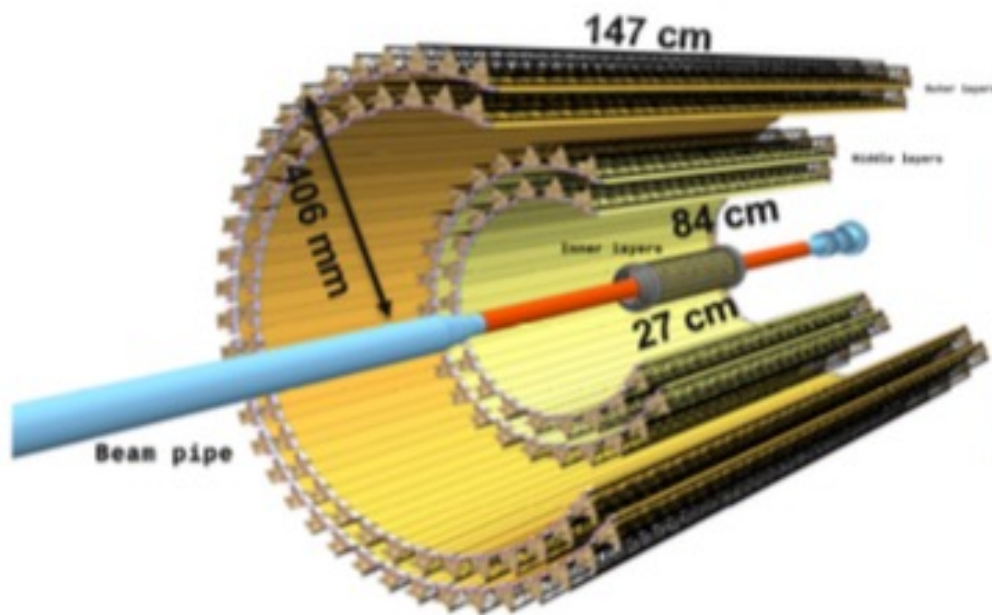


Sensors without internal gain



Sensors without internal gain

The new ALICE tracking system is entirely based on Monolithic Active Pixel Sensors called **ALPIDE**.



Monolithic

No gain

CMOS

Sensors without internal gain

Hybrid

Two possible options:

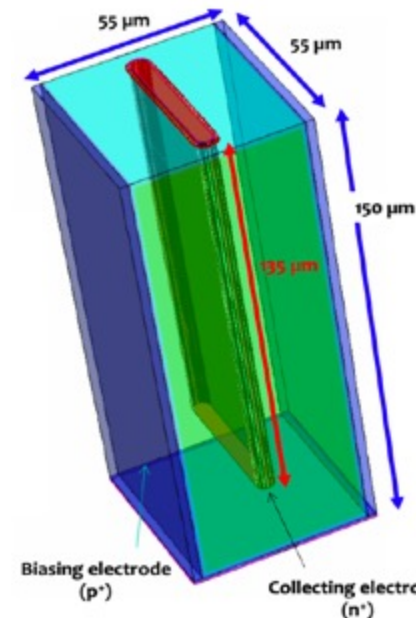
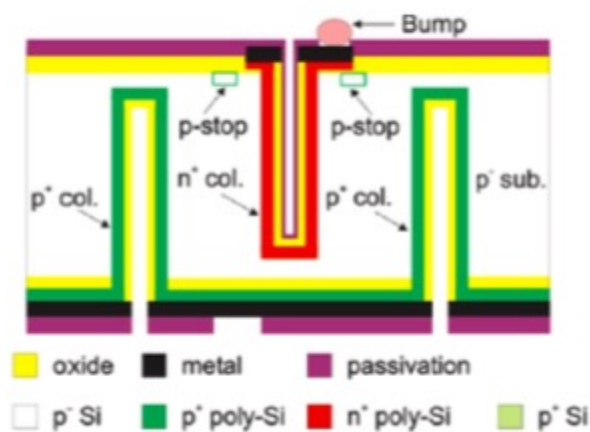
- Column
- Trenches
- The amount of charge is controlled by the sensor thickness (~1-2 fC)

Both requires small pixels to achieve good temporal precision
=> very good position resolution

No gain

3D
Si/Diamond

Schematic Cross Section



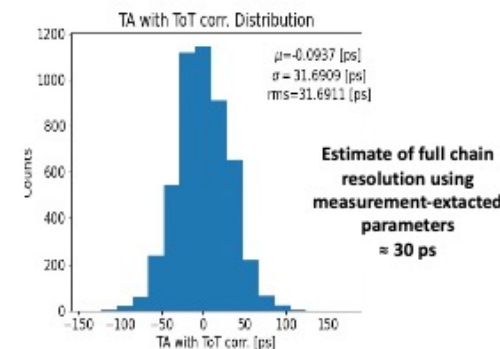
Timespot1: 28 nm ASIC

Pixels size = 55 μm

Sensor ~ 11 ps

ASIC: Front-end ~ 25 ps, 20 TDC

3D diamond column ~ 70 ps



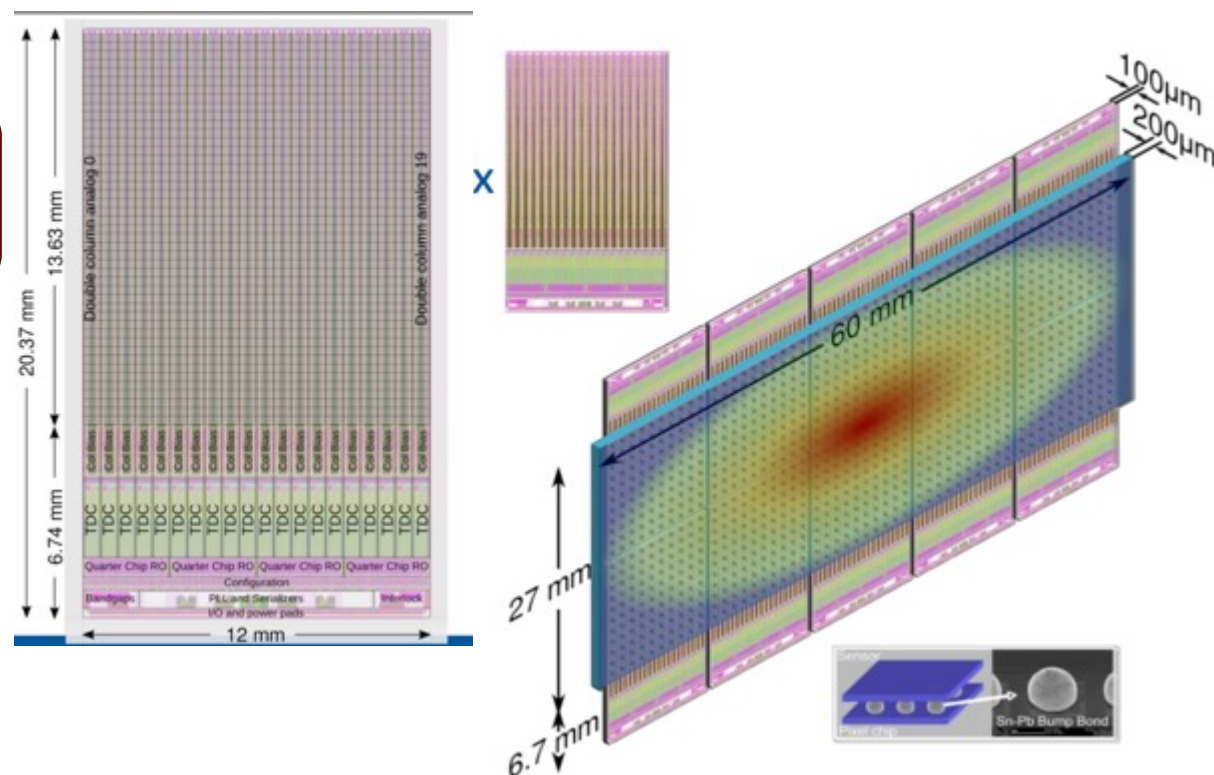
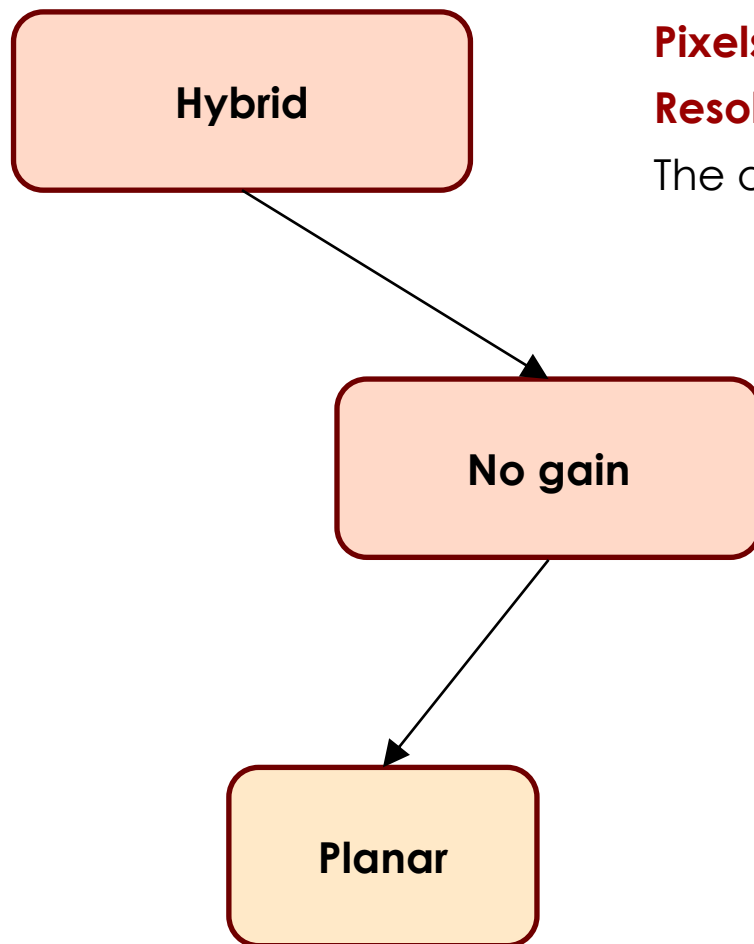
Sensors without internal gain

The TDCpix ASIC of the NA62 Gigatracker
==> 130 nm ASIC, 45 x 40 pixels

Pixels size = 300 x 300 μm^2

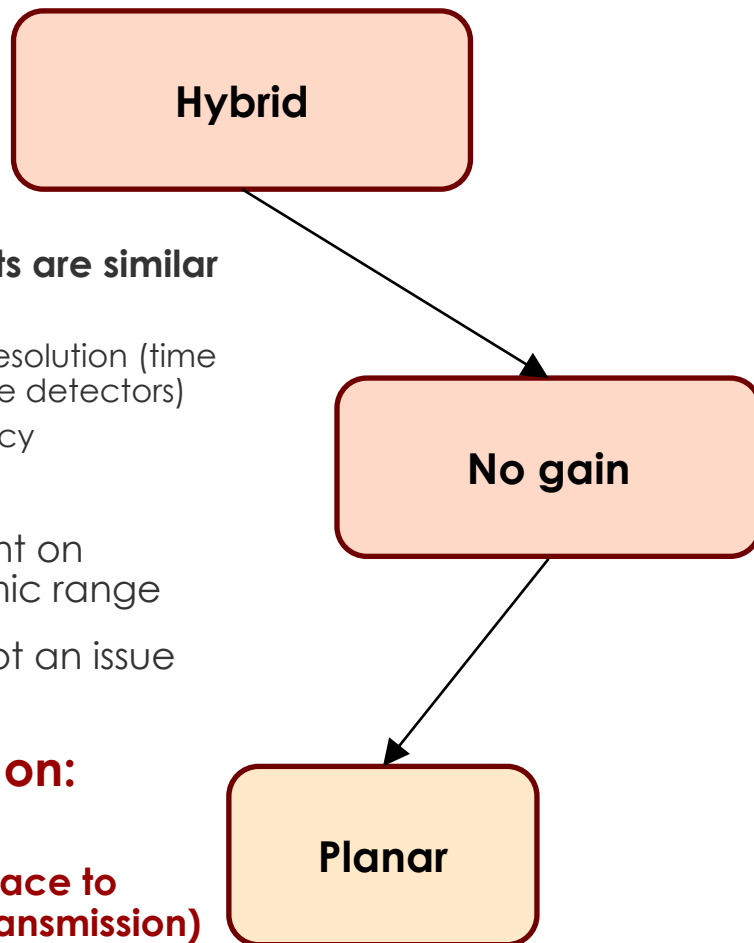
Resolution ~ 120 ps RMS

The only 4D tracking system on a working experiment



Sensors without internal gain

Space, the final frontier, these are the voyages of the silicon trackers in space...



Most of the requirements are similar to the accelerator use:

- spatial and time resolution (time resolution for future detectors)
- detection efficiency
- material budget

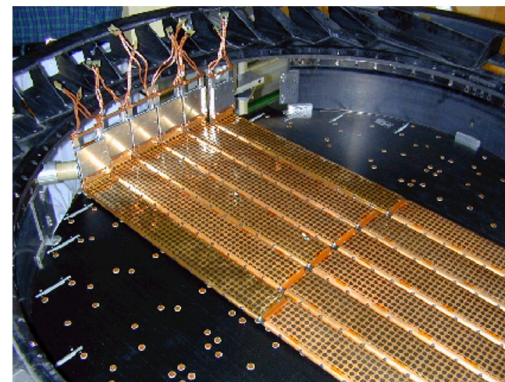
One special requirement on electronics: high dynamic range

Radiation hardness is not an issue (compared to LHC)

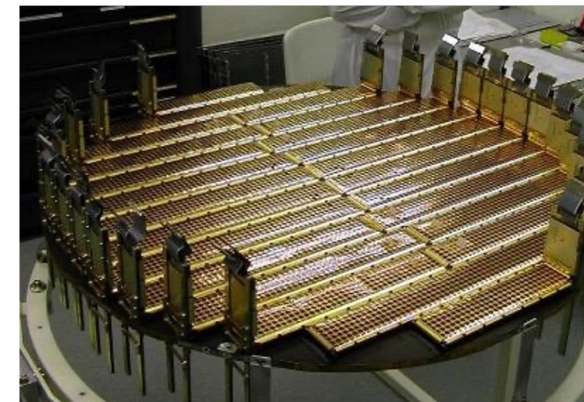
STRONG limitation on:

- **Power budget**
- **Bandwidth (space to ground data transmission)**

AMS-01 silicon tracker on Space Shuttle, 1998, $\sim 3 \text{ m}^2$



AMS-02 silicon tracker on Space Shuttle 2011, $\sim 6.5 \text{ m}^2$

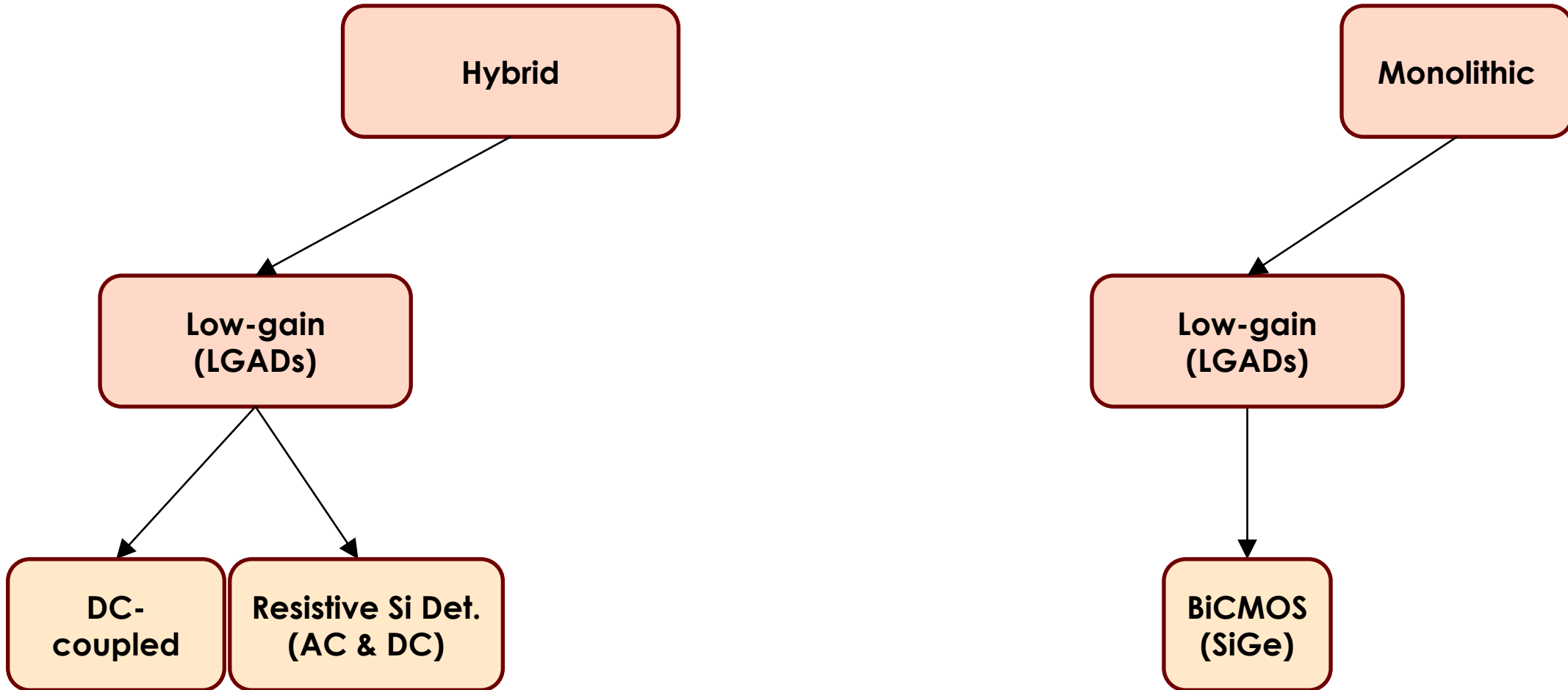


Semiconductor detectors (strips, pad, pixels) are widely used in space

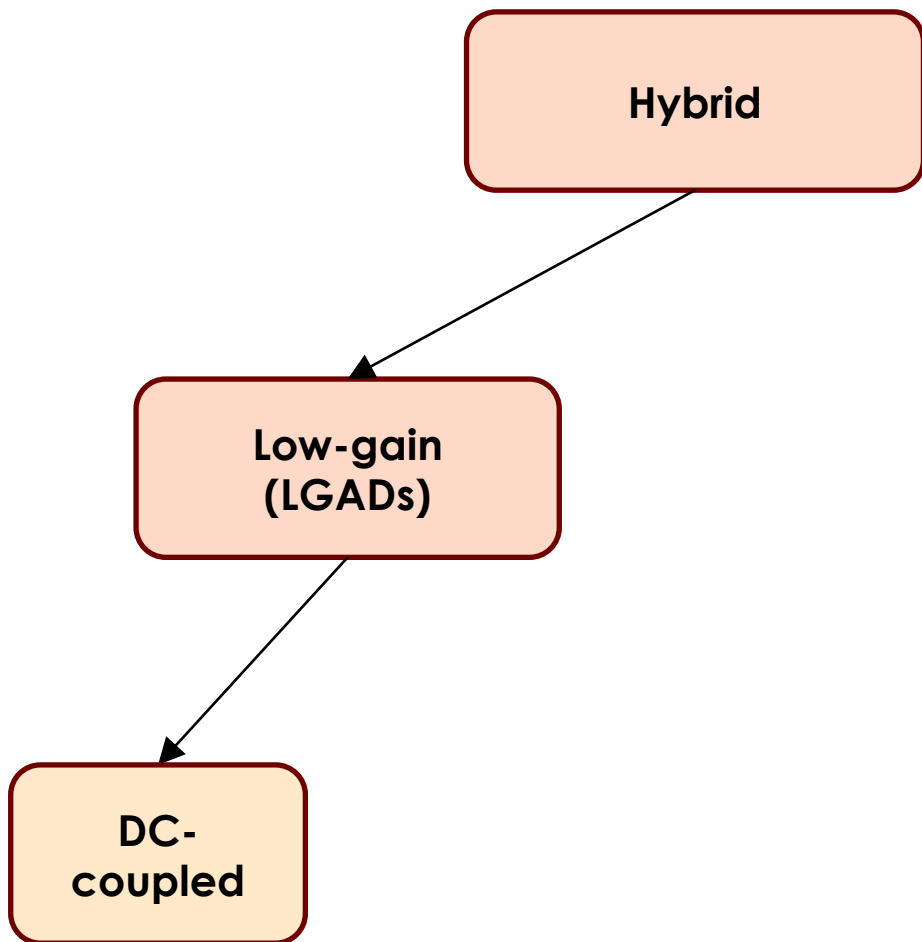
Operating Missions						
	Mission Start	Si-sensor area	Strip-length	Readout channels	Readout pitch	Spatial resolution
Fermi-LAT	2008	$\sim 74 \text{ m}^2$	38 cm	$\sim 880 \cdot 10^3$	228 μm	$\sim 66 \mu\text{m}$
AMS-02	2011	$\sim 7 \text{ m}^2$	29-62 cm	$\sim 200 \cdot 10^3$	110 μm	$\sim 7 \mu\text{m}$
DAMPE	2015	$\sim 7 \text{ m}^2$	38 cm	$\sim 70 \cdot 10^3$	242 μm	$\sim 40 \mu\text{m}$



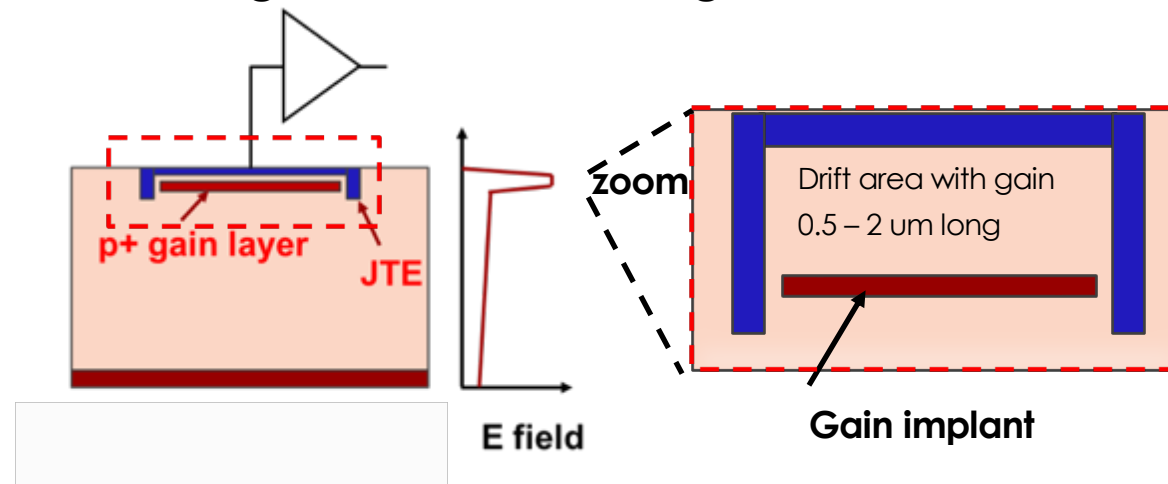
Sensors with internal gain



Sensors with internal gain



First design innovation: low-gain avalanche diodes



- The low-gain mechanism (LGAD), obtained with a moderately doped p-implant, is the defining feature of the design.
- The low gain allows segmenting and keeping the shot noise below the electronic noise, since the leakage current is low.

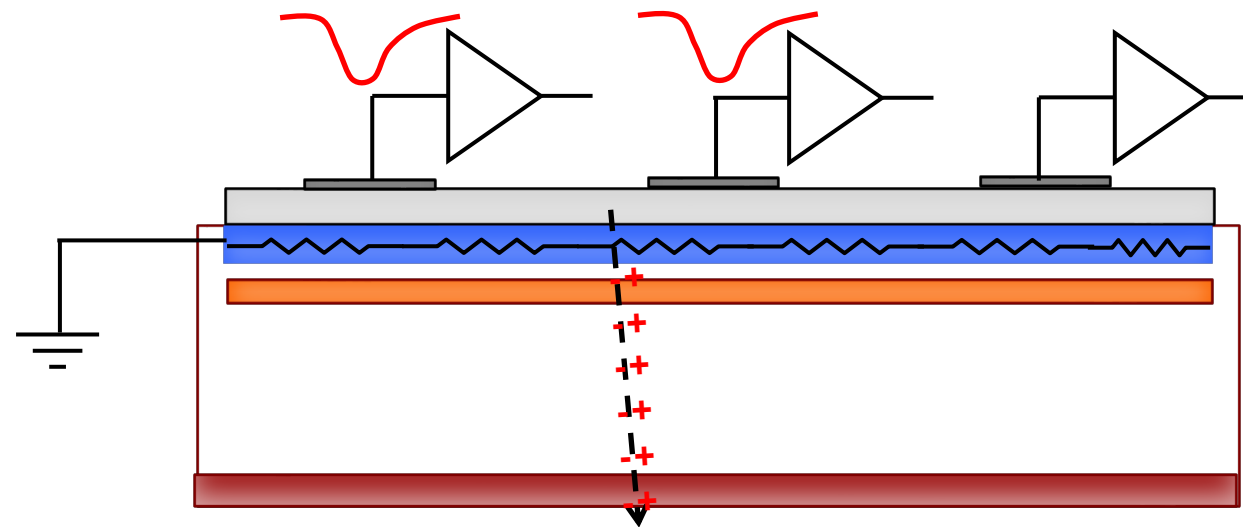
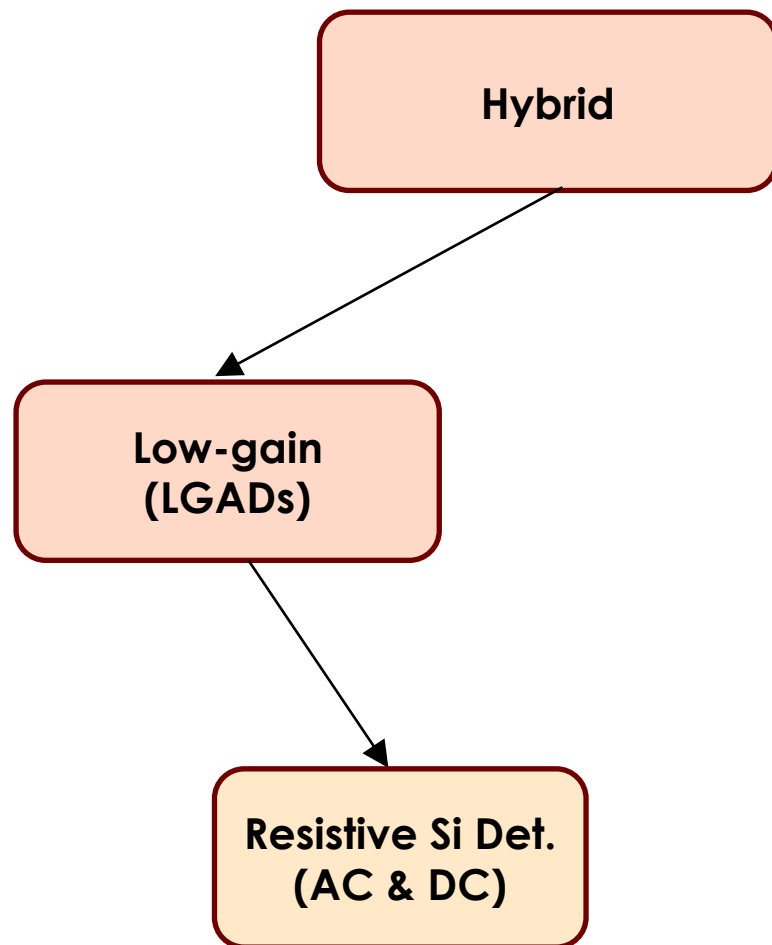
Choice of ATLAS & CMS for their "timing layer"

- Large pixels (1.3 x 1.3 mm²)
- Easy to manufacture (~ 20 m² to be built soon)
- ~ 30 ps resolution (sensor) and 20-30 ps the ASIC
- Rad-hard up to 1-2 E15 n/cm²

Very active R&D to extend this limit, financed by Gruppo V & AIDA innova (ExFlu)

Sensors with internal gain

Second design innovation: resistive read-out



A continuous resistive layer (n doped) shares the signal among read-out pads without the need of a magnetic field

- Excellent position resolution (3% of the pixel size) due to built-in charge sharing
- Temporal resolution as standard LGAD (30 ps)
- 100% fill factor
- Not optimal in high-occupancy environments
- **R&D carried on in Gruppo V INFN, and in experiment-specific groups (muColl, EIC, FCC-ee, ..)**



What will happen next in silicon-based tracking systems?

The ECFA road-map has identified 4 large families of R&Ds:

1. Achieve full integration of sensing and microelectronics in **monolithic CMOS pixel sensors**.
2. Develop solid-state sensors with **4D-capabilities** for tracking and calorimetry.
3. Extend capabilities of solid-state sensors to operate at **extreme fluences**.
4. Develop **full 3D-interconnection** technologies for solid-state devices in particle physics.



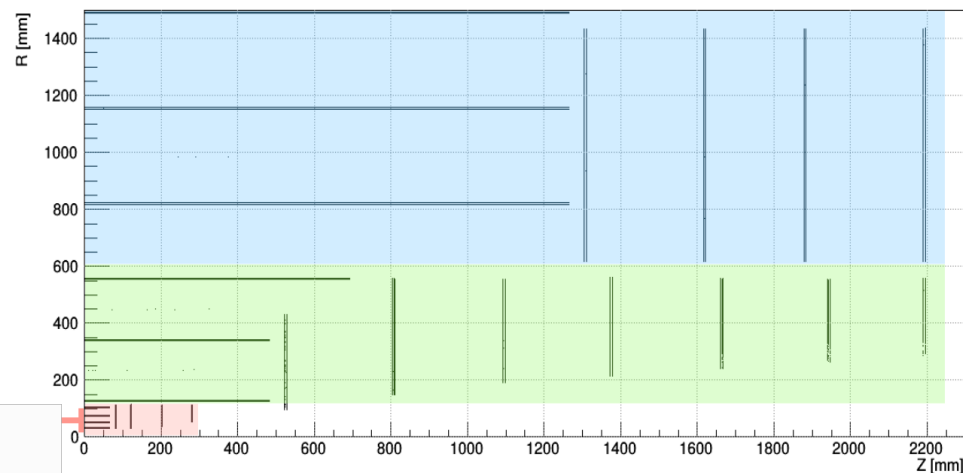
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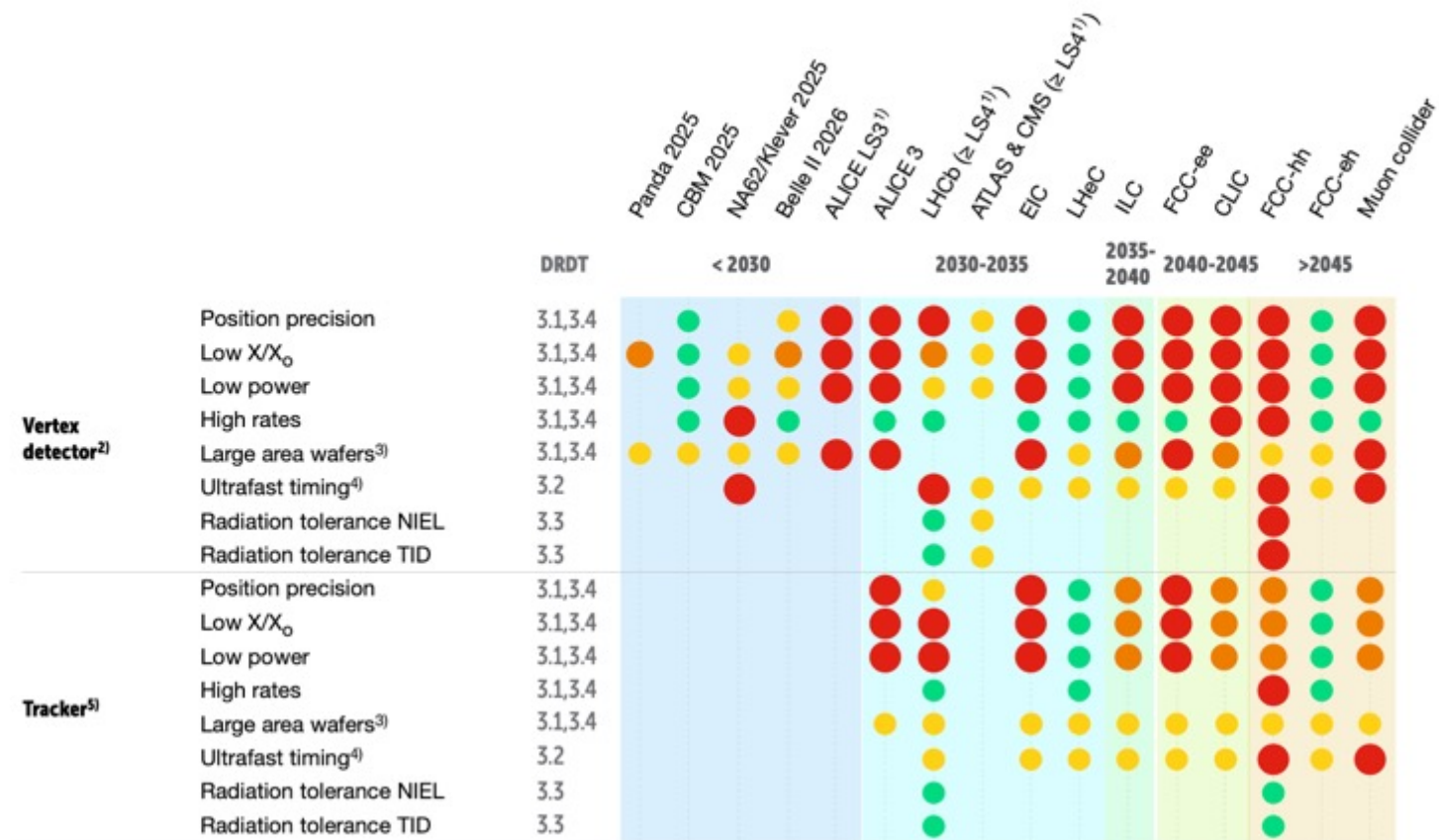
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Different environments require have vastly different requirements:

- Vertex
- Outer tracker
- Space
- Nuclear



What is actually needed (graphic)?



● Must happen or main physics goals cannot be met ● Important to meet several physics goals ● Desirable to enhance physics reach ● R&D needs being met

- 1) HL-LHC Long shutdowns: LS3/LS4 2025/2031
(see <https://lhc-commissioning.web.cern.ch/schedule/LHC-long-term.htm>)
- 2) LHCb/ATLAS/CMS consider Planar/3D sensors at the time of this document for rates and radiation tolerance. On a longer term, pixelated LGADs could be considered for potentially higher timing precision.
- 3) The size of wafers achievable can depend on technology (industrial process) with a general trend to benefit from larger areas.
- 4) Ultrafast timing refers to ≤ 100 ps depending on technology and detector purpose.
- 5) In trackers, coarser longitudinal granularities could be considered for MAPS. Thorough performance and cost comparison with passive CMOS would be needed. Pixelated LGADs could be considered for potentially higher timing precision.



What is actually needed (numbers)?

"Technical" Start Date		< 2030			2030 - 2035		2035 - 2040	2040 - 2045		> 2045	
		ALICE LS3	Belle II CBM	NA62	LHCb, ATLAS, CMS (\geq LS4) ⁷⁾	ALICE 3 - EIC	ILC	FCC-ee	CLIC	FCC-hh	Muon Collider
MAPS	technology node ¹⁾	65 nm - stitching	65 nm - stitching			28 nm		\leq 28 nm		\approx 10 nm	\leq 28 nm
	pitch	10 - 20 μ m	10 - 20 μ m			pitch \leq 10 μ m for $q_{it} \leq$ 3 μ m in VD					
	wafer size ²⁾	12"	12"			Reduce z-granularity in TK - pad granularity in analog Cal.					
	rate ³⁾				O(100) MHz/cm ²			5 GHz/cm ²		30 GHz/cm ²	
	ultrafast timing ⁴⁾					$\alpha_t \leq$ 100 ps				$\alpha_t \leq$ 20 ps	
	radiation tolerance				3×10^{15} neq/cm ²					$10^{18(16)}$ neq/cm ² VD/Cal.(Trk)	
Planar/3D/Passive CMOS	technology node ¹⁾				ASIC 28 nm	ASIC 28 nm		ASIC \leq 28 nm		ASIC \approx 10 nm	ASIC \leq 28 nm
	pitch				\leq 25 μ m in VD			\leq 10 μ m for $q_{it} \leq$ 3 μ m in VD			
	wafer size ²⁾							\leq 50 μ m for $q_{it} \leq$ 10 μ m in Trk			
	rate ³⁾				6 GHz /cm ²					30 GHz/cm ²	
	ultrafast timing ⁴⁾				$\alpha_t \approx$ 50 - 100 ps		$\alpha_t \leq$ 100 ps			$\alpha_t \leq$ 20 ps	
	radiation tolerance				6×10^{16} neq/cm ²					$10^{18(16)}$ neq/cm ² VD/Cal.(Trk)	
LGADs	technology node ¹⁾						ASIC 28 nm	ASIC \leq 28 nm		ASIC \approx 10 nm	
	pitch			\approx 300 μ m (100% fill factor)	\leq 50 μ m (100% fill factor)		same as for other technologies with ultimate pitch \leq 10 μ m for $q_{it} \leq$ 3 μ m in VD				
	wafer size ²⁾				$>$ 3"		12"				
	rate ³⁾				6 GHz /cm ²					30 GHz/cm ²	
	ultrafast timing ⁴⁾				$\alpha_t \leq$ 30 ps	$\alpha_t =$ 20 ps (PID)	$\alpha_t \leq$ 20 ps VD/Trk/Cal.	$\alpha_t \leq$ 10 ps PID	$\alpha_t \leq$ 20 ps VD/Trk/Cal.	$\alpha_t \leq$ 20 ps VD/Trk/Cal.	
	radiation tolerance				\approx 5×10^{15} neq/cm ²					$10^{18(16)}$ neq/cm ² VD/Cal.(Trk)	
Backend processing	sensor thickness ⁵⁾	$<$ 50 μ m MAPS	$<$ 50 μ m MAPS		$<$ 150 μ m Planar/3D/Pas. $<$ 50 μ m LGADs	$<$ 50 μ m MAPS, Planar/3D/Passive CMOS, LGADs					
	3D integration ⁶⁾										

Only the projects requiring a new feature first are retained in this table. Values are indicative of performance targets and of operating conditions relevant to R&D. The latter are reported for the regions most exposed to radiation. The colors indicate when key progress (red) would be needed for a given technology or when they would be desirable (yellow). Green indicates requirements are being met. The different technologies are alternatives for the various detectors. The final choices will depend on their ability to achieve different performance parameters together. Heterogenous layer designs can combine technologies to optimize the overall performance.

1. The evolution in the technology node is progressive and indicative. It can depend on achievements in each node. It will also be driven by industrial standards.
2. The size of wafers achievable can depend on technology with a general trend of benefits from larger areas in all detectors. Either to bend sensors (depending on thickness and detector) or to house more than one sensor in a single substrate.
3. Reported rates are within bunch trains for ILC and CLIC.
4. The values reported are indicative of expected intrinsic performance, not excluding that it can be better with different achievements for sensors w/o amplification. Implementation of 4D-tracking at e-e colliders will depend on ability to maintain low X/X0 for tracking precision.
5. Thin sensors are not a requirement for analog calorimetry energy resolution, while they could provide better timing precision.
6. 3D integration exist in the commercial process (imagers) and could be beneficial in several performance aspects for future solid-state devices. It may be needed to fulfil the most stringent requirements and/or to enable desirable performance. Initial demonstrators could enter HL-LHC upgrades.
7. MAPS technology is only foreseen for use in the LHCb tracker. Planar/3D/passive CMOS are foreseen for the LHCb, ATLAS, and CMS vertex detectors, rates and radiation tolerance are indicated for LHCb where values are the highest (conditions for ATLAS and CMS are already met).



Technical Requirements of 4D-Tracking: 2 examples

1) At the next generation of Upgrades (@hadron colliders)

(NA62 4x, LHCb run5, vTag, CMS-PPS,...FCC -hh...)

- Space Resolution $\sigma_s \approx 10 \mu\text{m}$ (pixel pitch $\approx 40\text{--}60 \mu\text{m}$)
- Time Resolution $\sigma_t \leq 50 \text{ ps}$ on the full chain ($\sigma_t = \sigma_{\text{sensor}} \oplus \sigma_{\text{FE}} \oplus \sigma_{\text{TDC}}$)
- Radiation hardness to high fluences (for sensors) and high doses (for electronics).
Fluences $\Phi = 10^{16} \div 10^{17} \text{ MeV n}_{\text{eq}}/\text{cm}^2$ and Doses $> 1 \div 2 \text{ Grad}$
- A detection efficiency of $\varepsilon > 99\%$ per layer is typically required (high fill factor)
- The material budget must be kept below $1 \div 0.5 \%$ radiation length per layer

Very challenging front-end electronics must be developed:
high resolution @ $10\text{s } \mu\text{W}/\text{pixel}$, huge data bandwidth $\approx 100 \text{ Gbps}/\text{cm}^2$.
Today a complete solution for that is FAR from being available.
Developments ongoing

2) In future space applications

Here the problem is the opposite:

- How do we achieve precise timing with very long strips and limited power?
- Is it possible at all?
- Are "strips" the correct solution?



Table of Sensor Technologies for 4D-tracking

	Technology	Pixel pitch [μm]	Space resolution	Max Time resolution [ps]	Max fluence [$10^{16} \text{ MeV n}_{\text{eq}}/\text{cm}^2$]	Geometric efficiency	V_{bias} [V]	Technological Readiness Level (1-9)
Hybrid	LGAD	>500	pitch/ $\sqrt{12}$	30 ^[1]	< 0.5	>90%	250-550	7-8
	3D-trench[5]	55		10 ^[5]	> 2.5	99%	100	6-7
	TI- LGAD	>40 ^[2]		30 ^[3]	< 0.5 *	>85%	250-550	3-4
	AC-LGAD (RSD)	50-2000	Pixel*0.03	30 ^[4]	< 0.5*	99%	250-550	3-4
Monolithic	picoAD Si-Ge BiCMOS 130nm	65	pitch/ $\sqrt{12}$	17 ^[6]	Typical ≈ 0.1	>99%	125	3
	fastPIX CMOS 180 nm	15	pitch/ $\sqrt{12}$	150 ^[7]	Typical ≈ 0.1	>99%	2.4	3

*Expected value. Only partially validated

[1] A. Howard 37th RD50 Workshop

[2] G. Paternoster et al., IEEE Electron Device Letters, vol. 41, no. 6, pp. (2020)

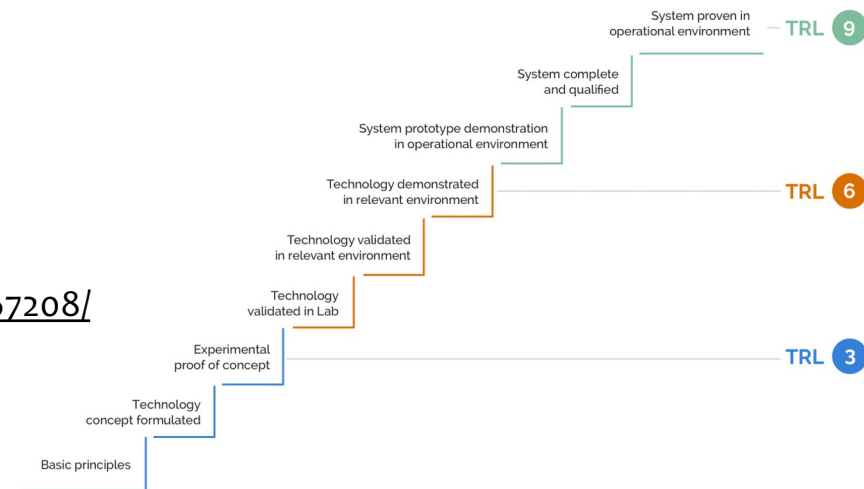
[3] M. Senger et al., NIMA, Vol. 1039 (2022)

[4] M. Tornago et al, NIMA, Vol. 1003 (2021)

[5] A. Lampis et al., 23rd IWORLD (2022), <https://indico.cern.ch/event/1120714/contributions/4867208/>

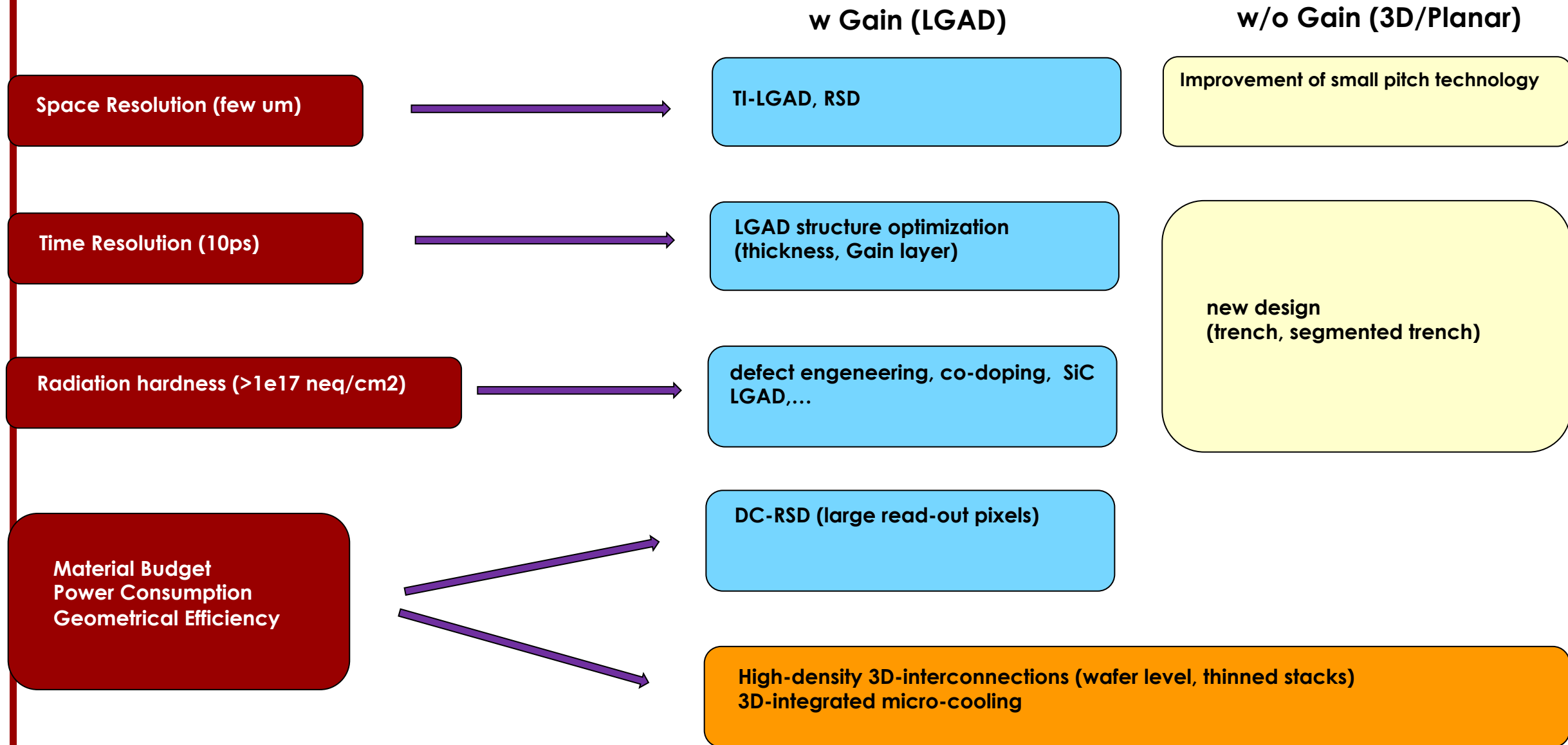
[6] L. Paolozzi et al., 1st Monolith Workshop (2022), <https://indico.cern.ch/event/1179742/>

[7] W. Snoeys et al., 1st Monolith Workshop (2022), <https://indico.cern.ch/event/1179742/>





Sensors for future hybrid detectors





ASIC State of the art

Incomplete list of ASICs for timing pixels (handle with care!)

Name)	Year	CMOS node [nm]	σ_t [ps] on 1 MIP	Pitch [μm]	# pixels	C_{in} [fF]	Power per pixel [μW]	Average power [W/cm^2]	MPV per MIP [fc]	Max hit rate [GHz/cm^2]	TW correct. type	Sensor tested
Timespot1	2021	28	< 40 (AFE) < 20 (TDC)	55	1024	35	20 (AFE) 38 (TDC)*	1.8 (pixel)	2.0	100 (pixel)	ToT	3D
Timepix4	2020	65	70 (AFE) 60 (TDC)	55	$229 \cdot 10^3$	65	15 (AFE)	0.5 (AFE)	1.6	150 (pixel) 0.36 (R/O)	ToT	planar
TDCpix (NA62)	2014	130	75 (circuit) < 200 (sens)	300	1800	250	300 (FE+disc)	3.3 (pixel)	0.5-10 (range)	0.8	ToT	planar
Fastpix	2021	180	≈ 150	10–20	68	< 1	no TDC	N	N	N	Only analog	MAPS
Fast2	2020	110	15	500	32	$3.4 \cdot 10^3$	$3 \cdot 10^3$	1.2	16	120	Only analog	LGAD
Monolith	2021	130 Si-Ge	~ 20 (AFE)	100	144	80	150 (AFE)	1.8 (pixel)	N	N	Ampl. PeriphTDC	MAPS
TOPHIR2X	2021	130	55	3000	32	N	$12.4 \cdot 10^3$	0.1	N	$2.8 \cdot 10^{-2}$	ToT	SiPM
ETROC1	2020	65	35	1300	16	$3.5 \cdot 10^3$	$2.4 \cdot 10^3$	0.2	6	2.3	ToT	LGAD
ALTIROC1	2020	130	50	1300	25	$5 \cdot 10^3$	$4.4 \cdot 10^3$	0.3	4	N	ToT	LGAD

N = not applicable or not known

*at 350 kHz per pixel



Obs1: Progetti a lungo termine

Nel passato abbiamo avuto cicli di

R&D → Detector – R&D

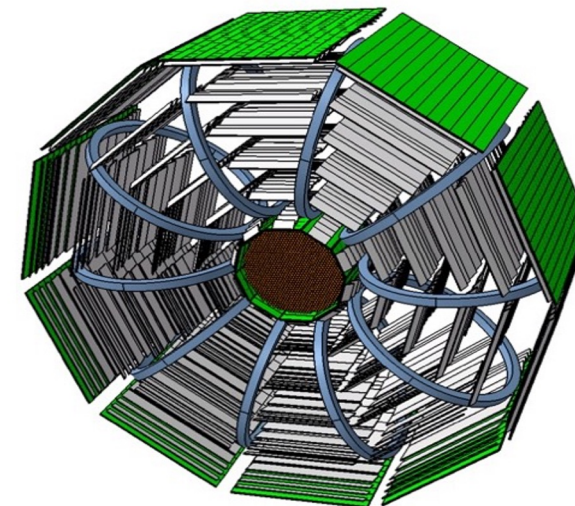
che erano corti rispetto alla vita lavorativa e dunque nell'attività INFN.

I tempi si sono allungati con la complessità degli esperimenti e delle tecnologie.

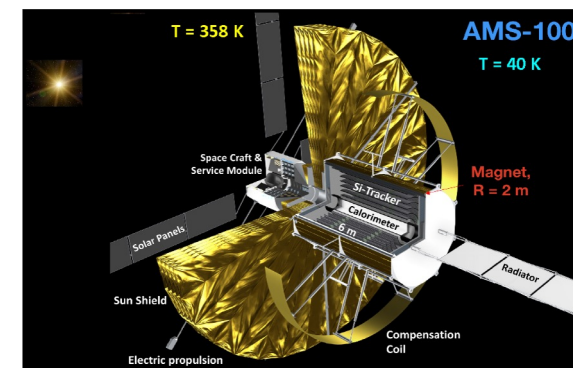
Eccetto per upgrade durante HL-LHC, gli altri scenari hanno una scala temporale estremamente lontana.

- Come generare un percorso che stimoli R&D a lungo termine?
- Come coinvolgere junior/senior su queste scale di tempi?

ALADINO Italian leadership



AMS 100 (2040, 2050?)





Obs2: scelte tecnologiche e finanziamenti

- **Non è chiaro quale sarà la direzione dei future colliders, quali saranno i punti essenziali da sviluppare**

Low power, timing , material budget , radiation resistance , high data transfer, On-detector intelligence

- **Tecnologie importanti (interconnessioni, stacking...) sono praticamente inaccessibili a causa dei costi e del fatto che per ora il loro utilizzo sia stato proposto da gruppi sparsi**

- Ci vuole uno sforzo dell'ente? RD53 ha dimostrato l'utilità di sforzi collettivi trans-experiments

- **IGNITE** (sviluppo 28 nm) e' un caso isolato o l'inizio di una nuova politica dell'ente mirata a finanziare, **fuori da gruppo V**, sviluppi chiave non legati ad un esperimento?

- Come si lega INGITE (o più in generale questo modello di finanziamento) alla proposta dei DRD del CERN-ECFA?