β-Chip preliminary results

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List of questions and doubt

- We need an External trigger (input trigger with possibility to validation)
- Trigger AND or OR between Chips
- Simultaneous acquisition of 2 chips
- Busy Output
- Trigger Mask on specific channels
- Flag on channel that have generate the trigger (for internal trigger mode)
- What are values of VFS and TEMP in the output file
- Strange behavior with trigger frequency > 1 kHz (change in gain)
- Forcing the path on the high gain we have noticed a "saturation" at ~1500 ADC channel. Could it be a path switch on the low gain???
- The acquisition program register 225 kEvts/s for trigger frequency > 50 kHz (DAQ saturation???)
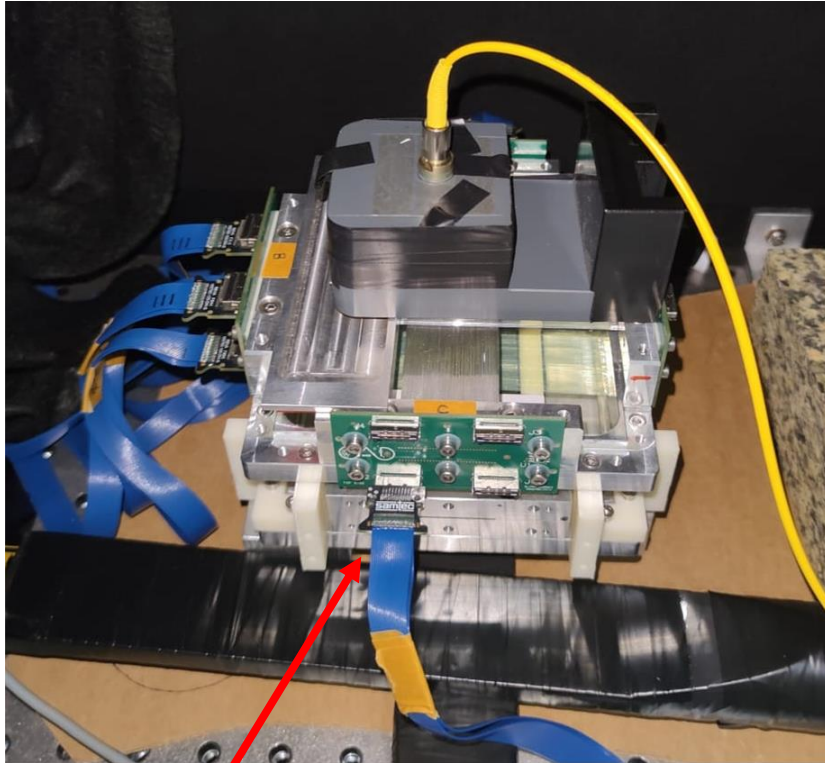
Laser with fiber Set-Up

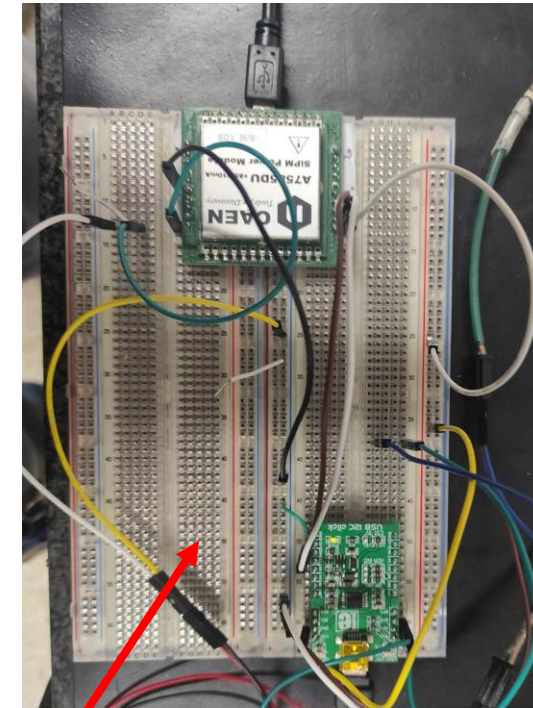# β-Chip test with Laser SetUp
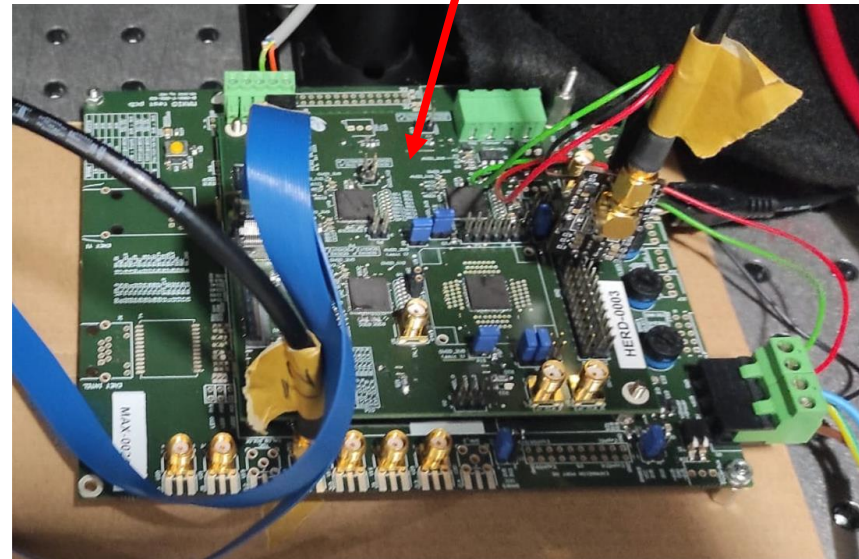
Laser diffuse on fiber array

ASIC 1

ASIC 0
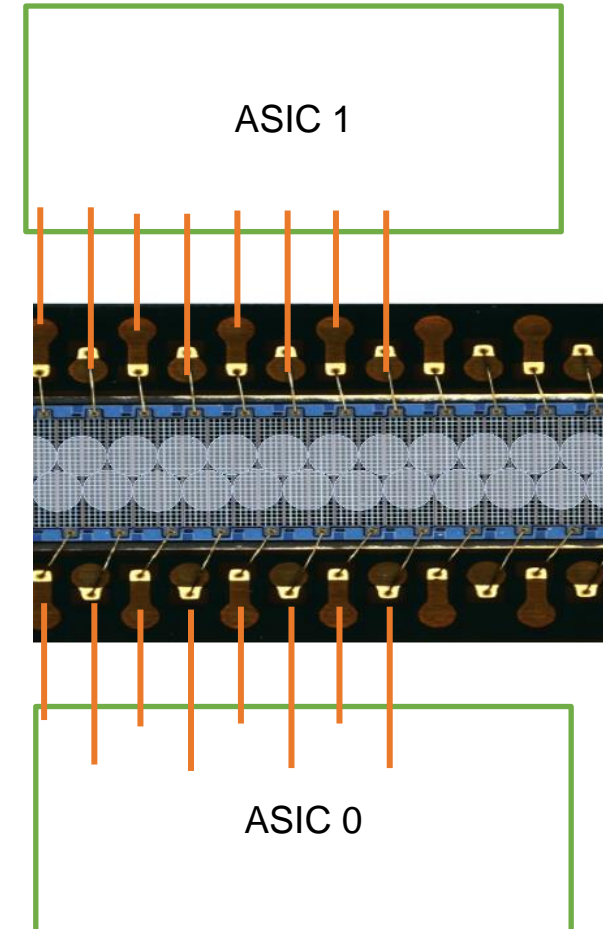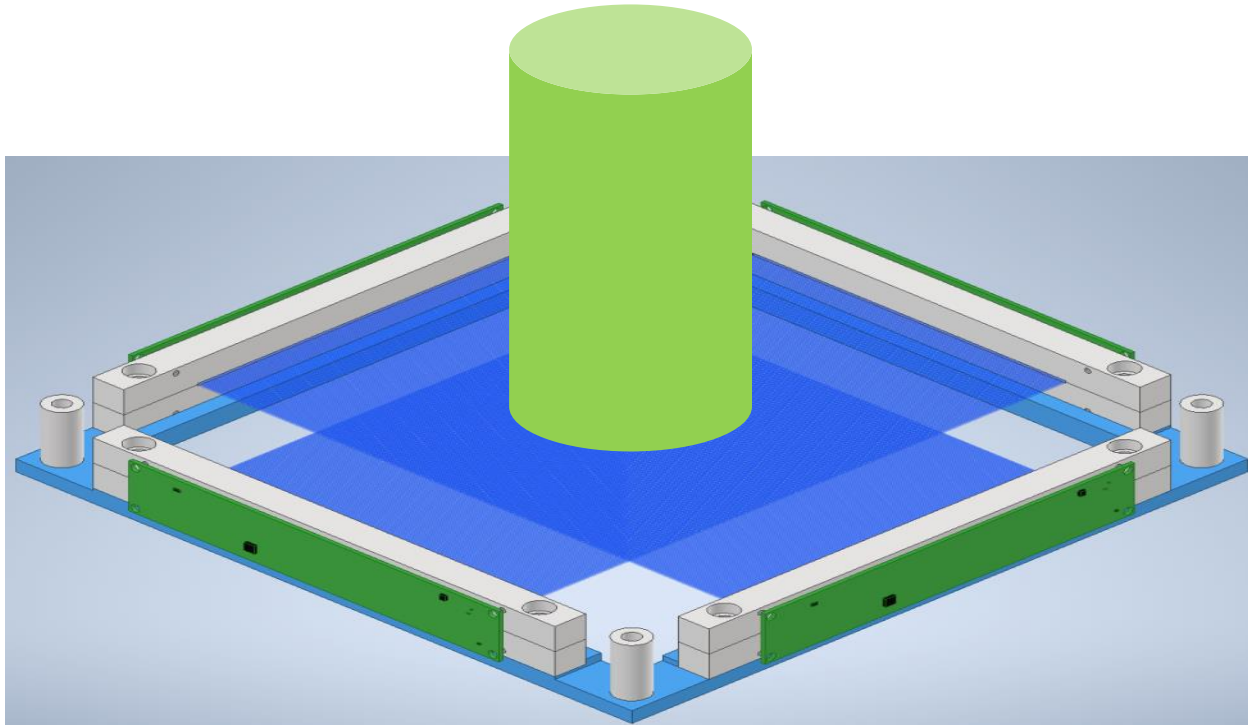
β-Chip test with Laser SetUp
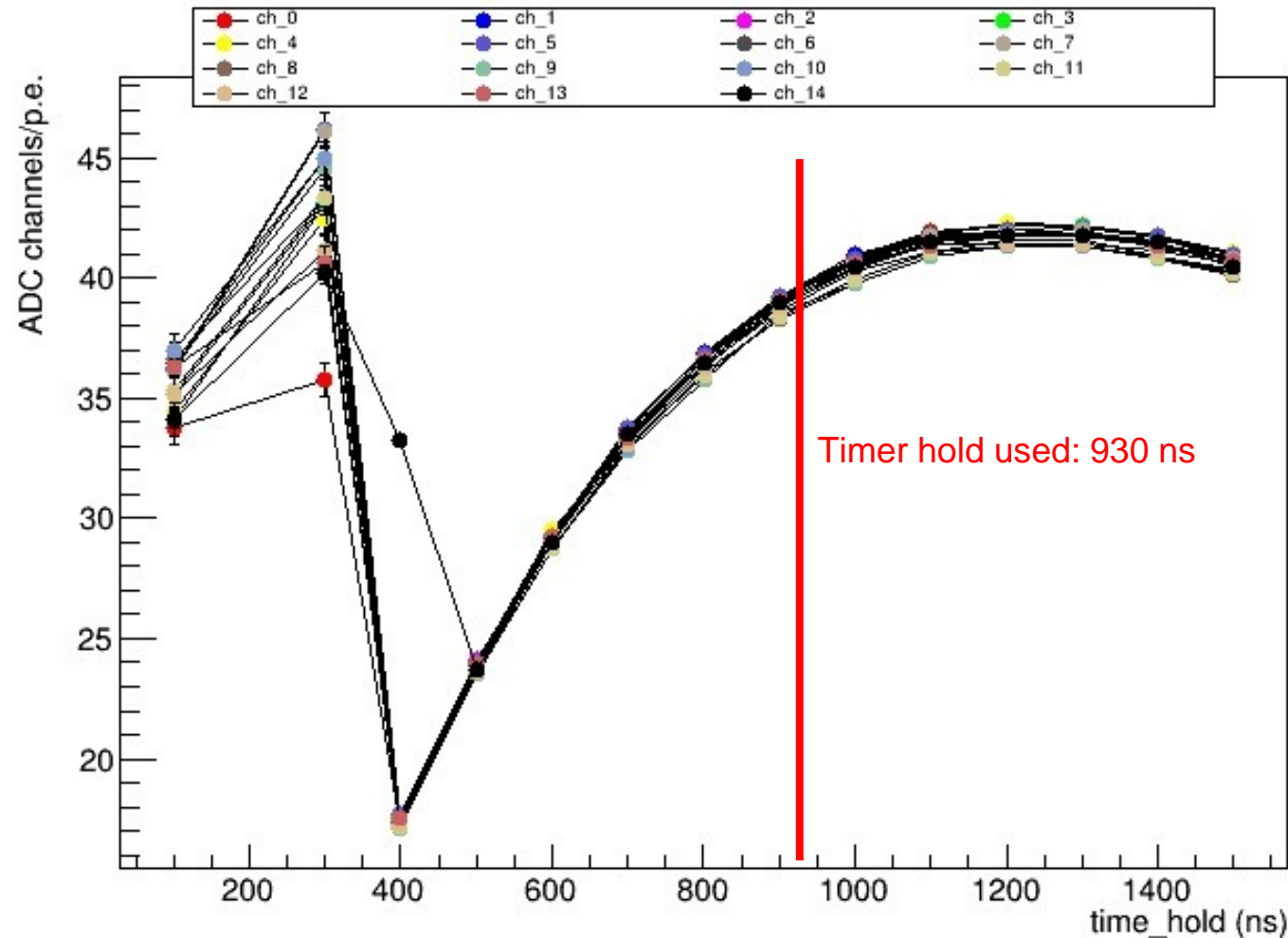
β-Chip front-end board

β-Chip

CAEN A7585D SiPM voltage module – Controlled by USB/i2c module

Timer Hold scan

The external trigger was sent from board to the laser trigger input
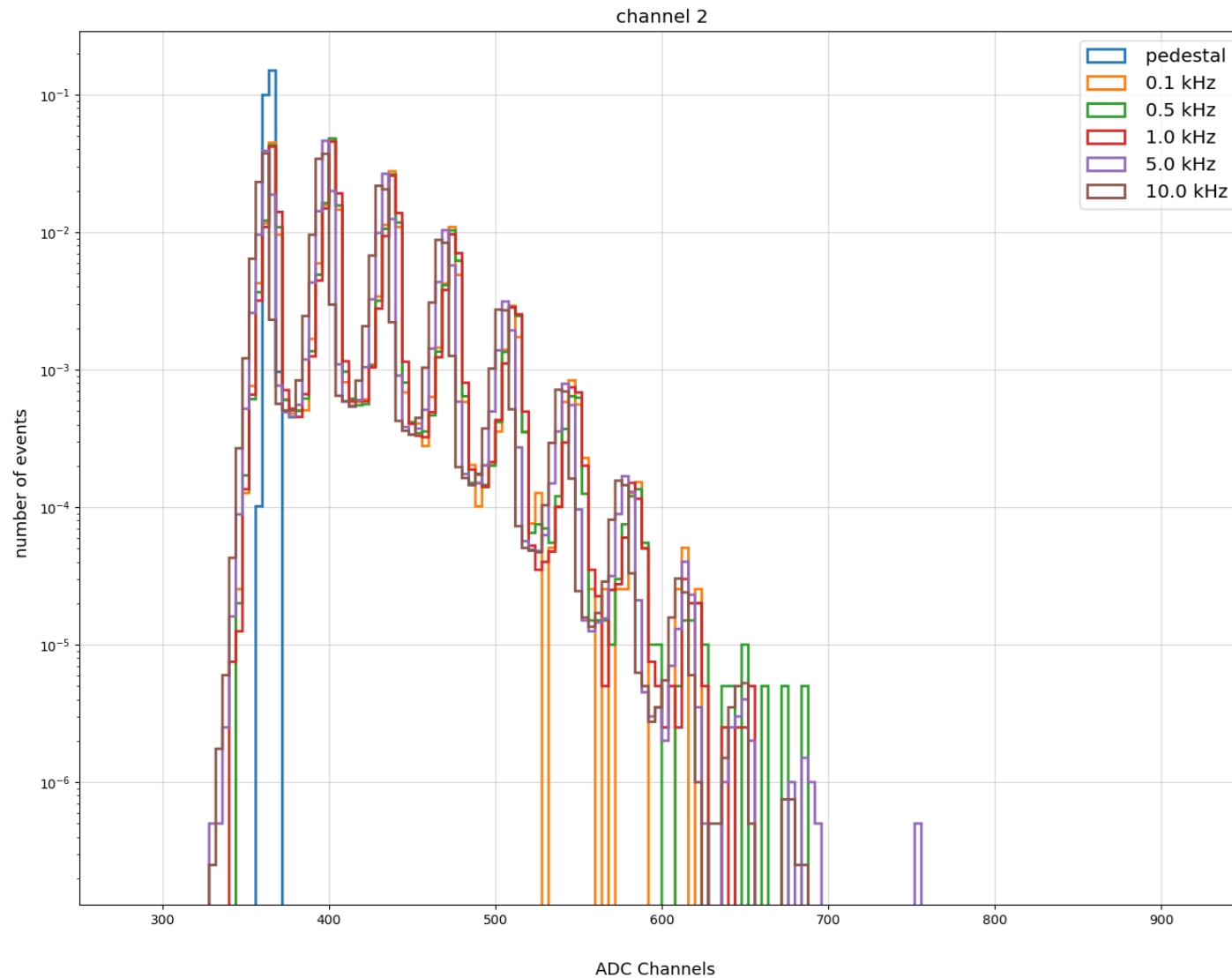
External trigger mode: **Timer Hold**

./beta.bin config -b MAX-0020 --asic_id 1 --i2c_freq 1 -c --cgain_hg 8 --cgain_lg 8 --cgain_sh_c2 8 -- cgain_sh_c3 8 --cgain_hg_lpf 8 --cgain_lg_lpf 8 -- timer_rst 1500 -t 0 255 1 255 2 255 3 255 4 255 5 255 6 255 7 255 8 255 9 255 10 255 11 255 12 255 13 255 14 255 15 255 --vref 32 --voff_pream 32 -- mux_drv 0 --mux_path 0 --timer_hold VH --fpga_trg 1 --trg_delay 100

VH = [100, 300, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200, 1300, 1400, 1500] ns

Timer hold used: 930 ns

FPGA Trigger Scan

The external trigger was sent from board to the laser trigger input
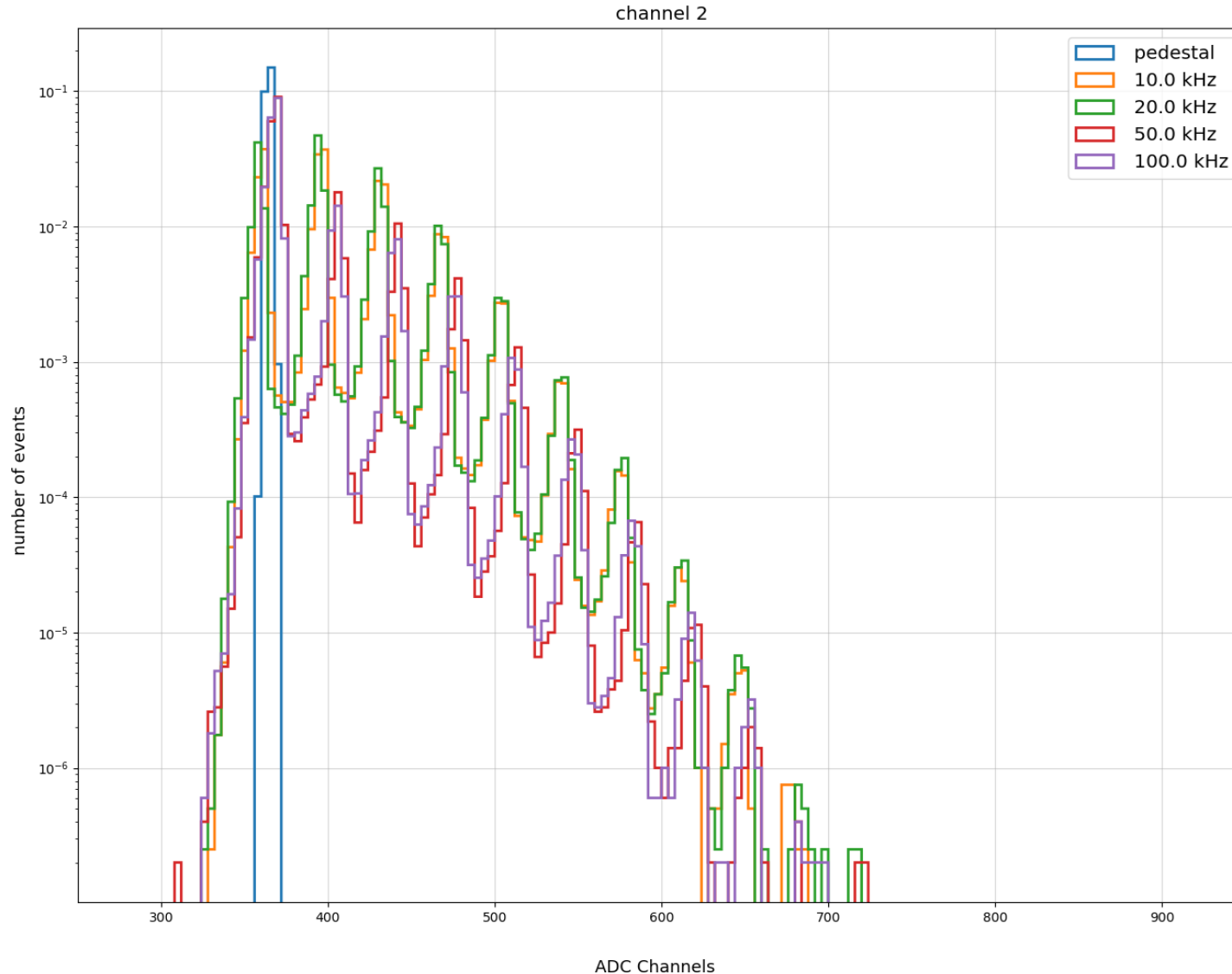
External trigger mode: **FPGA Trigger**

channel 2

From 100 Hz to 10 kHz the finger plots look good

The external trigger was sent from board to the laser trigger input
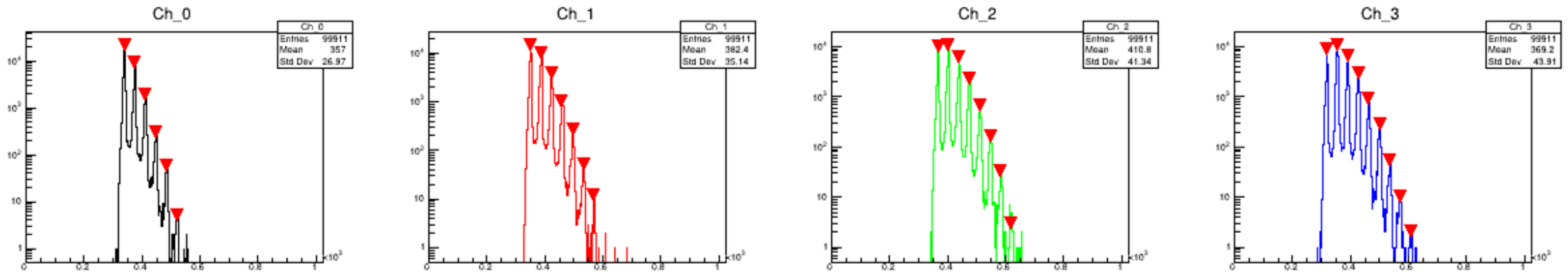
External trigger mode: **FPGA Trigger**

From trigger frequency > 50 kHz the peaks change in position and shape.
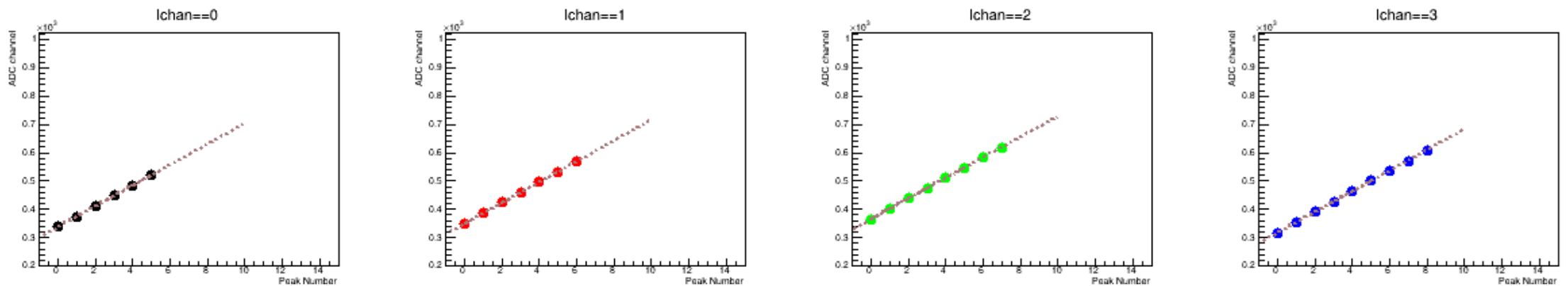
The acquisition program register 225 kEvts/s both for 50 kHz and 100 kHz (DAQ saturation???)

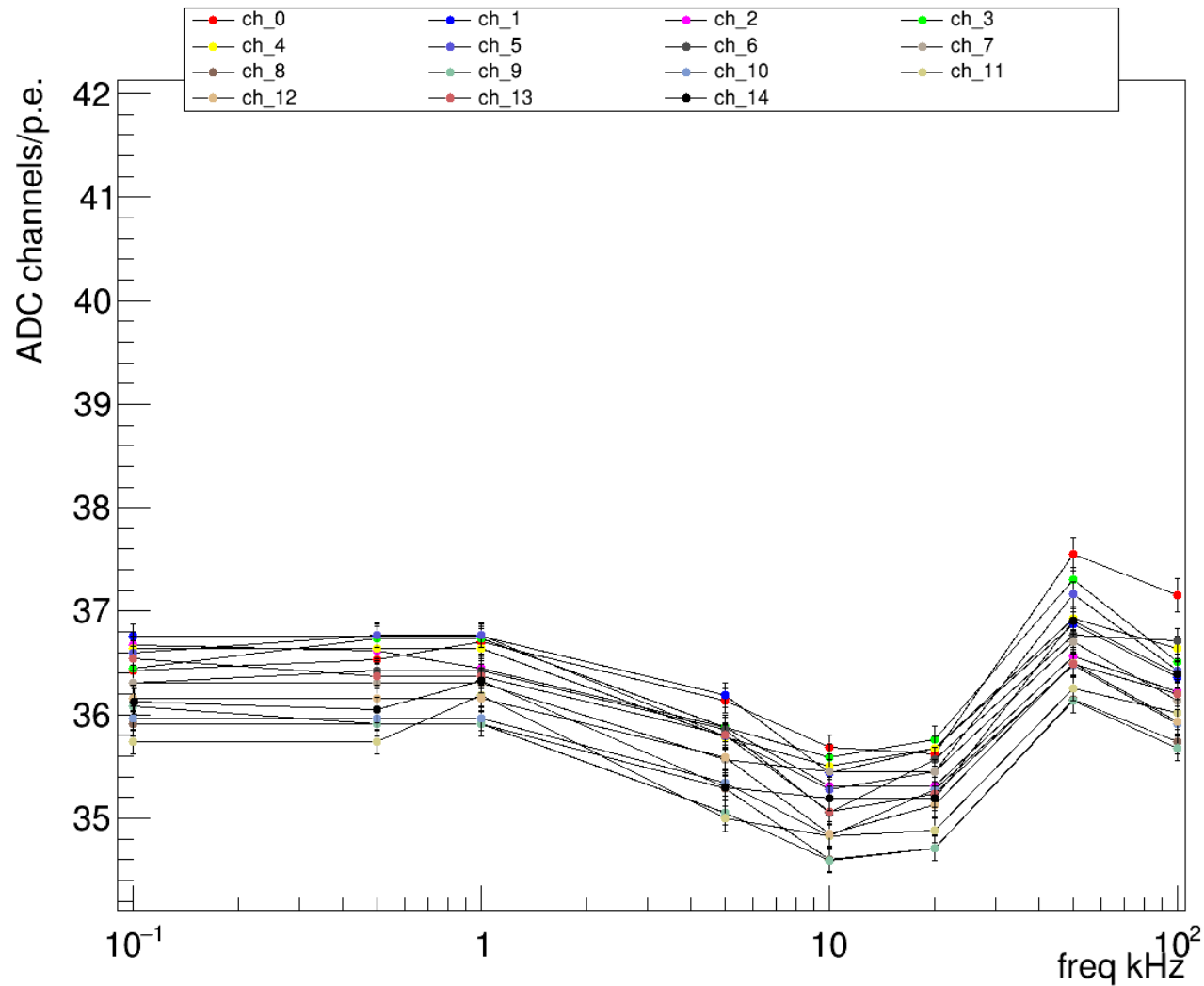**The external trigger was sent from board to the laser trigger input**

External trigger mode: **FPGA Trigger** ROOT TSpectrum **1 kHz example**

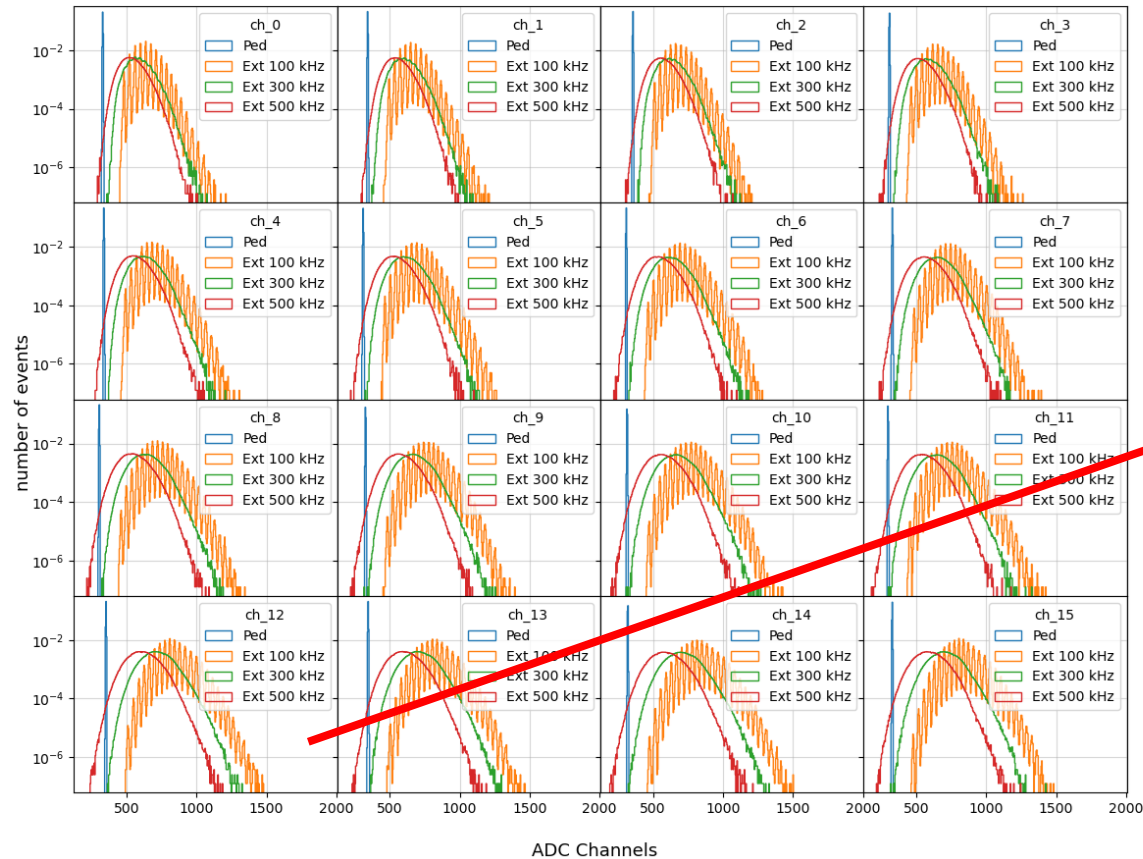**Gain** channel by channel (ADC Channels/ # p.e.)
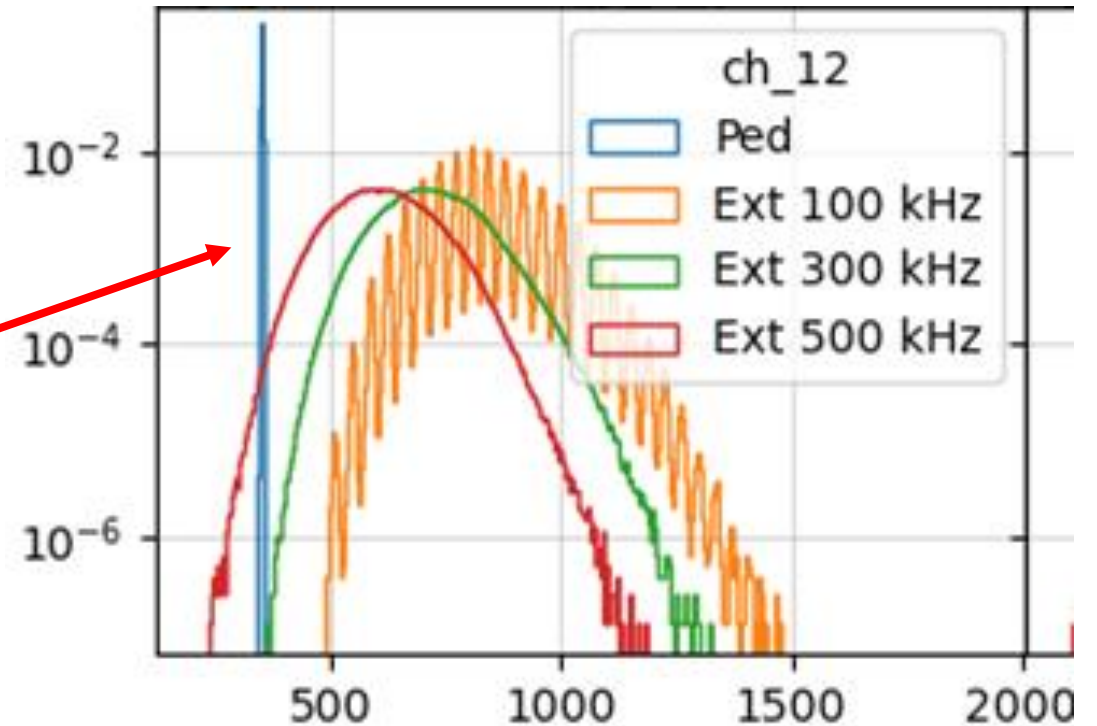
External trigger mode: **FPGA Trigger**

./beta.bin config -b MAX-0020 --asic_id 1 --i2c_freq 1 -c --cgain_hg 8 --cgain_lg 8 --cgain_sh_c2 8 -- cgain_sh_c3 8 --cgain_hg_lpf 8 --cgain_lg_lpf 8 -- timer_rst 1500 -t 0 255 1 255 2 255 3 255 4 255 5 255 6 255 7 255 8 255 9 255 10 255 11 255 12 255 13 255 14 255 15 255 --vref 32 --voff_pream 32 -- mux_drv 0 --mux_path 0 --timer_hold 930 --fpga_trg VF --trg_delay 100

VF = [0.1, 0.5, 1, 5, 10, 20, 50, 100] kHz

External trigger mode: **FPGA Trigger**

Laser directly on SiPM array Freq => 100 kHz

Threshold scan (Ch2)

The laser have a pulse frequency of 1 kHz and no external trigger was used by board

Internal trigger mode: **Threshold scan (Ch2)**

Configuration command:

./beta.bin config -b MAX-0020 --asic_id 1 --i2c_freq 1 -c --cgain_hg 8 --cgain_lg 8 --cgain_sh_c2 8 --cgain_sh_c3 8 --cgain_hg_lpf 8 --cgain_lg_lpf 8 --timer_rst 1500 -t 0 255 1 255 2 TH 3 255 4 255 5 255 6 255 7 255 8 255 9 255 10 255 11 255 12 255 13 255 14 255 15 255 --vref 32 --voff_pream 32 --mux_drv 0 --mux_path 0 --timer_hold 930
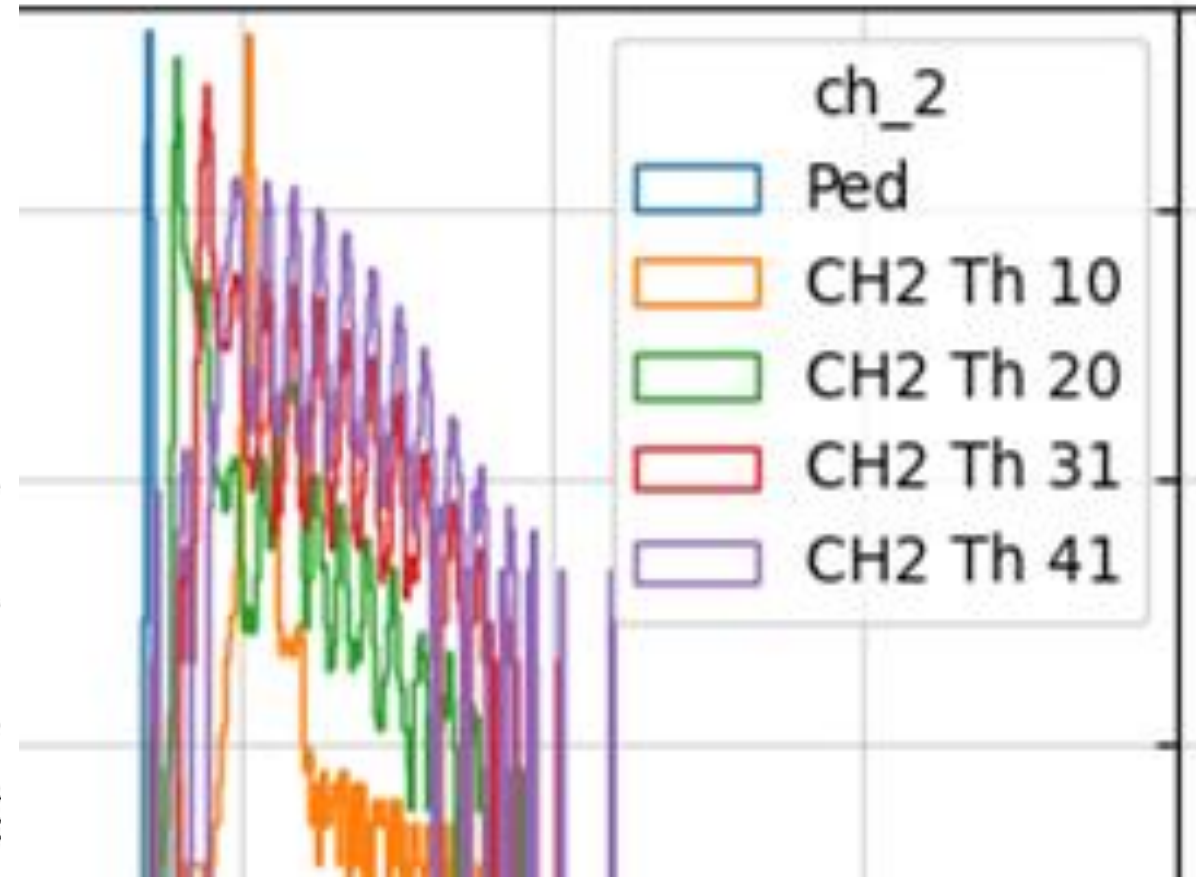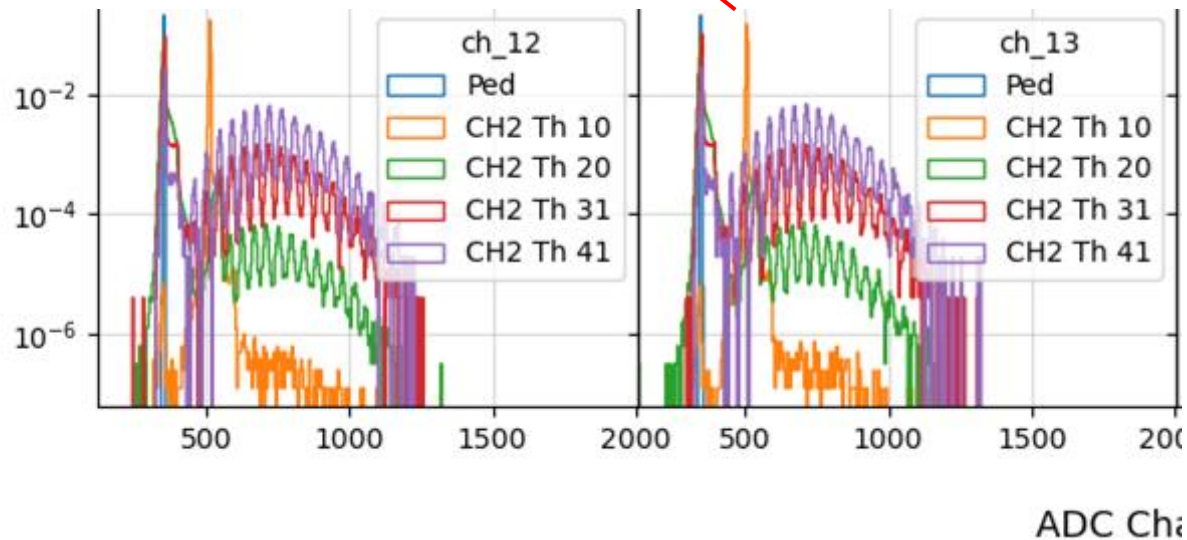
TH = [10, 20, 31, 41, 51, 71, 91, 111, 131, 151, 181, 211, 231, 251]

- **Sometimes using specific thresholds, the acquisition software makes a segmentation fault.**

Internal trigger mode: **Threshold scan (Ch2)**
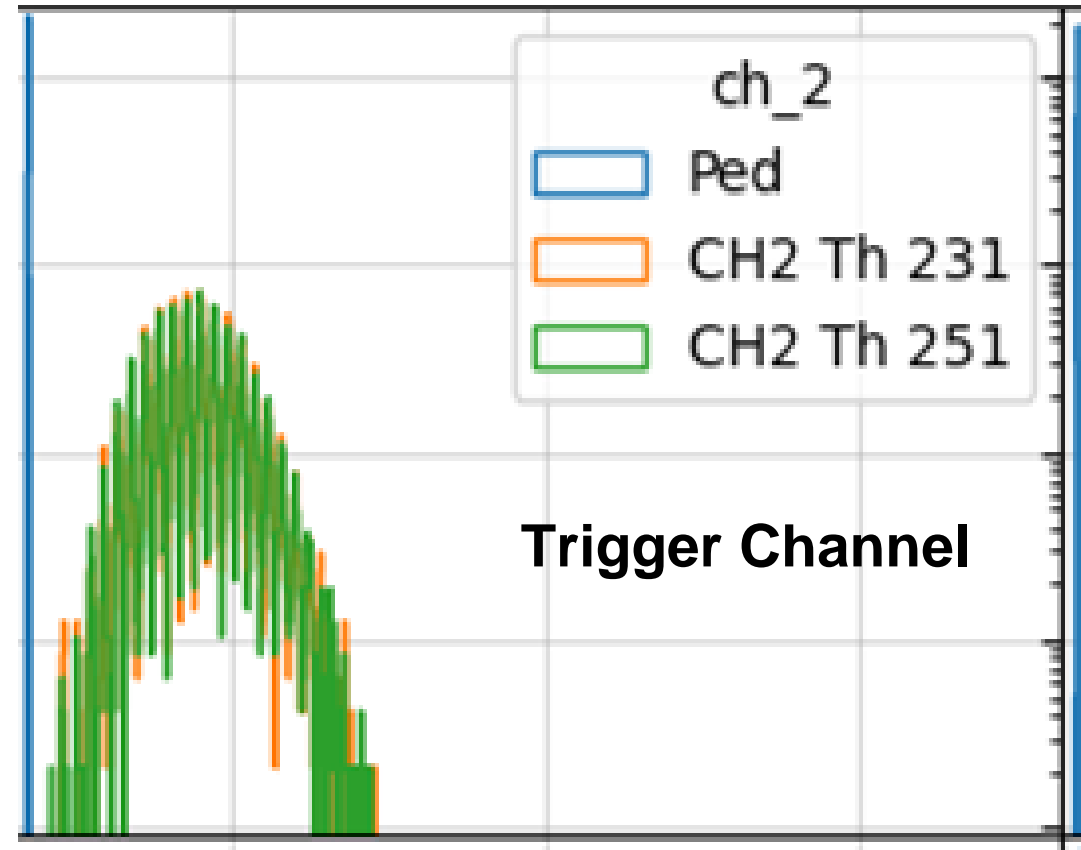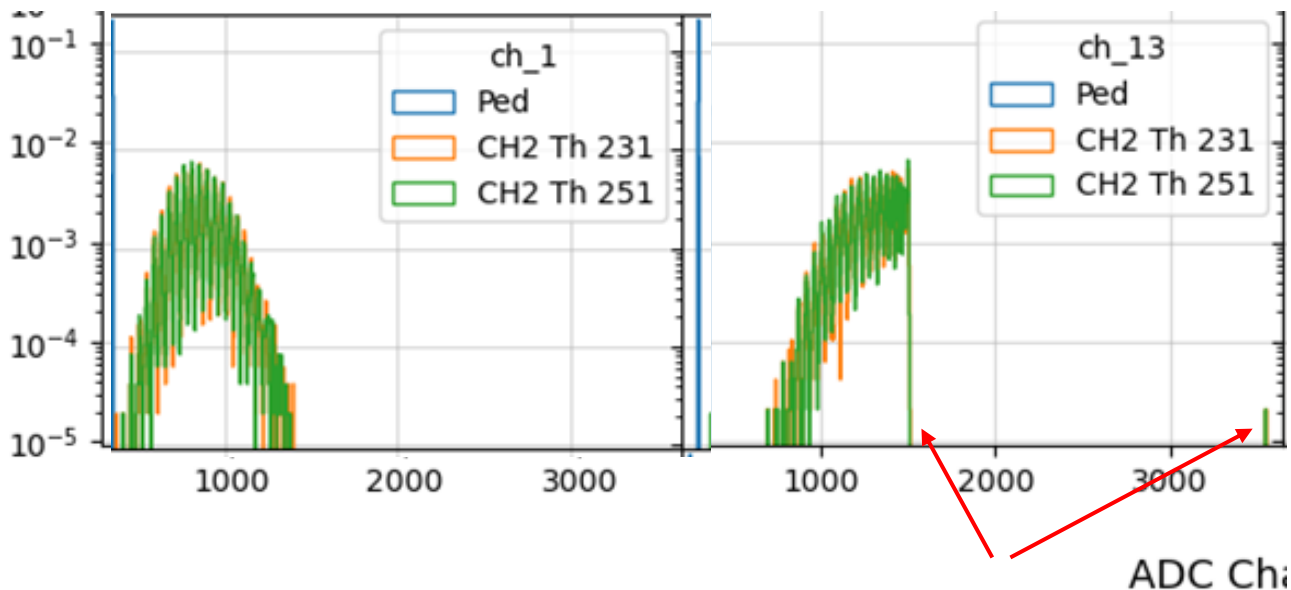
Laser directly on SiPM array (Low Threshold)

Strange peak for low internal trigger threshold. (Increase VFS and TEMP)

Internal trigger mode: **Threshold scan (Ch2)**

Laser directly on SiPM array (Higher laser intensity than previous slide)


Not in trigger channels

Trigger Channel

The "saturation" change ~1500 ADC channel and probably switch on the low gain???

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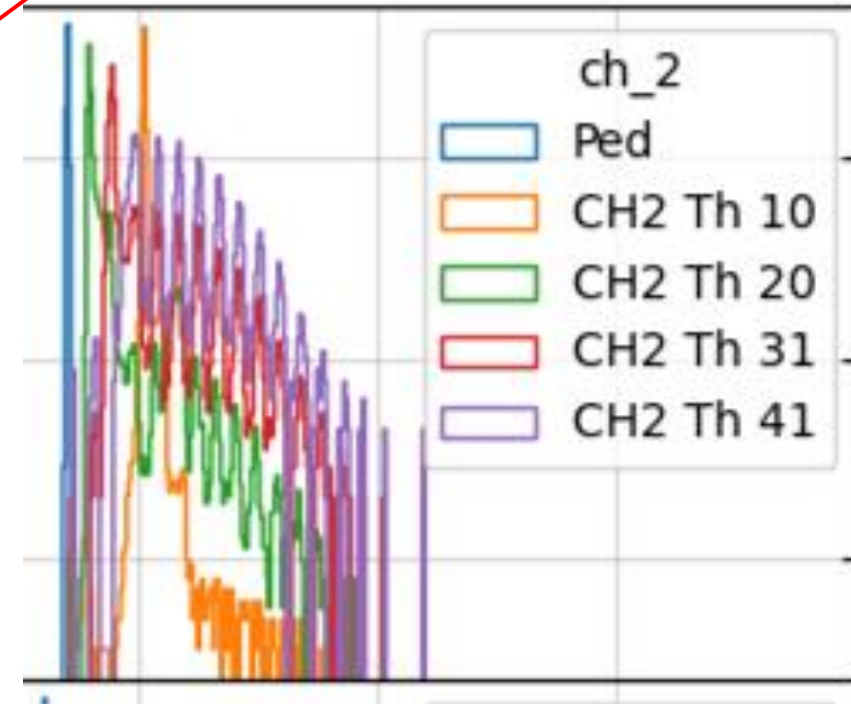
Back-Up Slides

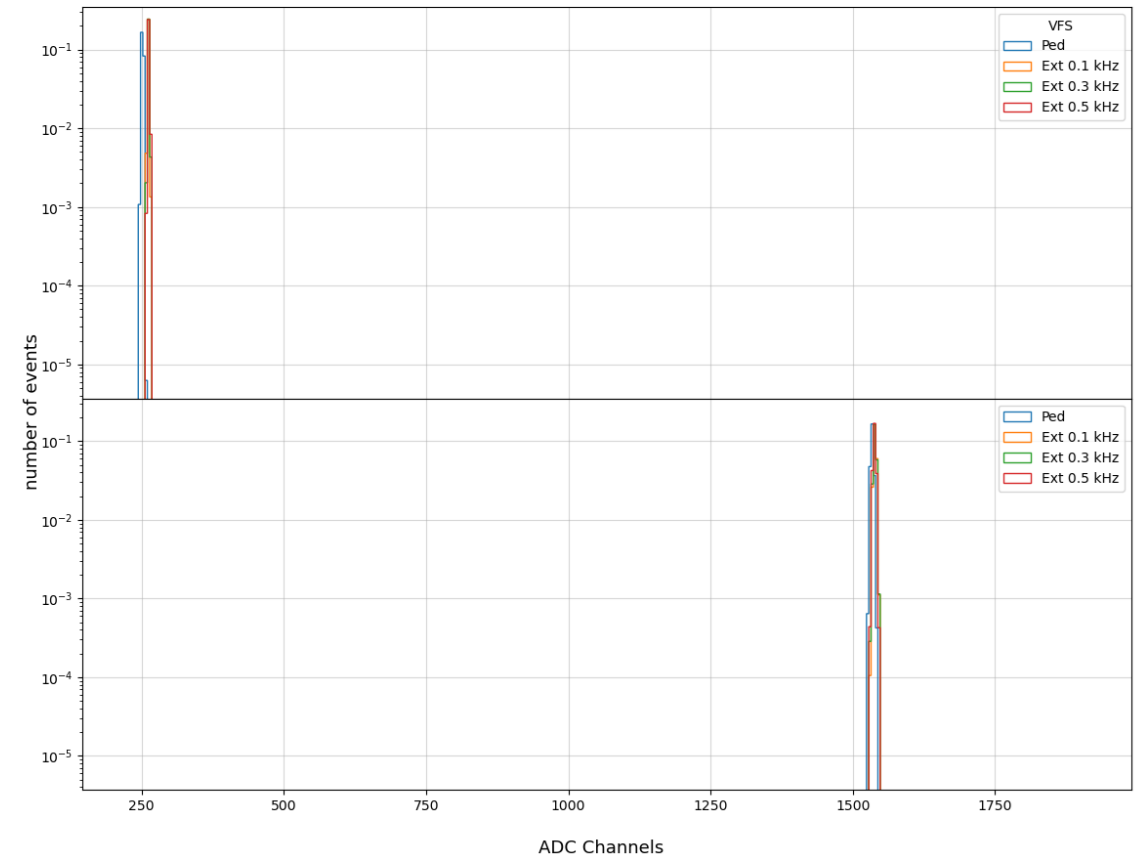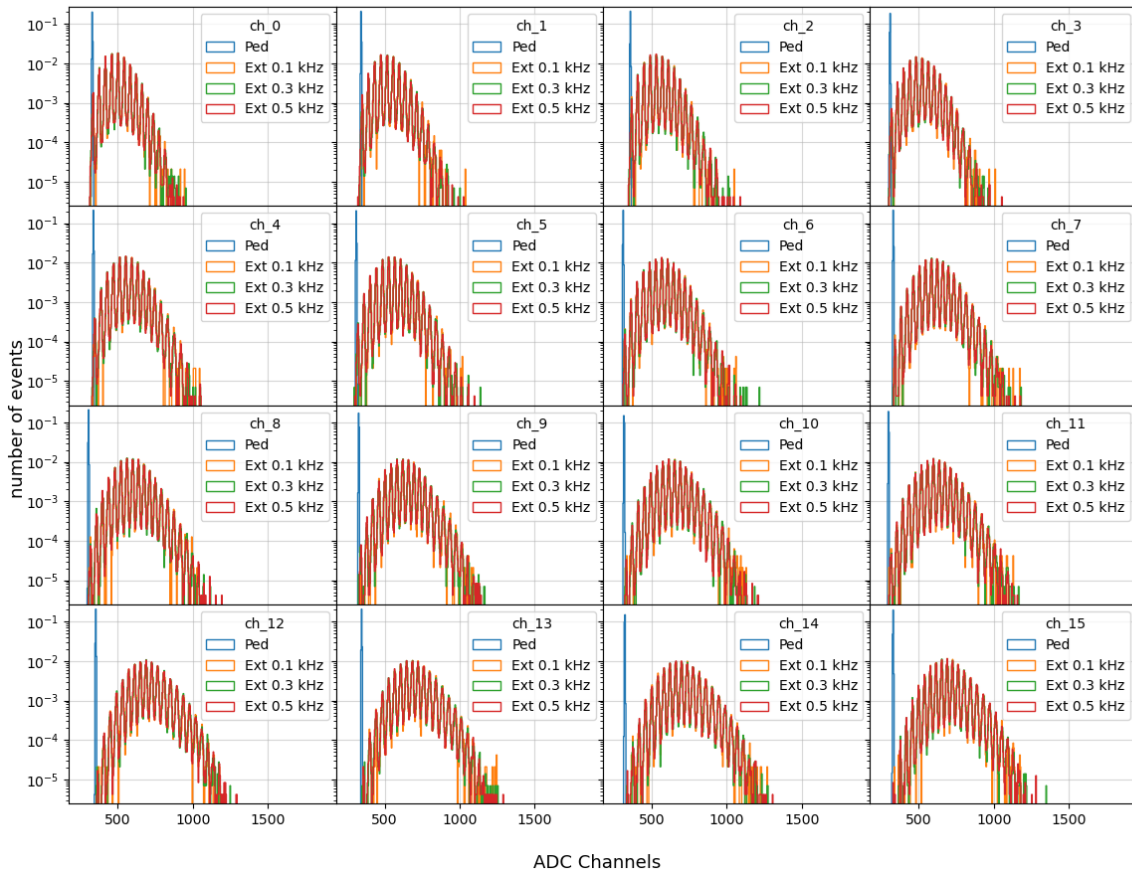# Trigger threshold studies (Int trigger Ch2)
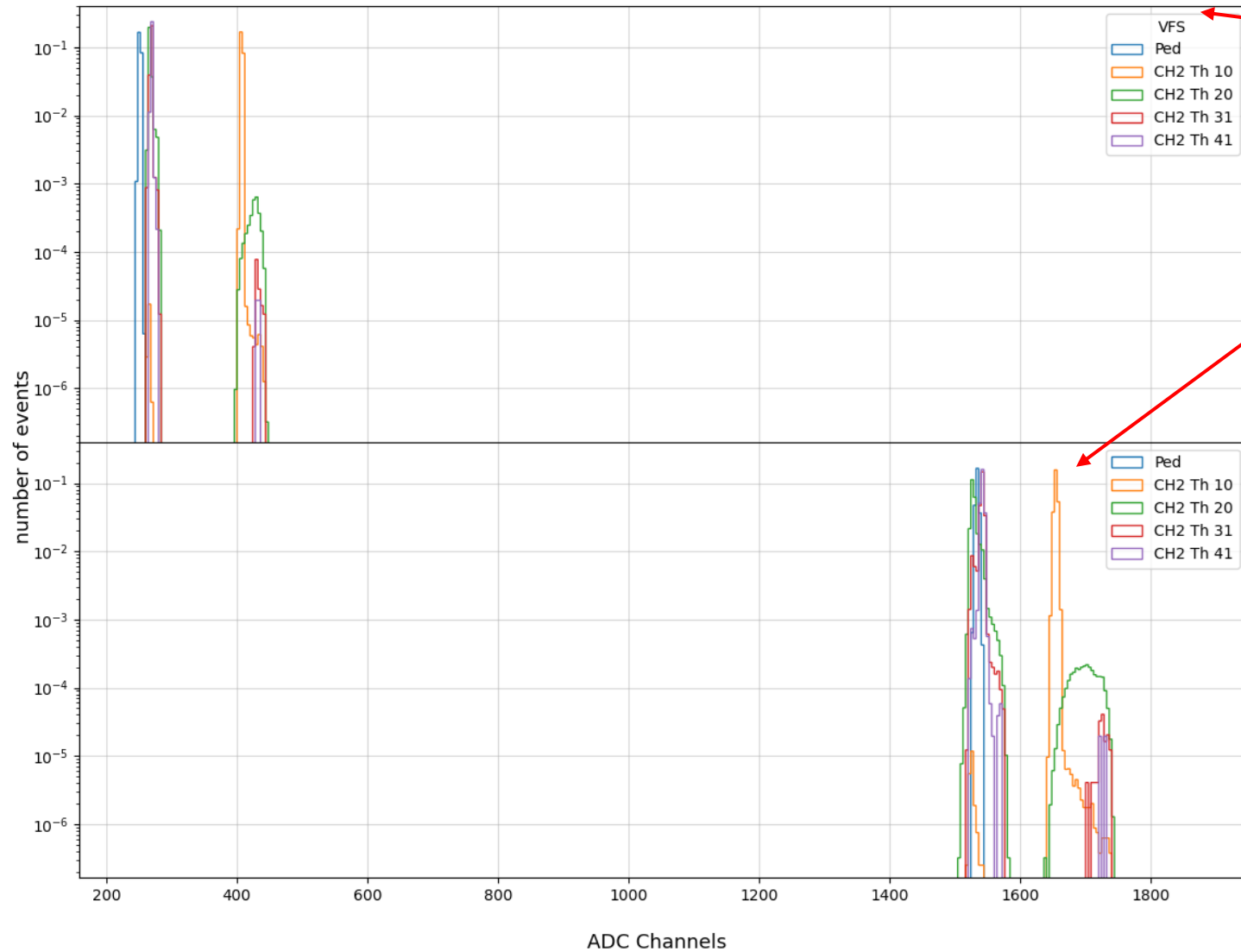
The value of VFS and TEMP change in shape and the value in the acquisition with lower thresholds (and higher trigger frequencies)
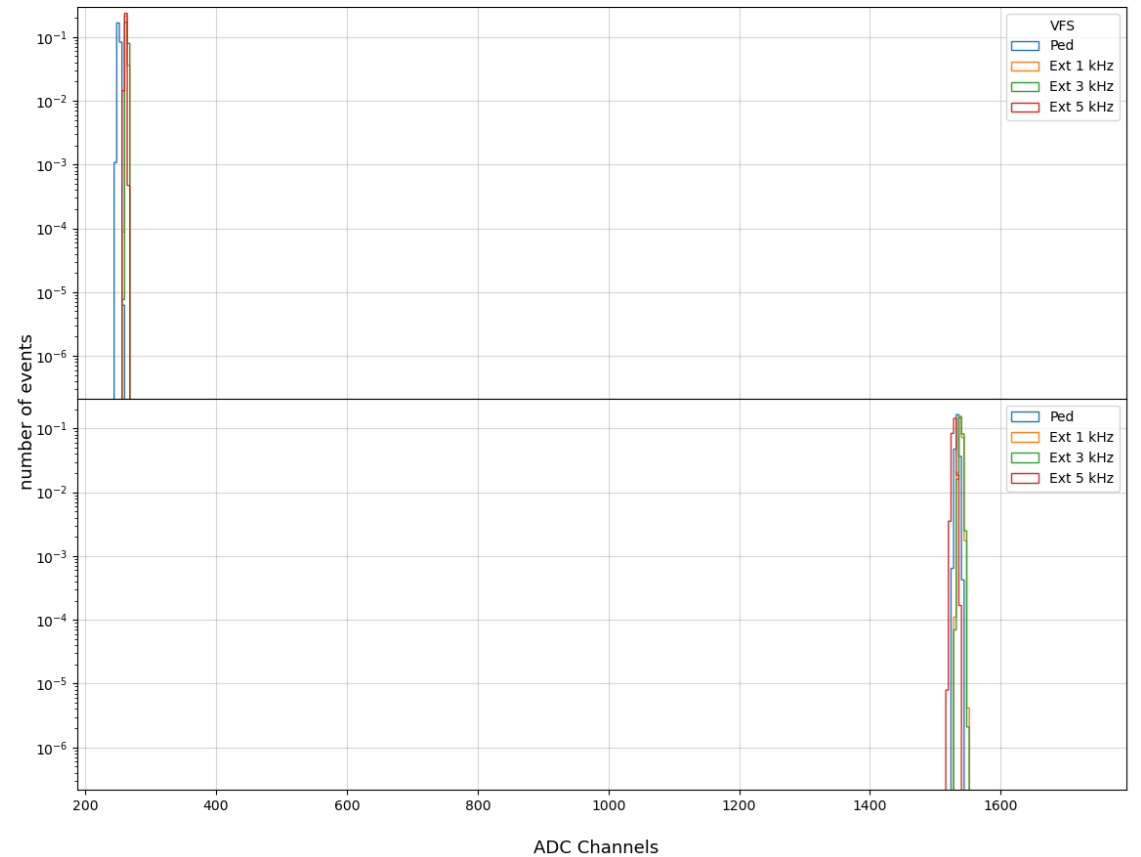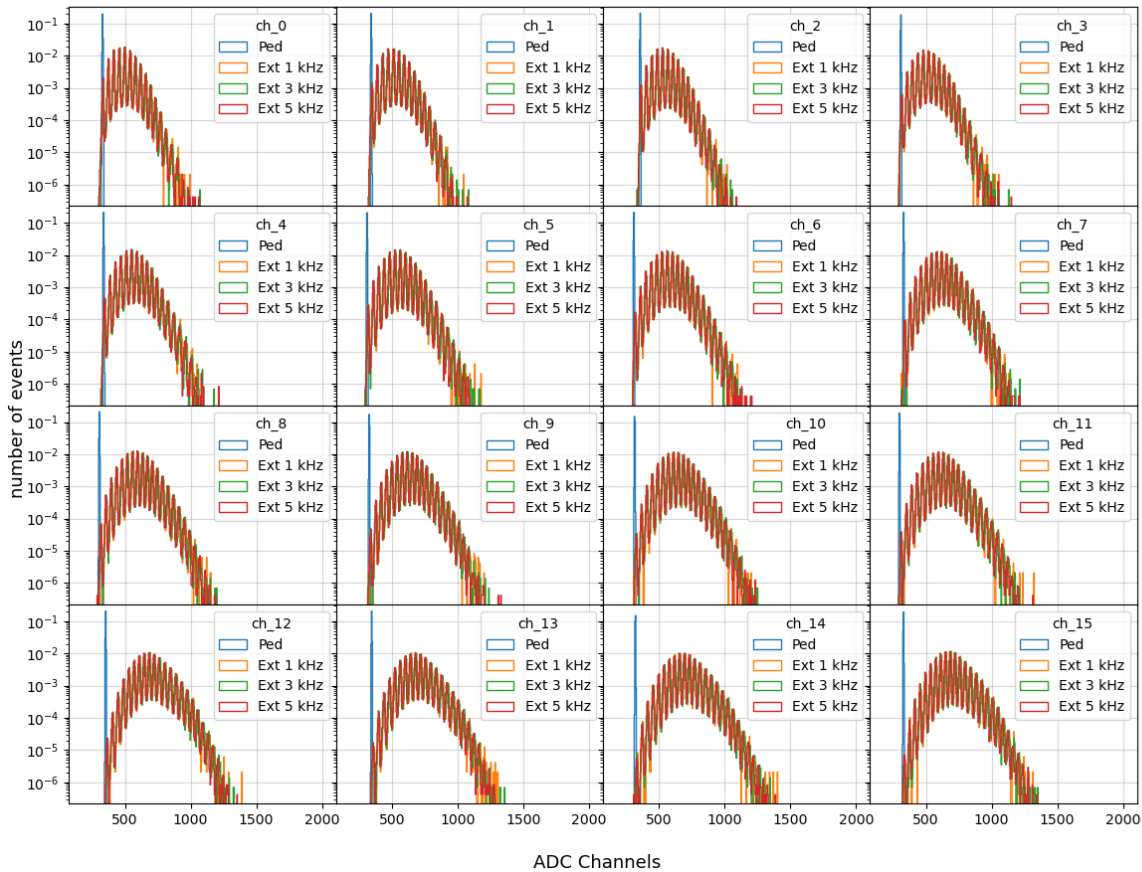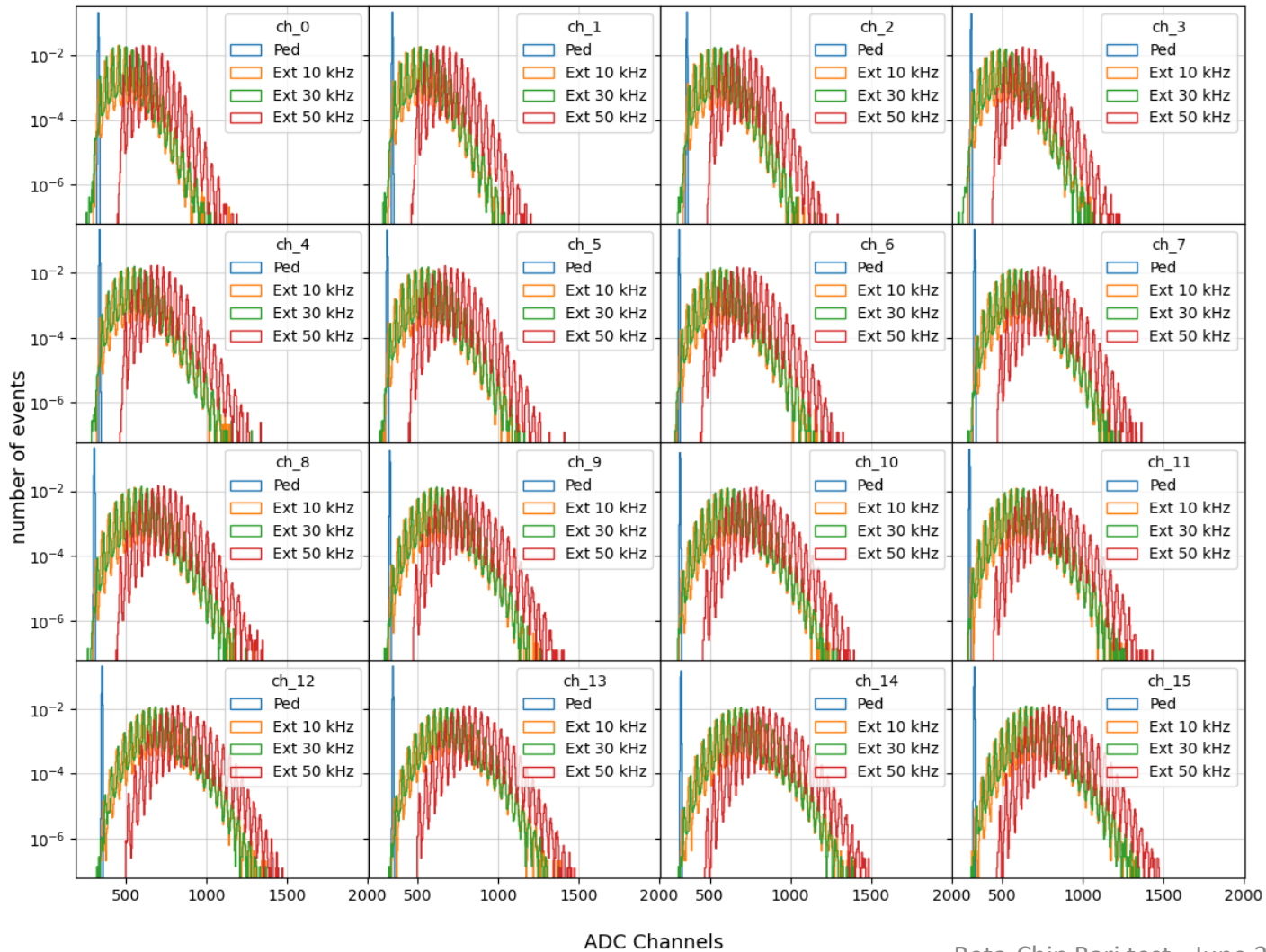
Laser directly on SiPM array lower threshold
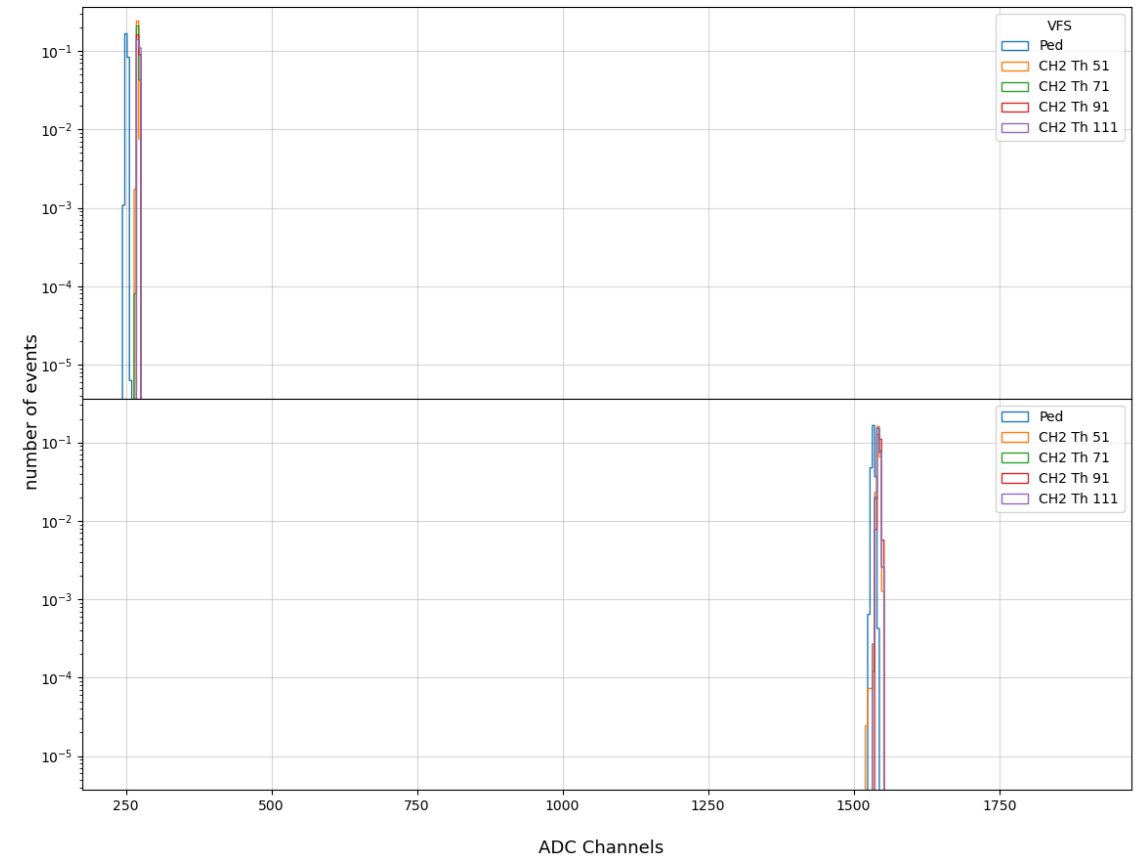
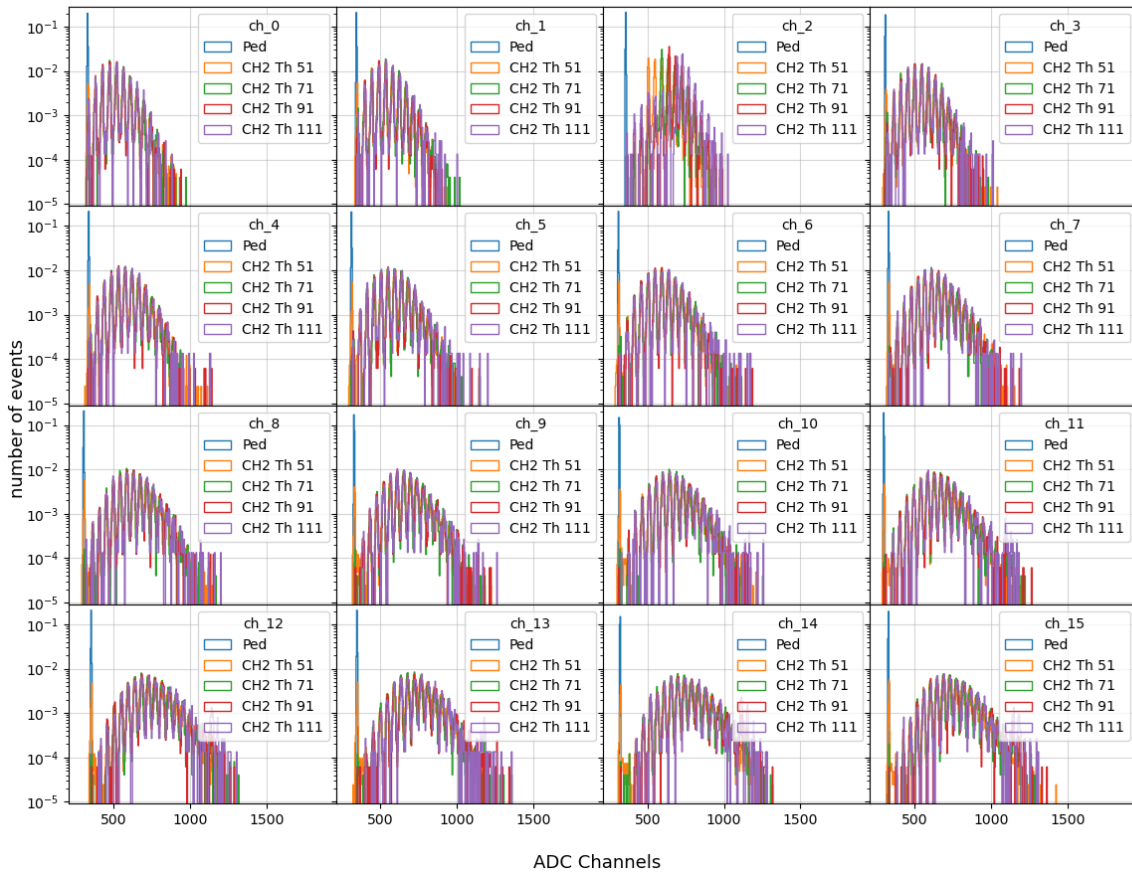# External trigger mode: **FPGA Trigger**

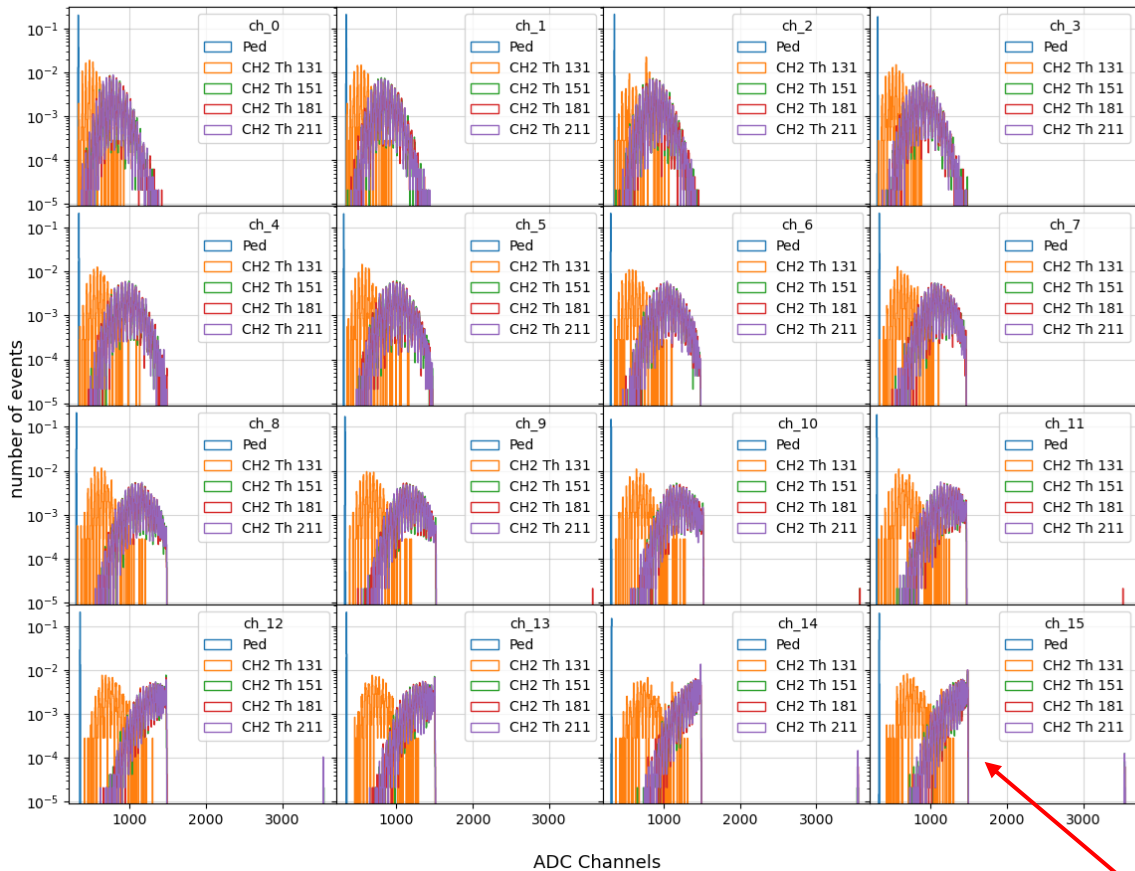# External trigger mode: **FPGA Trigger**

External trigger mode: **FPGA Trigger**

Trigger threshold studies (Int trigger Ch2)

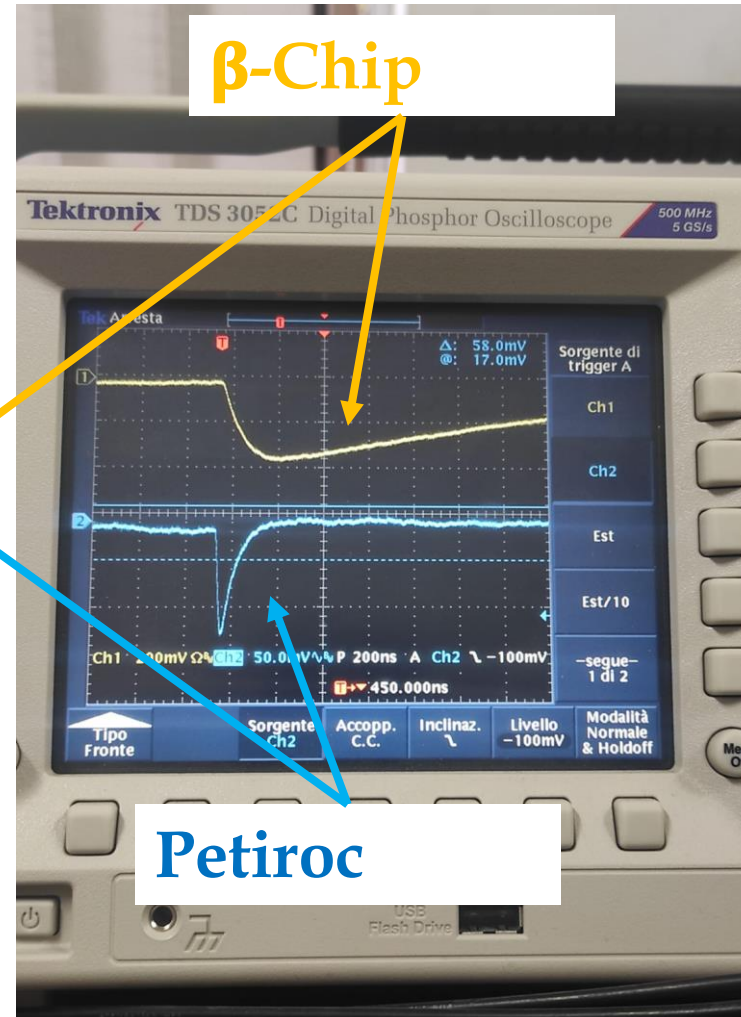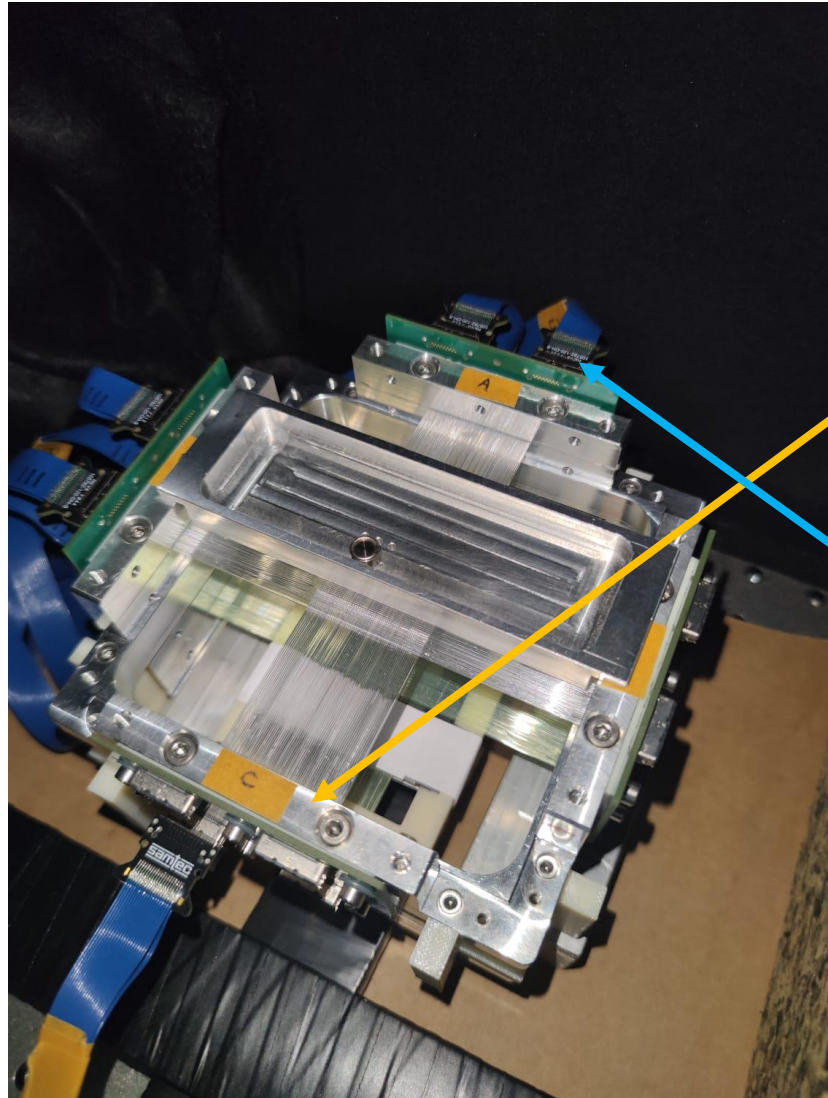# Trigger threshold studies (Int trigger Ch2)

From Th 151 we have increased the laser intensity

Measurements with Sr90 source

β-Chip

Petiroc

Triggered with oscilloscope

- **SiPM arrays to both ends of the fiber tracker**
  - One side read-out with PETIROC
  - The other side read-out with Beta-chip
- **Since the Beta-chip does not accept external trigger, we have used the Beta-chip trigger signal to force the readout of the Petiroc board**
  - The current firmware of the beta-chip does not allow to synchronize the two systems

Measurements with Sr90 source

Single SiPM channel

Sr90