PSD – PS Beam Test 2022

FABIO



The main goal of this beam test is to check the whole DAQ chain before the SPS beam test with ions in late November (23-29 November)

PSD protoype

Short bar with trapezoidal face



We plan to build:

- 4 short bars 40 cm long
- 4 short bar 30cm long

And then assembly two orthogonal planes

4 bars will be machine in Bari2 bars will be machine in Lecce2 bars will be machine in GSSI





GSSI will take care of the mechanics of the prototype

SiPM

► We plan to equip each bar with different SiPMs



1 x \$14160-1315PS

The SIPMs on the two sides will be mounted on PCB fixed in supporting endcaps

The SiPMs on the top of the bars will be mounted on PCB with 3 SiPM each

S14160-3050HS (TSV Tecnolgy) will me mounted on a dedicated PCB

All the SIPMs will be glued on the scintillator surfaces

1 x \$14160-3015PS

Readout

- Each bar will have 5/6 readout channels
- ► The total number of readout channels needed is 8x6=48
- The BetaChip evaluation board that we plan to use has 32 channels that can be used for this test
- We plan to use both BetaChip and Citiroc chip (CAEN DT5550W) to readout and compare the results

Trigger system



2 «fingers» H-V 100x10x5 mm to define a small area

1 Tile 100x100x10 with a central hole (2 cm diameter)

2 Tile 100x100x10 for all particles trigger

Each plastic scintillators has a double readout to reduce the effect of self trigger due to the dark noise of SiPM

SiPM Advansid NUV 3x3mm2 40um cell Adanvasid TransImpedence amplifier with analog signal fed into DT5495 CAEN



Trigger logic

The trigger logic already implemented in DT5495 with SciCompiler (already used in 2021 beam tests)



The implemented logic will provide a trigger signal (NIM and/or TTL) in 50ns (TBC)

The trigger logic could handle Spill signal from the PS machine and the busy signals from all the subdetctors.

The trigger could be provided to the Chinese Main Trigger board



CITIROC Chip

- We will use the same DAQ system used in the 2021 beam tests
- The CITIROC will work in autotrigger mode (AND between adjacent channels) and the Trigger System will provide the acknowledgment signal.



In the example two signal have been acquired since the acknowledgment signal is arrived in the defined time window

Beta Chip

- Some desiderata to be added to the evaluation board
 - External trigger input (NIM or TTL)
 - Busy output
 - AND logic between chip
 - Possibility to start and stop the acquisition via a command broadcasted TCP/IP

▶ ...



Action item

- Production of scintillating short bars
 - ► BARI, GSSI, LECCE
- Design of the beam test mechanics
 - GSSI
- Setup of triggering system
 - ► BARI
- Set-up of CITIRCO DAQ chain
 - ► BARI, GSSI, LECCE
- Set-up of BetaChip DAQ chain
 - ► ICCUB
- CNAO beam test logistic
 - ► PAVIA
- CERN beam test logistic
 - ► BARI, GSSI