Top tracker electronics: read out board and the rest

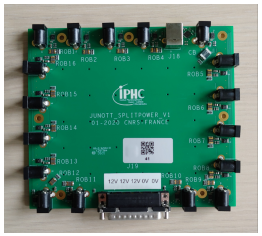
Alessandro Paoloni on behalf of
LNF Group (AP, Agnese Martini, Giulietto Felici, Lucia Votano)

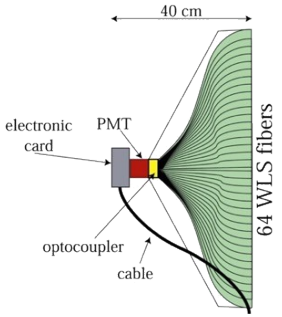
Meetings dei gruppi italiani di JUNO

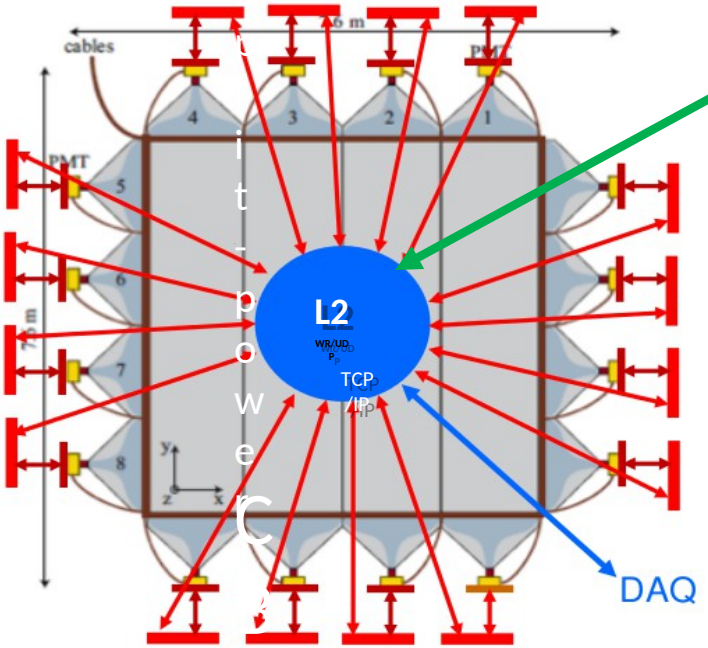
Milano 5-6 May 2022

TT wall read-out electronics

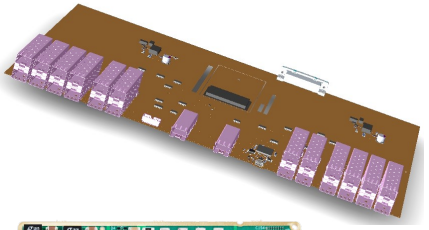
Split power





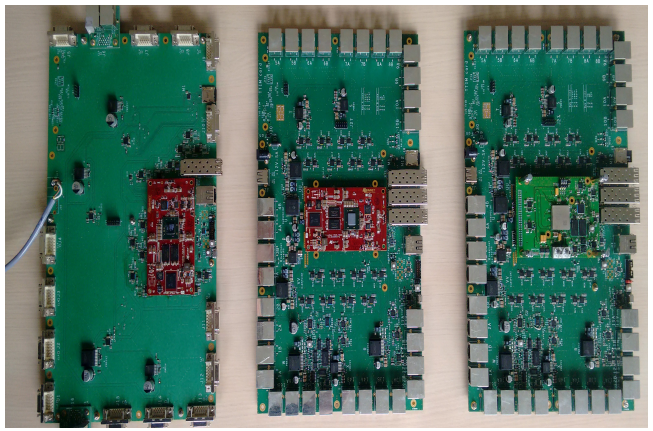


L2 trigger (GTB)



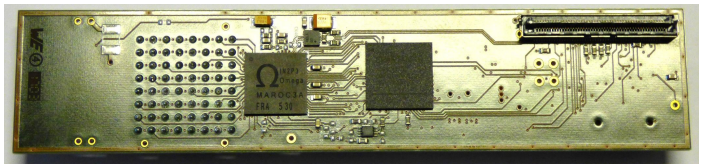
H7546 Hamamatsu
64 ch MAPMT

Concentrator Board



Boards with LNF involvment

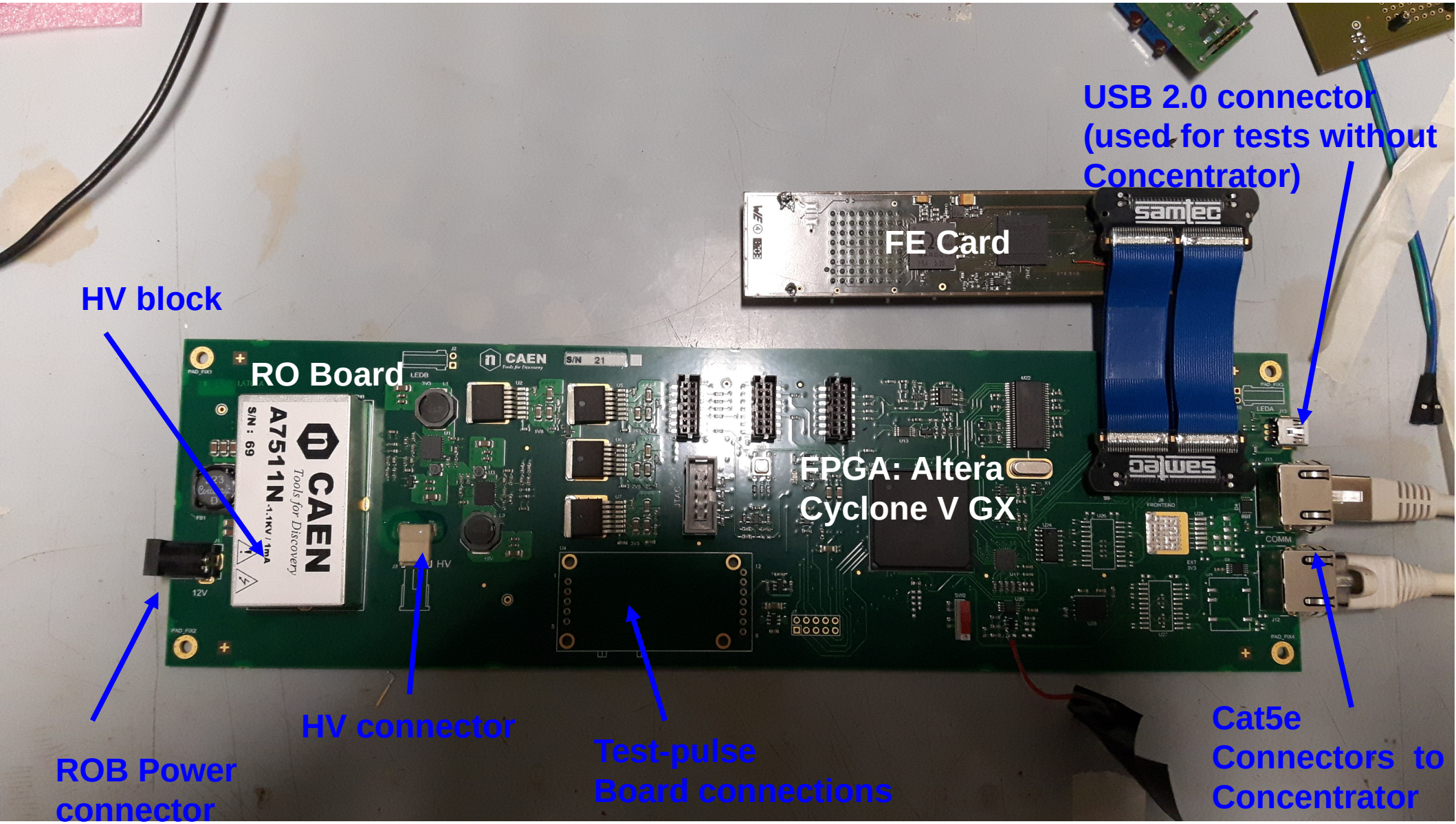
Front-End Board



System in numbers:
1000 FEB+ROB
63 Concentrator + Split power boards
1 L2 GTB
+ power supply + cabling

TT endcap:
Read-out and
Front-End Boards

Final prototype Read-Out Board picture



Set-up @ Strasbourg

New: Tests with prototype concentrators at Strasbourg, during November 2021, both on detector prototype and on test-bench.

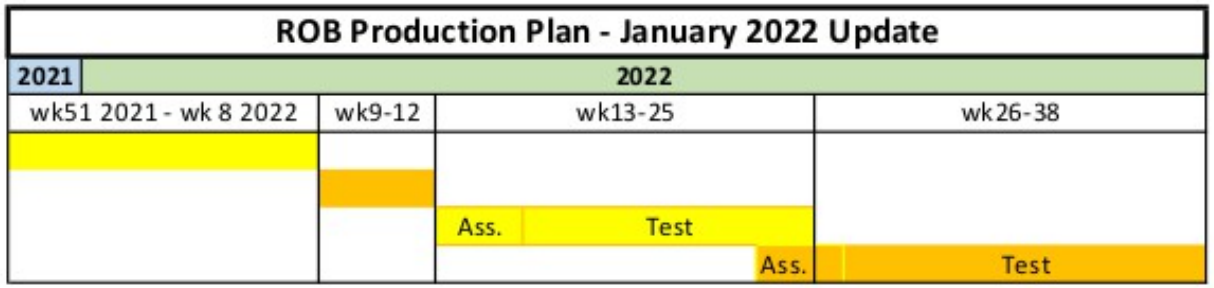
Test bench with 16 ROBs + Concentrator (realistic cabling and power)

Small detector prototype

ROB hardware frozen in December 2021 upon last agreed modifications.
Spare communication lines for possible future Architecture upgrades.

Schedule (from CAEN)

	Start	End
Pre-serie of 20 units Assembly	23/12/21	25/02/22
Pre-serie of 20 units Qualification Test	28/02/22	25/03/22
1st Bunch Assembly and Test (500 units)	28/03/22	24/06/22
2st Bunch Assembly and Test (500 units)	14/06/22	23/09/22

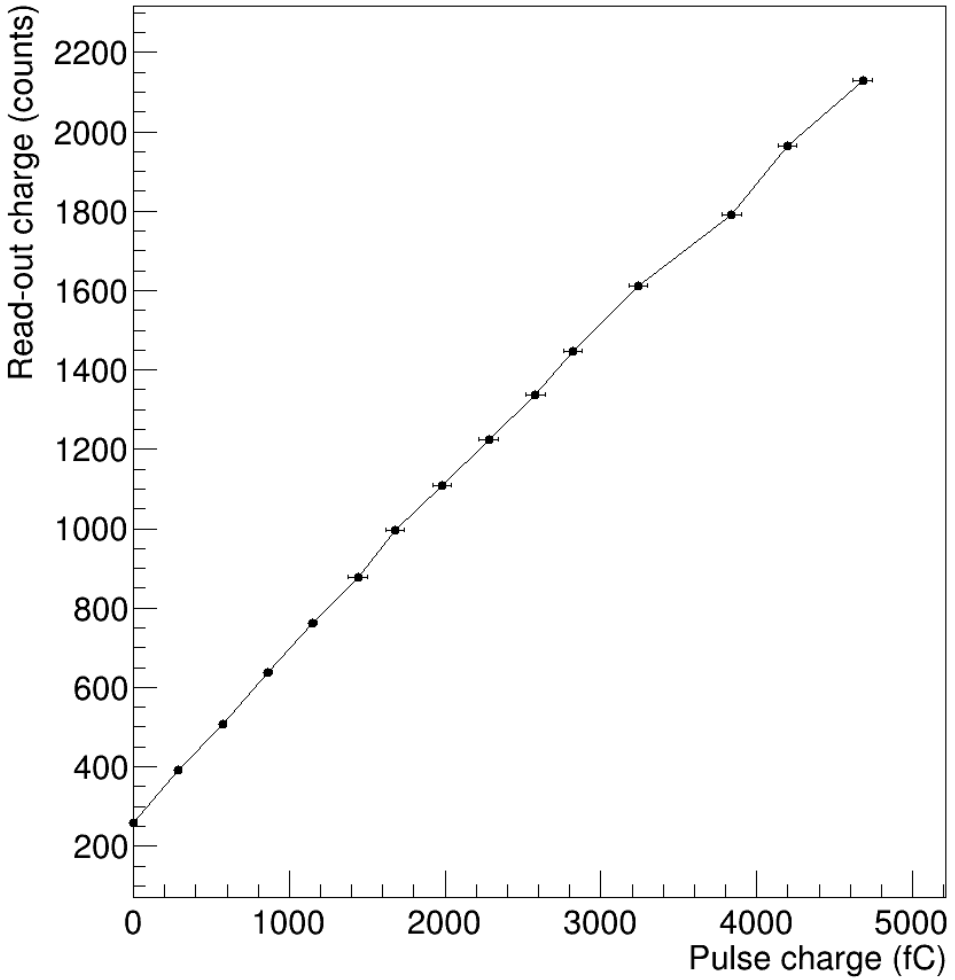


- **Preproduction of 20 boards ready at the end of February.**
- **First 500 boards ready and tested at the end of June.**
- **Last 500 boards ready and tested at the end of September.**

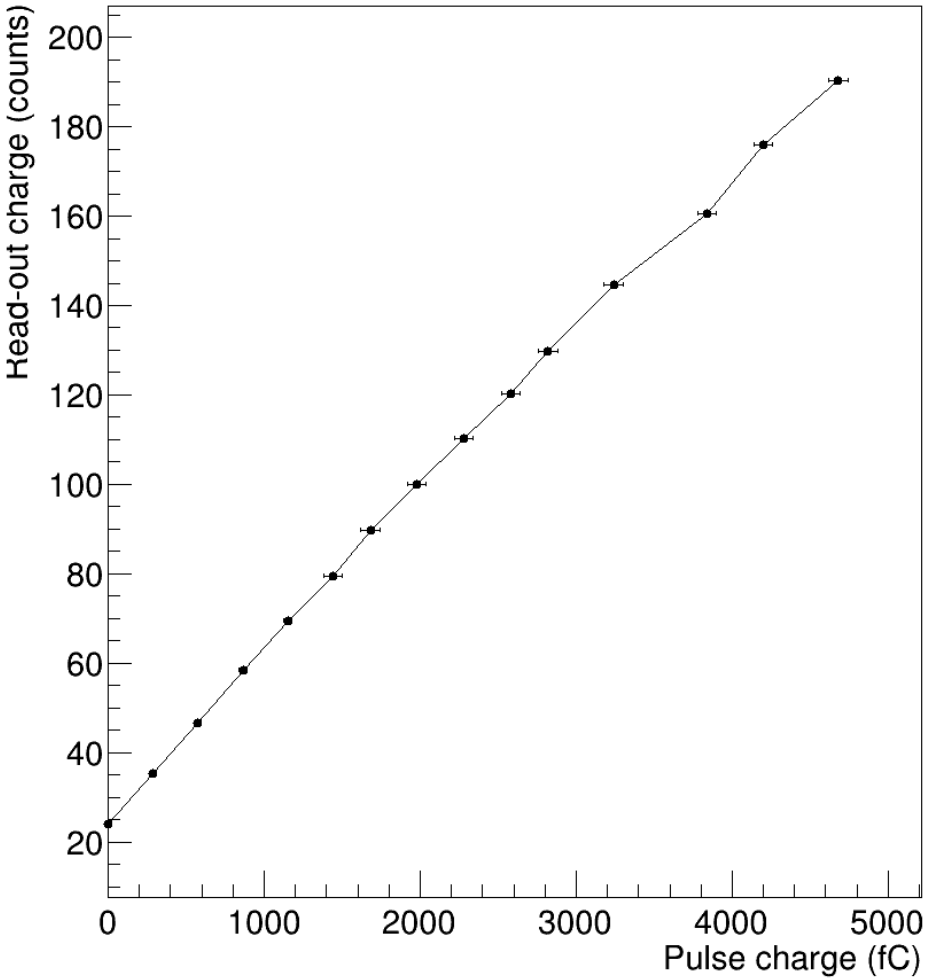
Preproduction Boards tested during April at CAEN and LNF: so far no problem observed.
Defined test protocol @CAEN (whole production) and @LNF (subsample of 100 boards).
Firmware almost ready (only missing FPGA of FEB and ROB re-flash).
Order of 16 boards for Strasburg set-up under placement.

LNF Final prototype tests

Flash ADC calibration

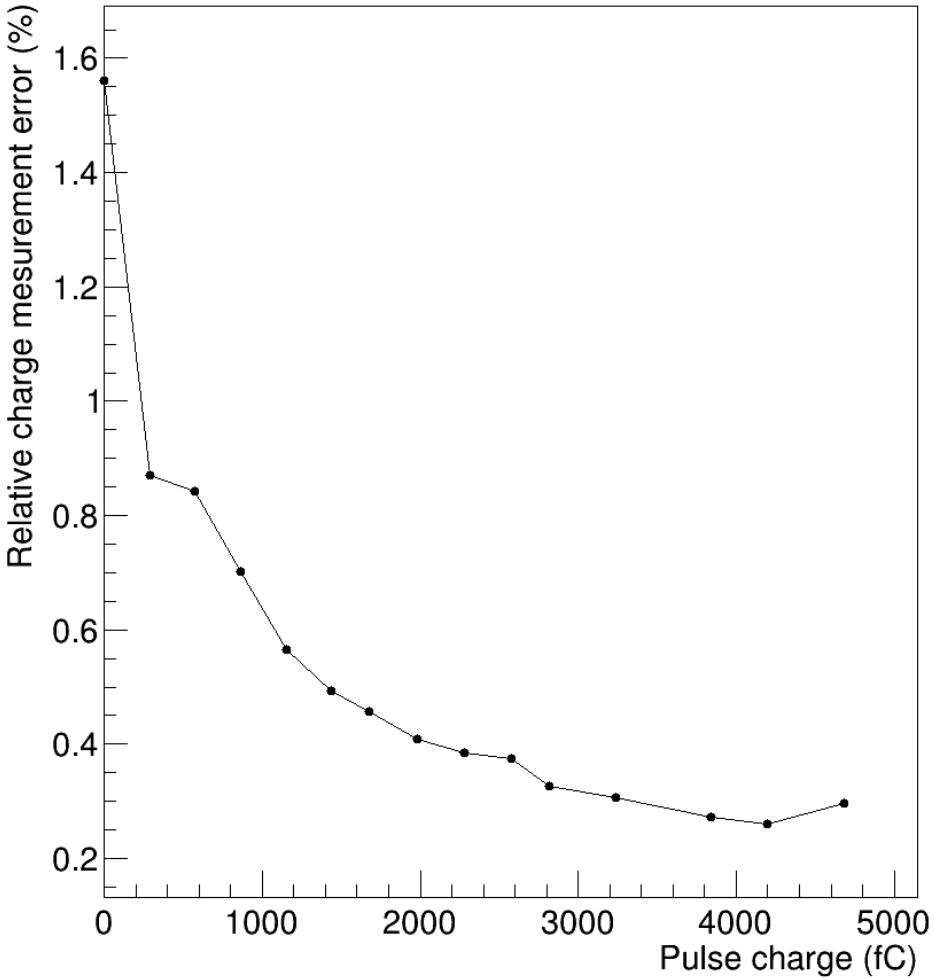


Wilkinson ADC calibration

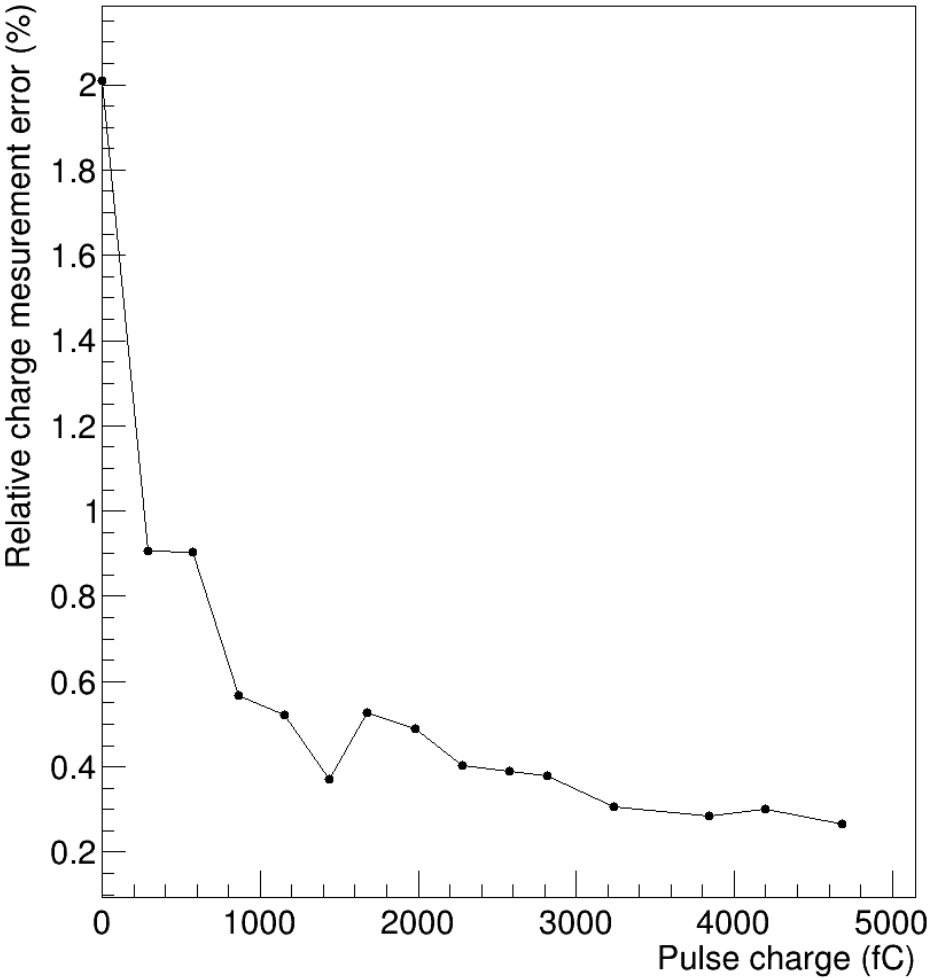


LNF Final prototype tests

Flash ADC precision

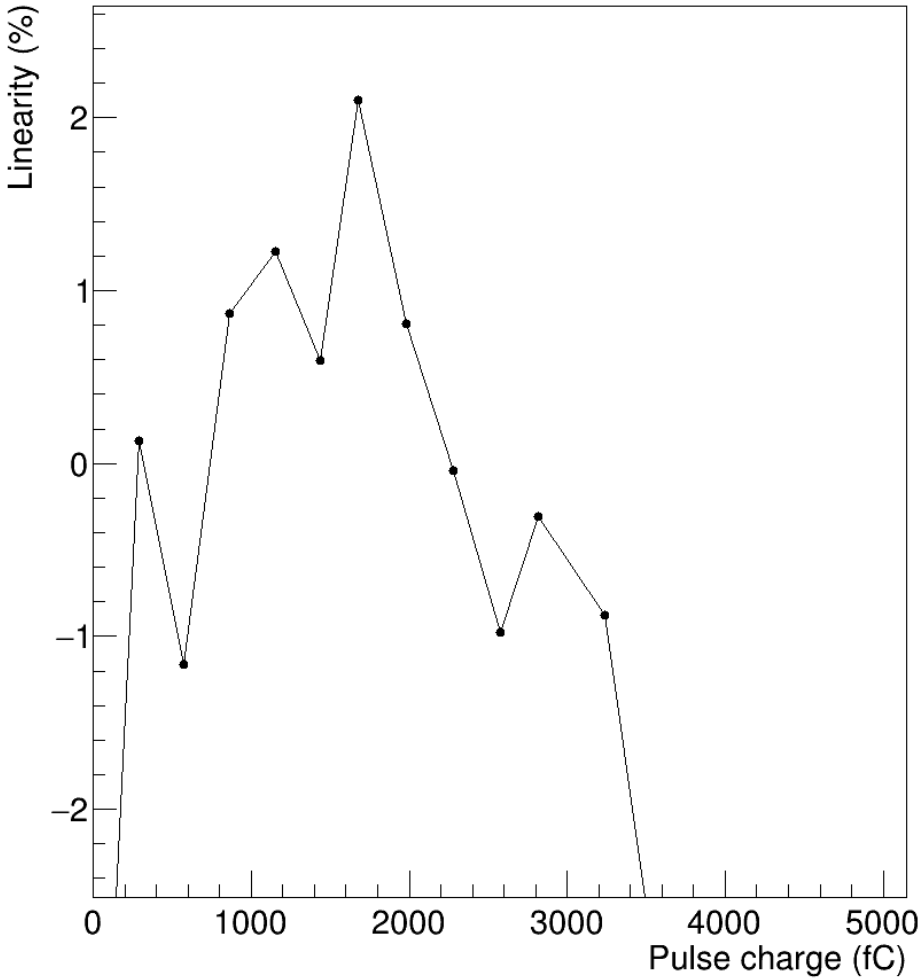


Wilkinson ADC precision

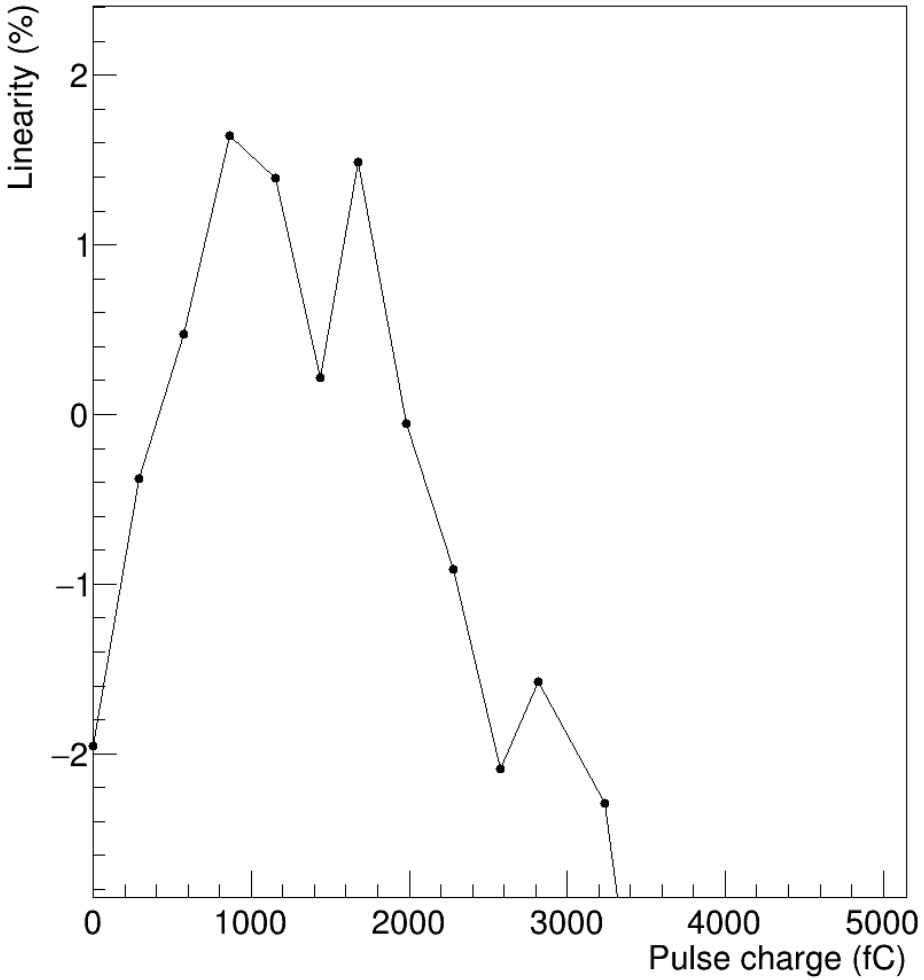


LNF Final prototype tests

Flash ADC linearity



Wilkinson ADC linearity



And in addition..... DAQ running over days without stops.

ROB Test protocol

1) LV levels verification
2) FPGA registers set to default values verification
3) MAROC3 setting
4) HV output measurement for a fixed Vset
5) LV level verification for LED light pulse intensity
6) Verification of DAQ functionality for different modes (Pedestal, calibration, Wilkinson, Flash, Zero-suppression, Hit pattern and Trigger rate tests)
7) ADCs response to fixed amplitude (@CAEN only of Flash ADC, @LNF on both using a FEB).

The rest.....

Concentrator: Money allocated. SOM board ordered apart (by Strasbourg).
Tender specifications for the motherboards+components+mounting drafted.

Cabling: waiting for Dubna group engineers to draw cable trays on system CAD.

ROB expedition ???? waiting for reply from IHEP.