Development of Modified 3D Detectors at FBK

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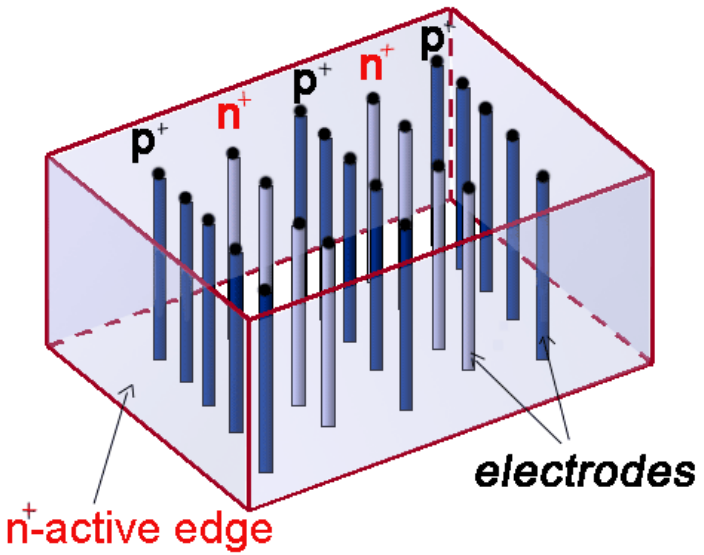
Outline

- Introduction
- 3D Double-Type-Column detectors
- 3D-DDTC^{+} (passing through columns)
  - Technology
  - Design options
  - Preliminary results
- Conclusions

3D detectors - State of the Art

First proposed by S. Parker et. al. in NIMA 395 (1997), 328



Best result:
66% of the original signal after
8.8×10^{15} cm^{-2} 1-MeV $n_{eq.}$ fluence

C. Da Via et. al.
NIMA 604 (2009) 504

ADVANTAGES:

- Electrode distance and active substrate thickness decoupled:
  - Low depletion voltage
  - Short Collection distance
  - Smaller trapping probability after irradiation

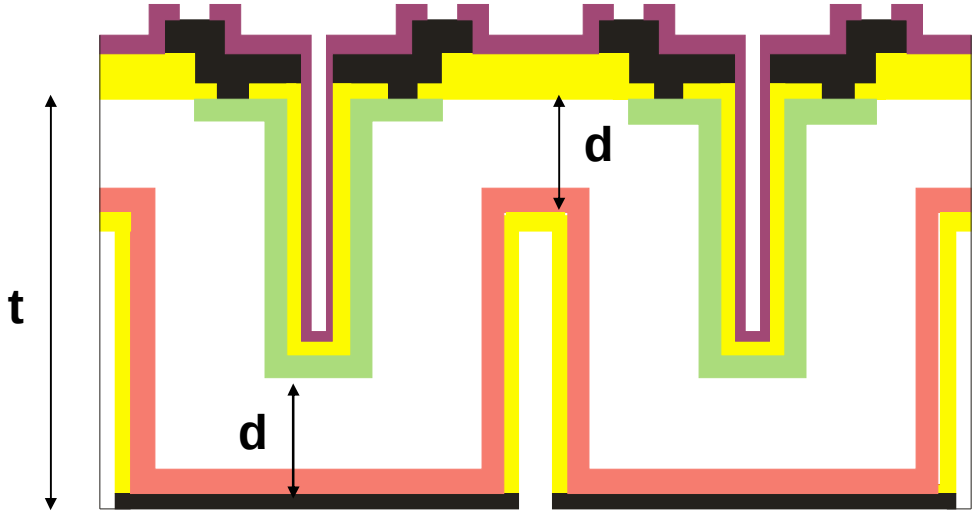
→ **High radiation hardness**

-Active edges:
  - Dead area reduced up to few microns from the edge

DISADVANTAGES:

- Non uniform response due to electrodes
- Complicated technology
- Higher capacitance with respect to planar

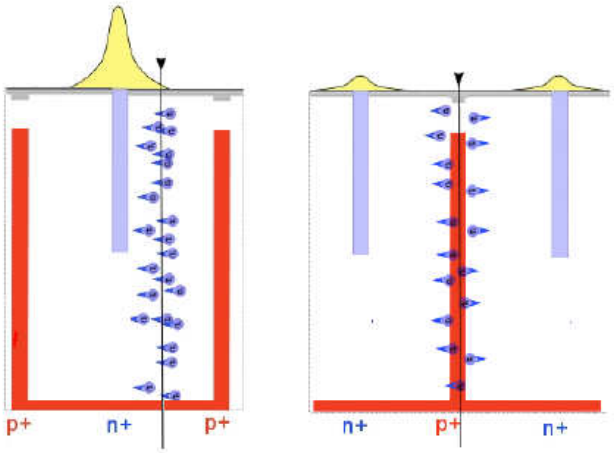
3D – DDTC detectors



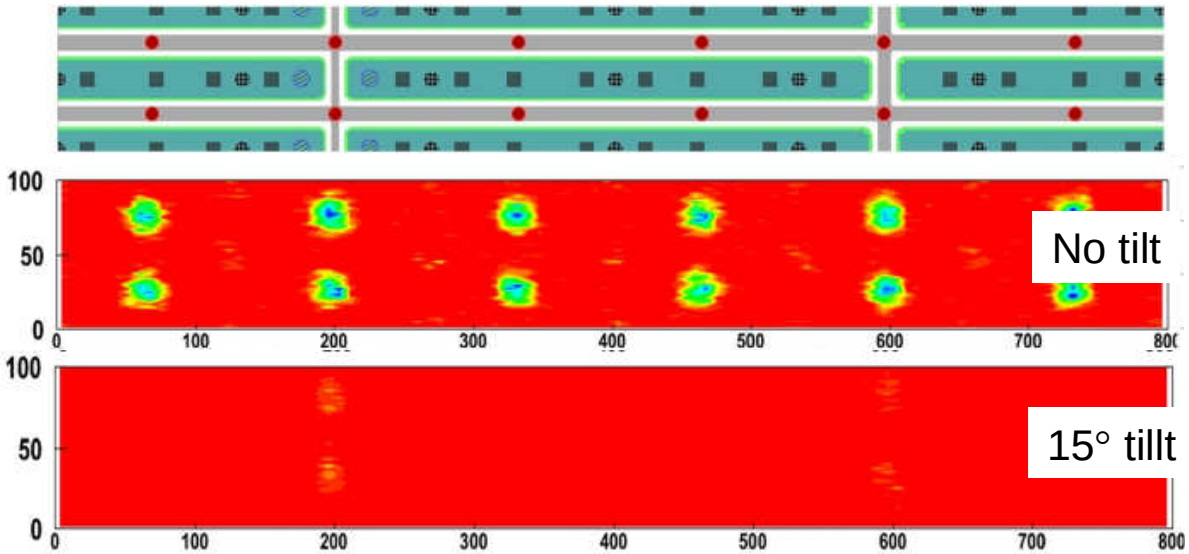
G.F. Dalla Betta et al., NSS2007

- To ease fabrication:
  Double-side process
- No support wafers
- Holes (~10 μm diam.) are "empty" (no poly-Si)

A. Micelli et al., Pixel 2010



Hit efficiency maps in 3E sensor irradiated with protons at 10^{15} n_{eq}/cm^2



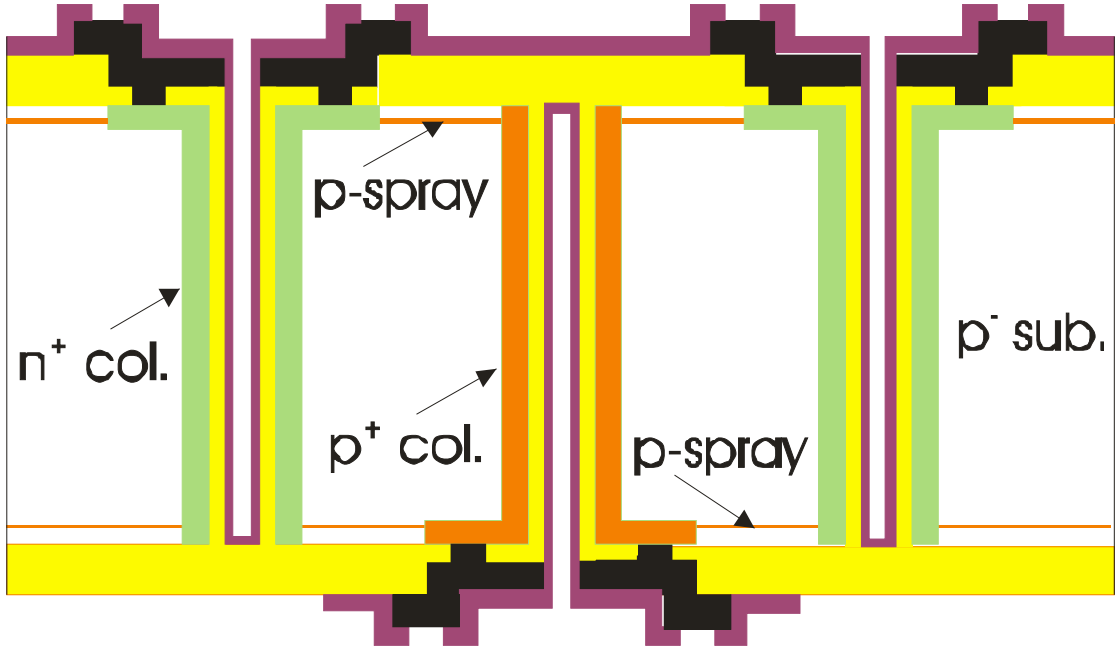
3D-DDTC: pros and cons

- fabrication process reasonably simple
- good process yield
- even with non optimized gap “d”, good performance up to irradiation fuence of 10^{15} n_{eq}/cm^2

- column depth difficult to control and to reproduce
- insufficient performance after very large irradiation fluences if “d” is too large

Next step ⇒ Modified 3D-DDTC process with passing through columns

3D-DDTC^{+}: passing through columns



Process aspects

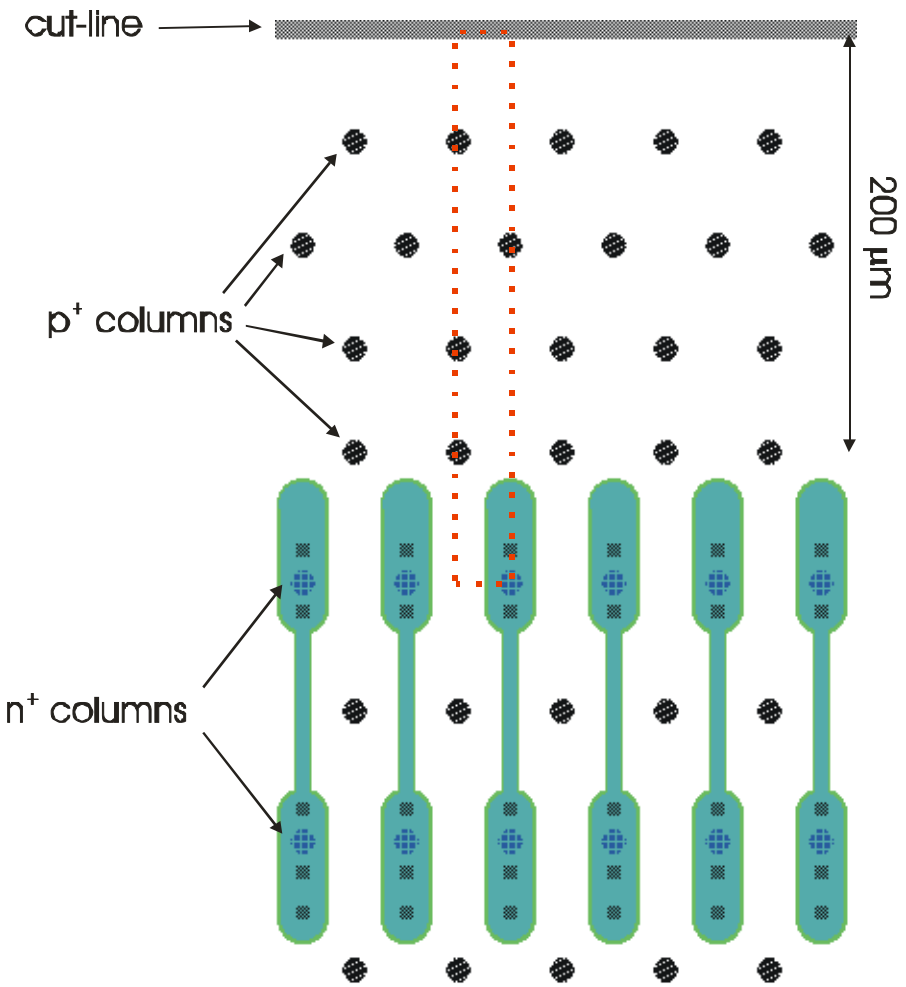
- Full double side process
- Column etching stops at thin membrane
- Edge protection layers to improve mechanical yield

Main design options

- Substrate bias from the back-side (also suitable for dual-readout pixel/strip detectors)
- No active edge, but allows for “slim-edge” detectors
- Technology of choice at FBK for ATLAS IBL prototypes

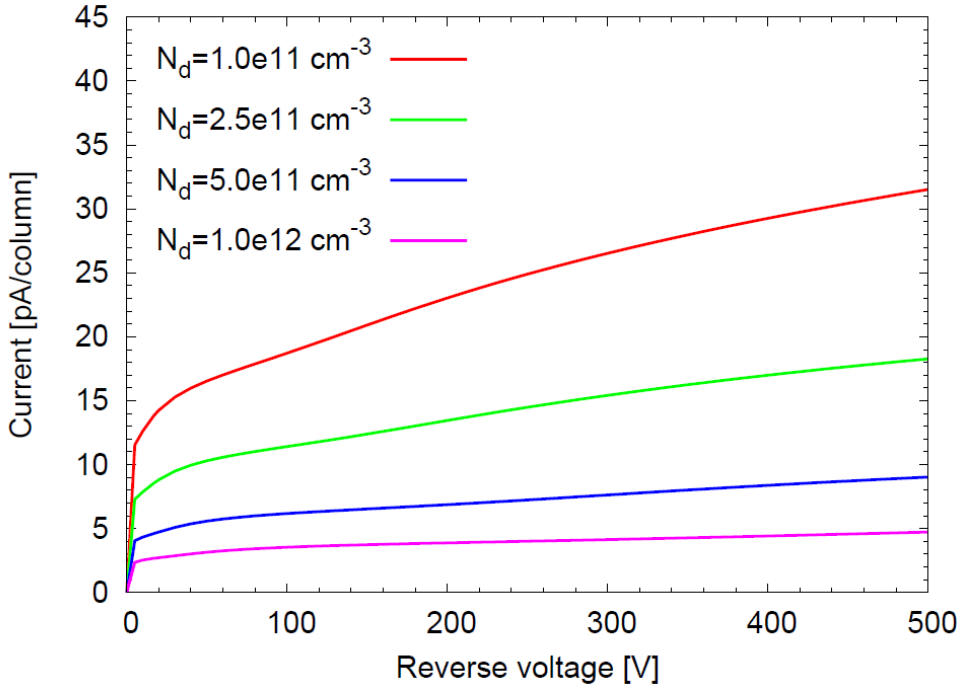
Slim edge option

Simulation domain



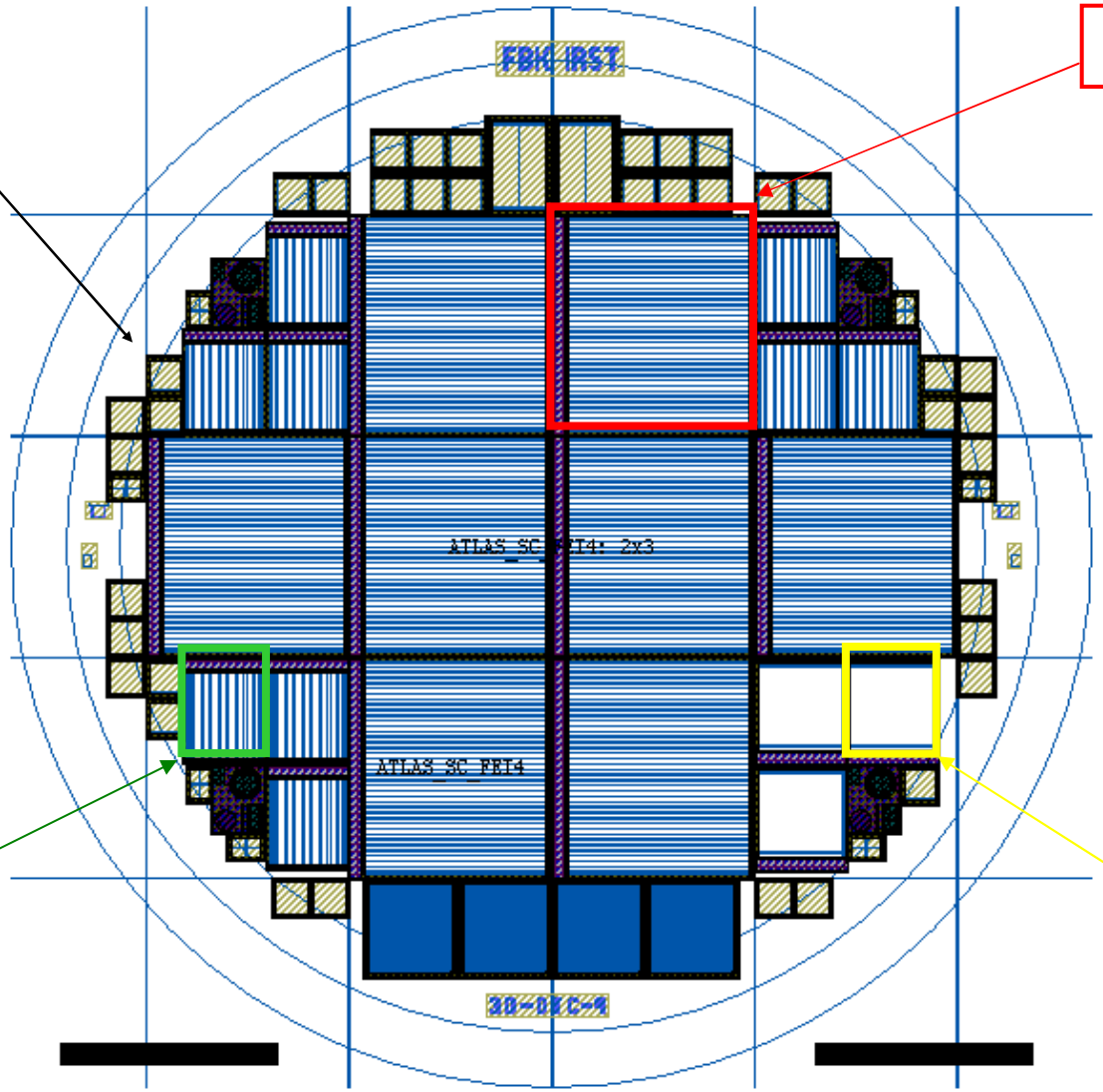
- Multiple Ohmic fence termination
- Dead area ~ 200 µm
- No leakage current drawn from highly damaged cut region

Simulated I-V curves



ATLAS 3D sensors for IBL: common floor-plan

Test structures (planar and 3D) at the periphery



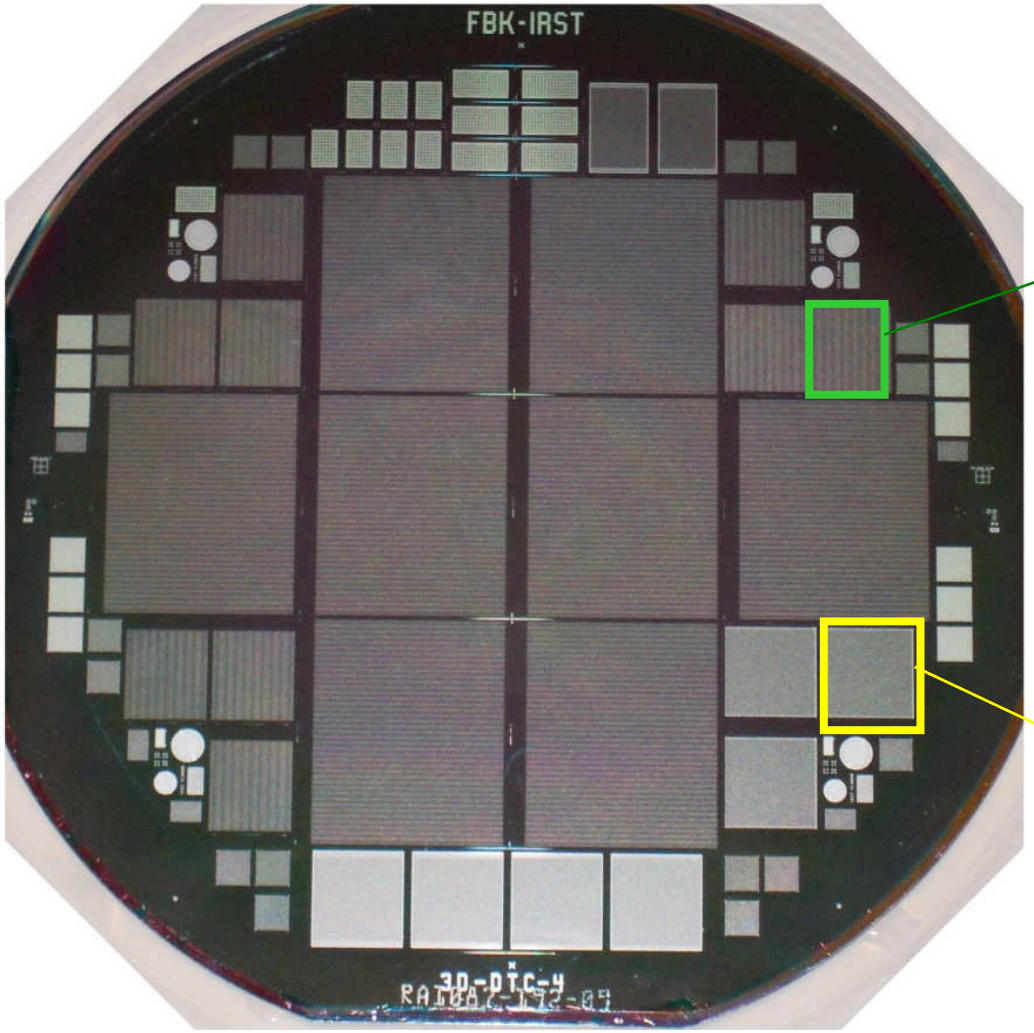
FE-I4 (8x)

FE-I3 (9x)

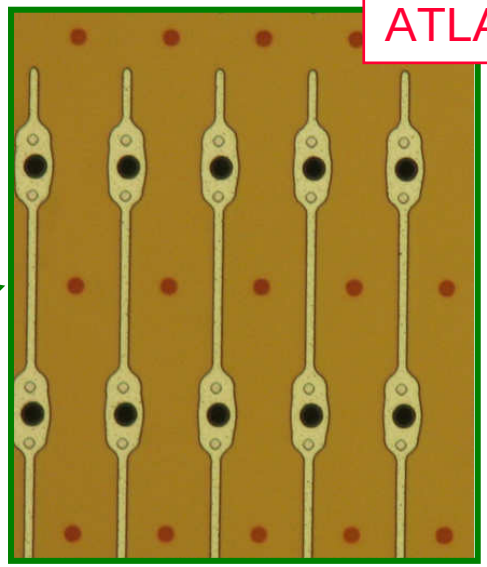
CMS (3x)

3D-DTC- 4: some pictures

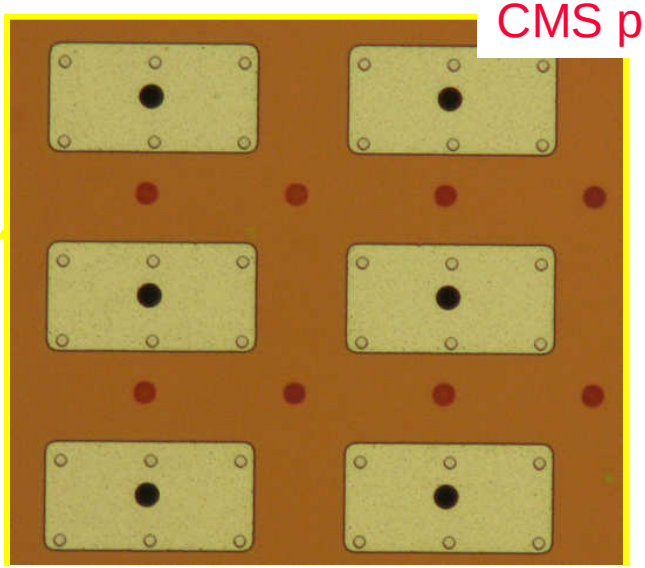
First processed wafer



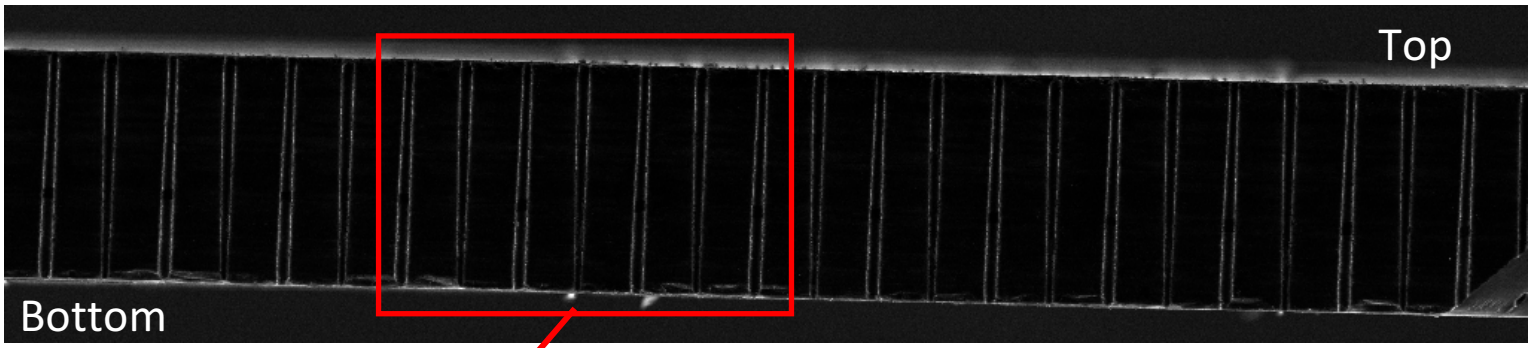
ATLAS pixels



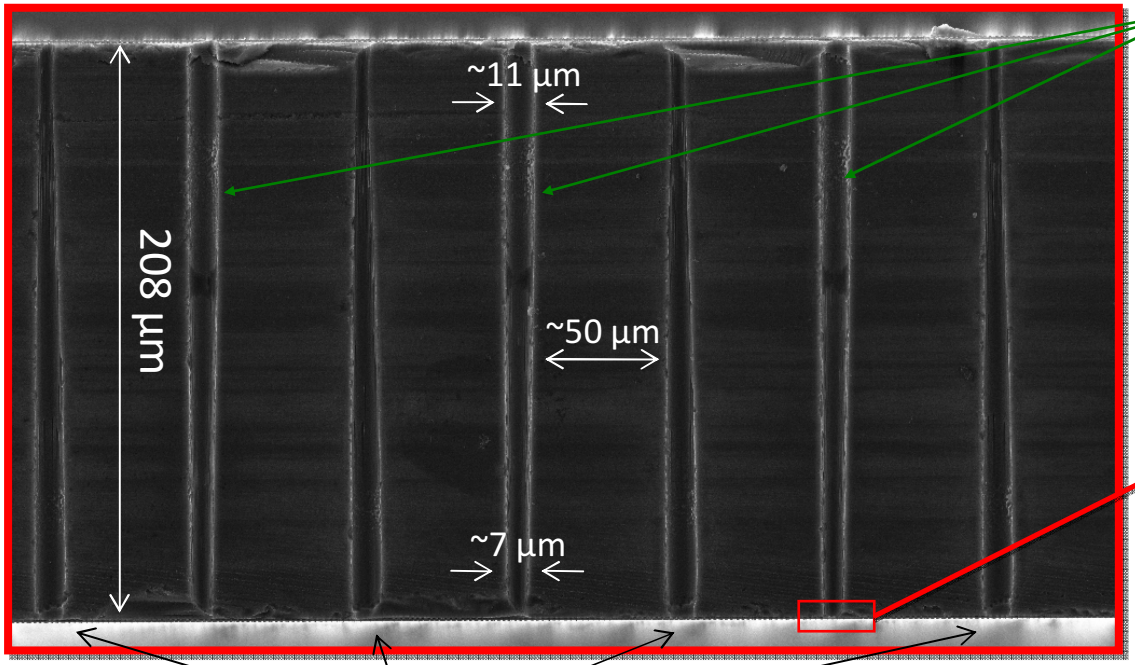
CMS pixels

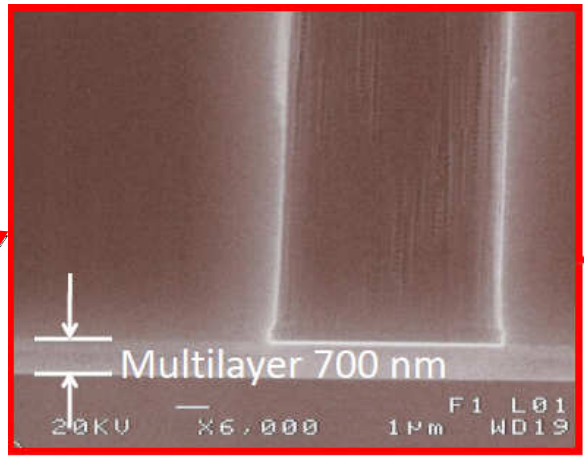


Passing through columns



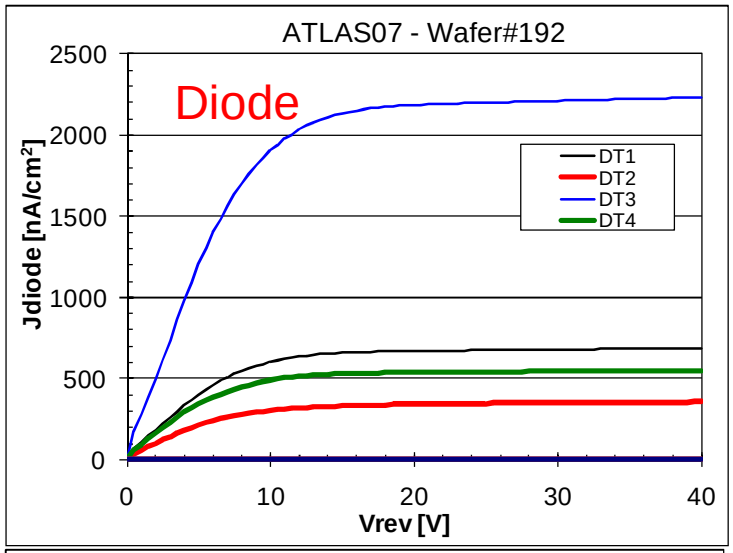
n+ columns (front side DRIE)

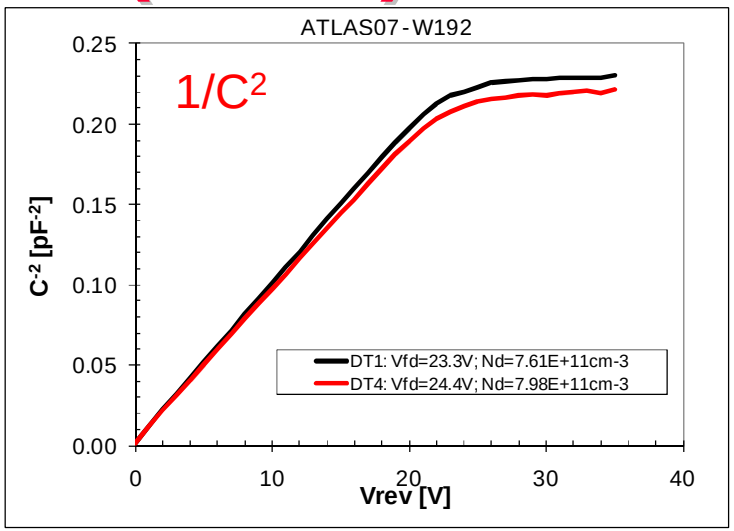


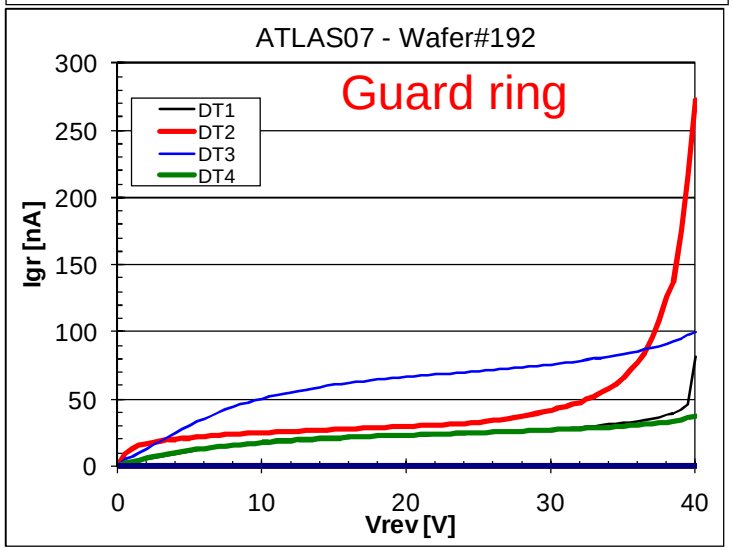


p+ columns (back side DRIE)

3D-DTC-4: preliminary results (1)
Planar test diodes (4mm²)





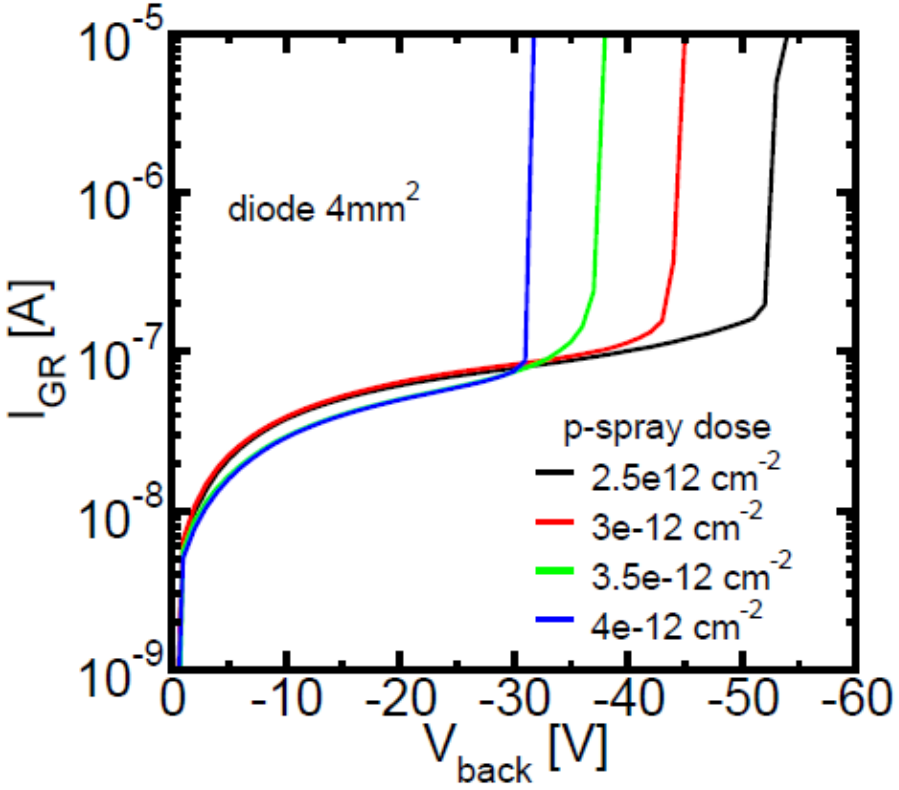


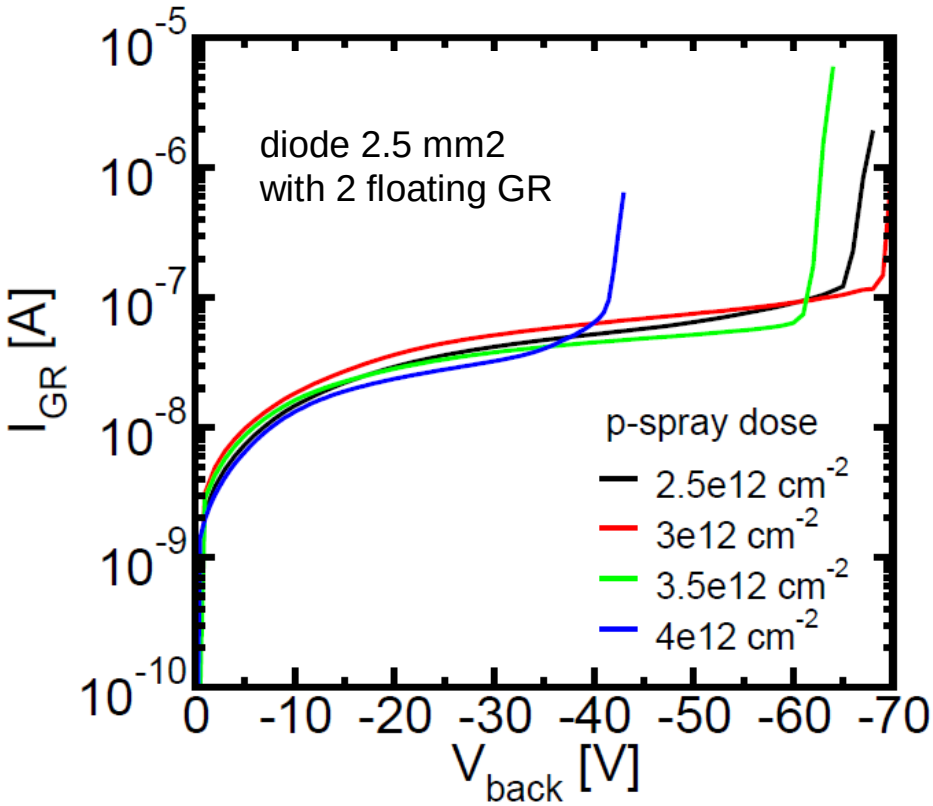
- J_{lk} ~ 500nA/cm² (higher than usual)
- V_{BD}~ 40-50V (p-spray)
- Vdepl ~20 V → ρ ~ 16 kΩ·cm
- Surface parameters ok:

  s_0=10-30cm/s, N_{ox}=2-6x10^{11} cm^{-2}

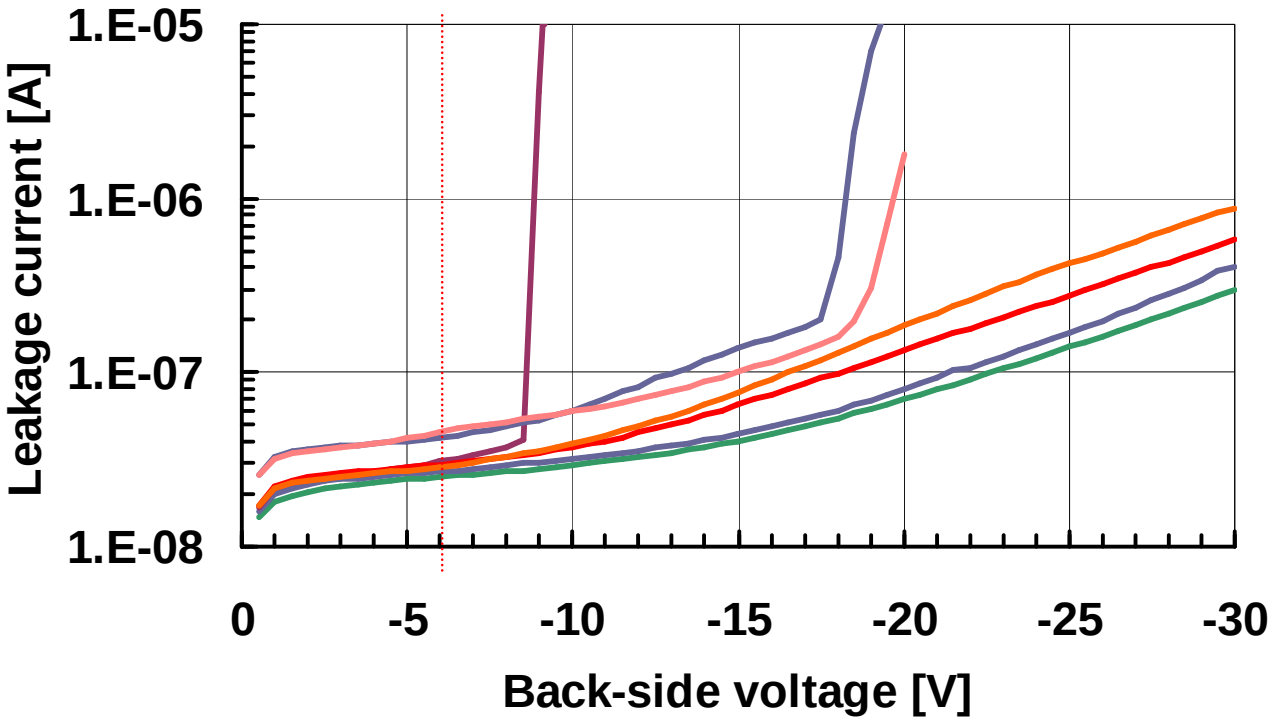
P-spray optimization studies

- Test batches of planar structures processed in parallel to 3D batches and using the same thermal budget
- Optimized p-spray doping profile and layout being investigated

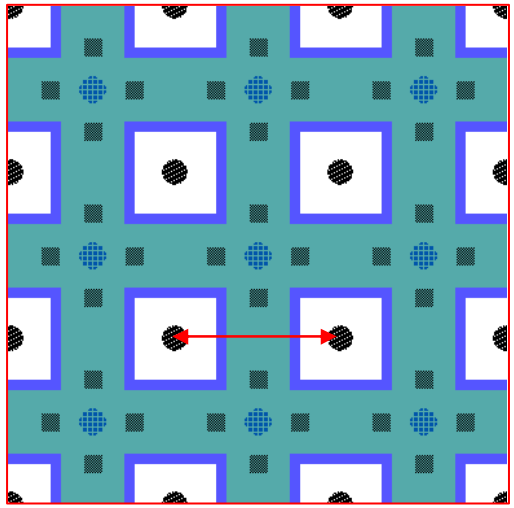




3D-DTC-4: preliminary results (2)
3D test diodes (~10mm²), I-V curves



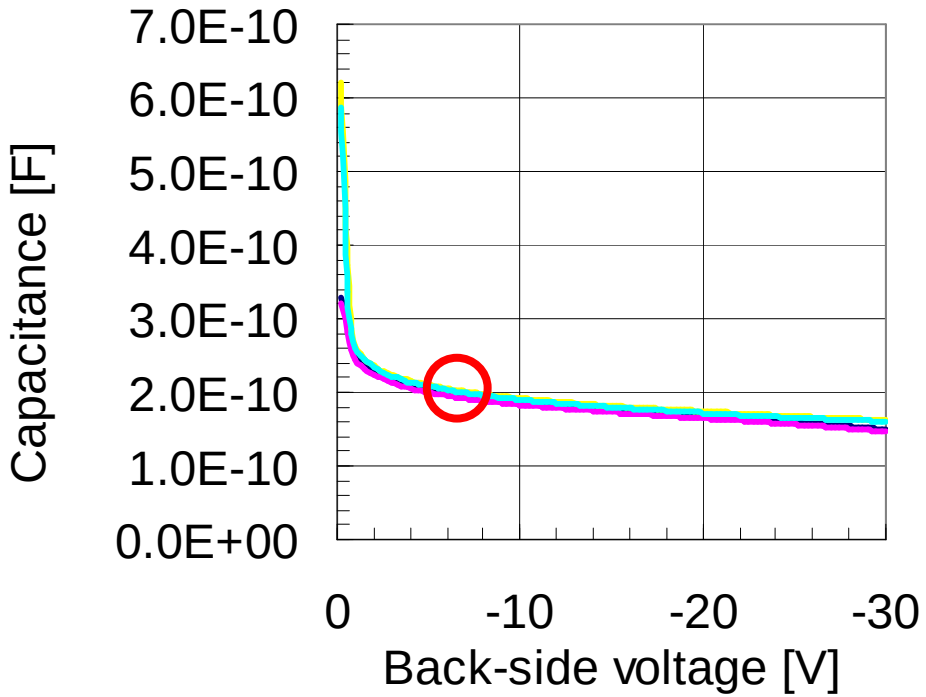
Layout detail

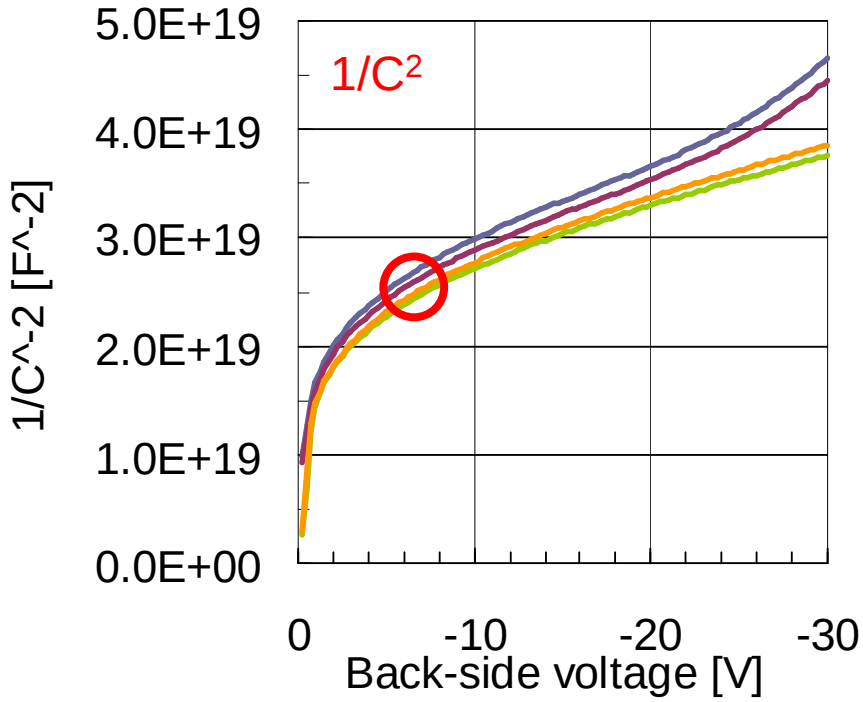


Array of 40x40 columns, pitch 80 μm

- J_{lk}~330 nA/cm² (~20 pA/col.) at V_{depl} (comparable to planar diodes)
- Leakage not degraded from DRIE but likely from mechanical stress
- Intrinsic breakdown (p-spray) + early breakdown due to defects

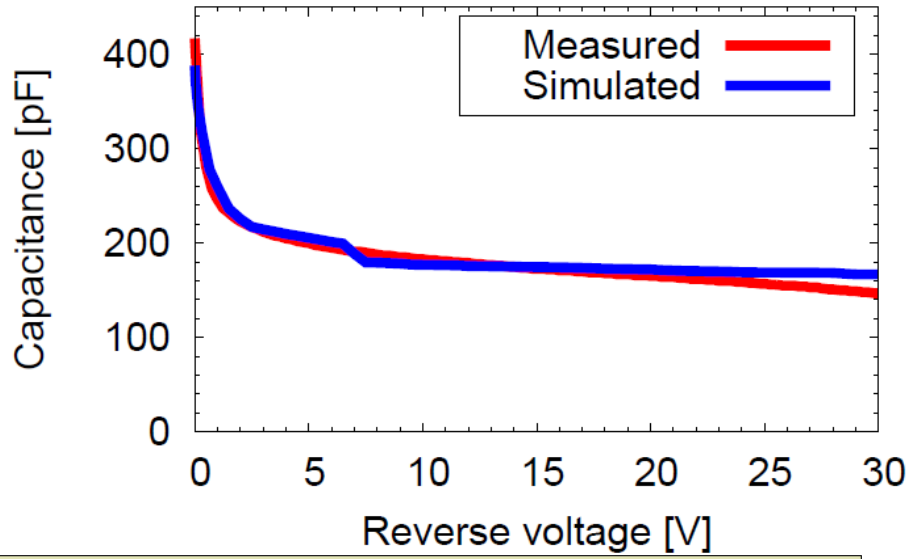
3D-DTC-4: preliminary results (3)
3D test diodes (~10mm²), C-V curves

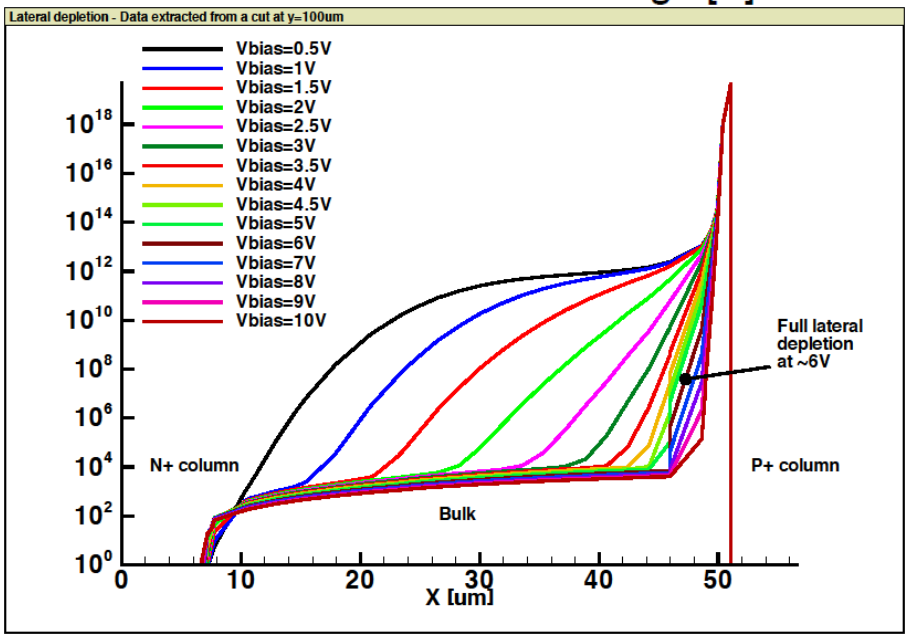


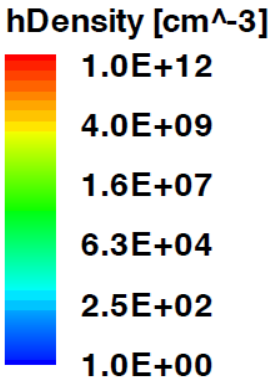


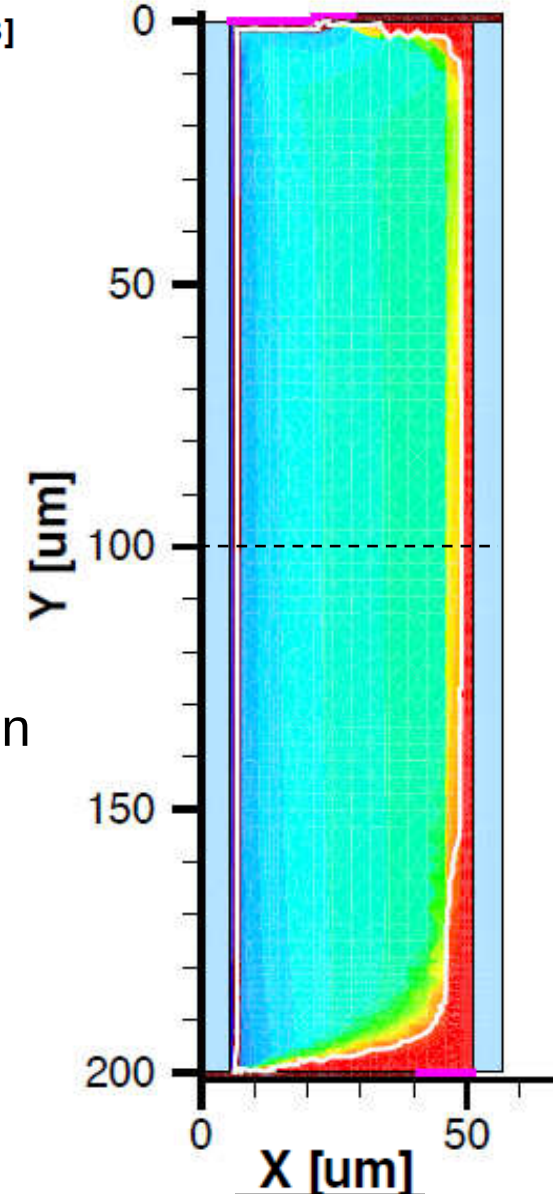
- Capacitance ~200pF (125 fF/col.) at V_{depl}
- Non negligible contribution from surface (p-spray)
- Depletion at a few V (see next slide)

3D diode: C-V simulation









- Lateral depletion at about 6V
- Corner at the bottom difficult to fully deplete

Conclusions

- The development of 3D detector technologies at FBK-irst is proceeding with encouraging results
- 3D-DDTC detectors have been extensively characterized in laboratory and beam tests, showing good performance up to an irradiation fluence of $1x10^{15}$ n_{eq}/cm^2
- To further improve performance and process reproducibility, 3D-DDTC^{+} detectors (with “passing through” columns) have been developed and preliminary results have been reported
- More wafers to come in a few weeks with an optimized fabrication process which improve electrical parameters