### **HERD-SCD** preliminary electronics fanout plan

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### 1.working principle

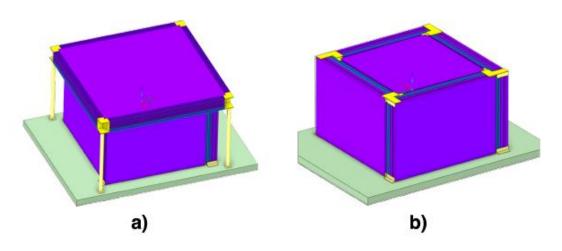


Figure 1 Layout of the SCD plans

There are two options for the design of the SCD and PSD systems. Option a) features a larger SCD-Top surface of  $\sim 1.8 \times 1.8 \text{m}^2$  with respect to the option b) one of  $\sim 1.4 \times 1.4 \text{m}^2$ . Correspondingly, option a) Side-SCD units are smaller with a surface of  $\sim 1.6 \times 1.1 \text{m}_2$  with respect to option b) ones of  $\sim 1.7 \times 1.2 \text{m}_2$ . Option b) would lead to a mechanically more manageable

SCD-Top with respect to option a).

Recently, HERD mechanical and thermal group has designed the preliminary version of the overall structure of HERD, as shown below.

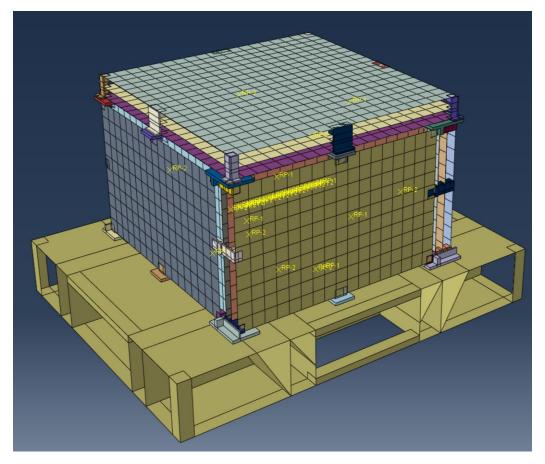


Figure 2 The HERD Mechanical structure drawing

The layout of SCD is similar to that of plan a), with a large top SCD and four smaller side SCDs.

The SCD electronics DAQ module(SCD-DAQ) is placed in the four corners of the bottom.

### 2.SCD electronics module layout

The SCD is constituted by 5 thin detector units, one squared-shaped unit placed on

the top of the instrument (SCD-Top), and 4 identical rectangular-shaped units (SCD-Side) placed on the other 4 sides. The 5 units compose a box-shaped structure with the base plane of the HERD experiment. Similarly the PSD detector is divided in 5 units with similar surface dimensions and mechanically connected to the SCD.

In the current design, there are 896 ladders in total, so it is almost impossible for every ladder to be directly connected to the SCD\_DAQ. The front-end interfaces such as signal, control and power supply must be summarized before they can be connected to DAQ, which is the work of FFB(Front fanout board)

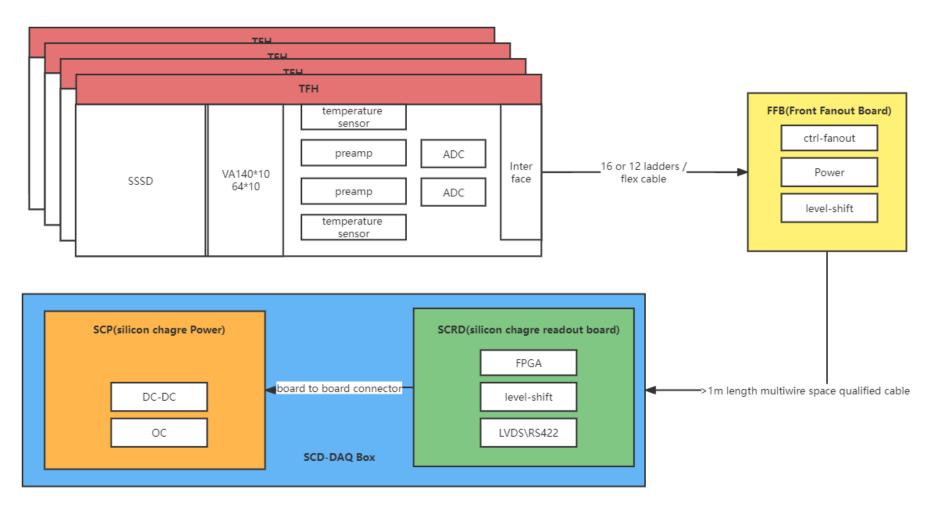


Figure 3 SCD electronics module layout

# 3. Layout of the SSSDs and FFBs

### 3.1 Layout of the side SSSDs and FFBs

#### SCD\_side

4 X layers (Horizontal) 11\*2 ladders per layer、8 SSSDs per ladder

4 Y layers (Vertical) 16 ladders per layer、11 SSSDs per ladder

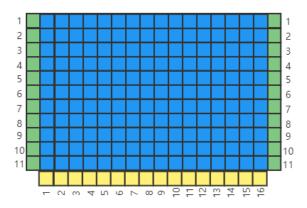


Figure 4 side SSSDs layout

For the side SCD detectors, there are 608 Ladders in total.

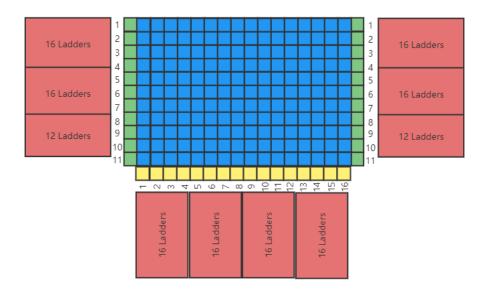


Figure 5 side FFB layout

Using the layout scheme of FFB in the above figure, 10 FFB boards are needed in one side. So for the side SSSDs, we need 40 FFBs in total.

Those FFBs are separated into two types, 12 laddders type and 16 ladders type.

## 3.2 Layout of the top SSSDs and FFBs

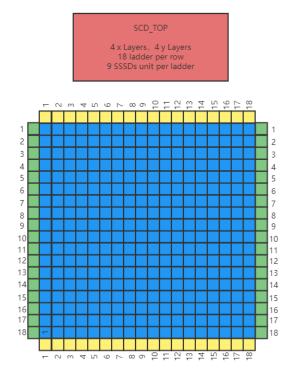


Figure 6 top SSSDs layout

For the top side SCD, there are 288 Ladders in total.

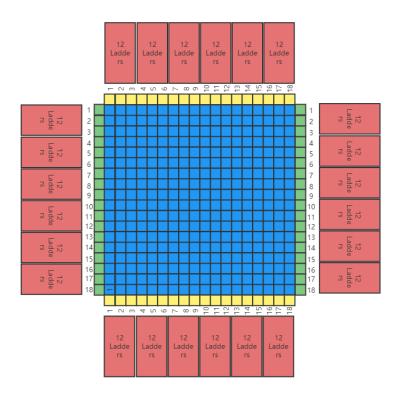


Figure 7 top FFB layout

Using the layout scheme of FFB in the above figure, 6 FFB boards are needed in one side. So for the side SSSDs, we need 24 FFBs in total.

Those FFBs are all 12 ladders type.

#### 3.3 Summary of the FFBs layout

For the side SCDs, 40 FFBs are needed in total.

For the top SCDs, 24 FFBs are needed in total.

Each DAQ box needs to be connected with 1 / 4 SCDS, so each DAQ box corresponds to 16 ladders.

#### 4. Cabling

Assuming that the chip used in the front end is still VA140 and the ADC chip is also placed in the front end, each ladder needs to use the signals shown in table 1

Most of these signals in the TFH are mergeable. Therefore, for the FFB used to match 12 ladders, at least 42 wires are required. For the FFB used to match 16 ladders, at least 50 wires are required. We can place the power conversion module on the FFB, which can reduce the loss of power on long-distance cables and also reduce the number of wires from FFB to DAQ.

Table 1 pins of the connectors of one TFH

	HERD	Signal type	mergeable
1	SHIFT_IN_A	Digital	√
2	ADC_SCLK_1	Digital	√
3	ADC_SDATA_1	Digital	×
4	CLKA	Digital	√
5	CLKB	Digital	√
6	SHIFT_IN_B	Digital	√
7	TEMP_DATA	Digital	√(MAX 128)

8	HOLD_B	Digital	√
9	TEST_ON	Digital	√
10	ADC_CS	Digital	√
11	RESET	Digital	✓
12	ADC_SCLK_2	Digital	√
13	ADC_SDATA_2	Digital	×
14	VCC	+3.3V/(1mA*2+1mA)*2	√
15	VDD	+1.5V/3mA*10	√
16	VSS	-2V/9mA*10	√
17	CALin	Analog	√
18	HVin	80V /<1uA	√
19	NC		√
20	GND	Power	√