Xilinx RFSoCs

Roadmap to Meet Current and Future Market Needs

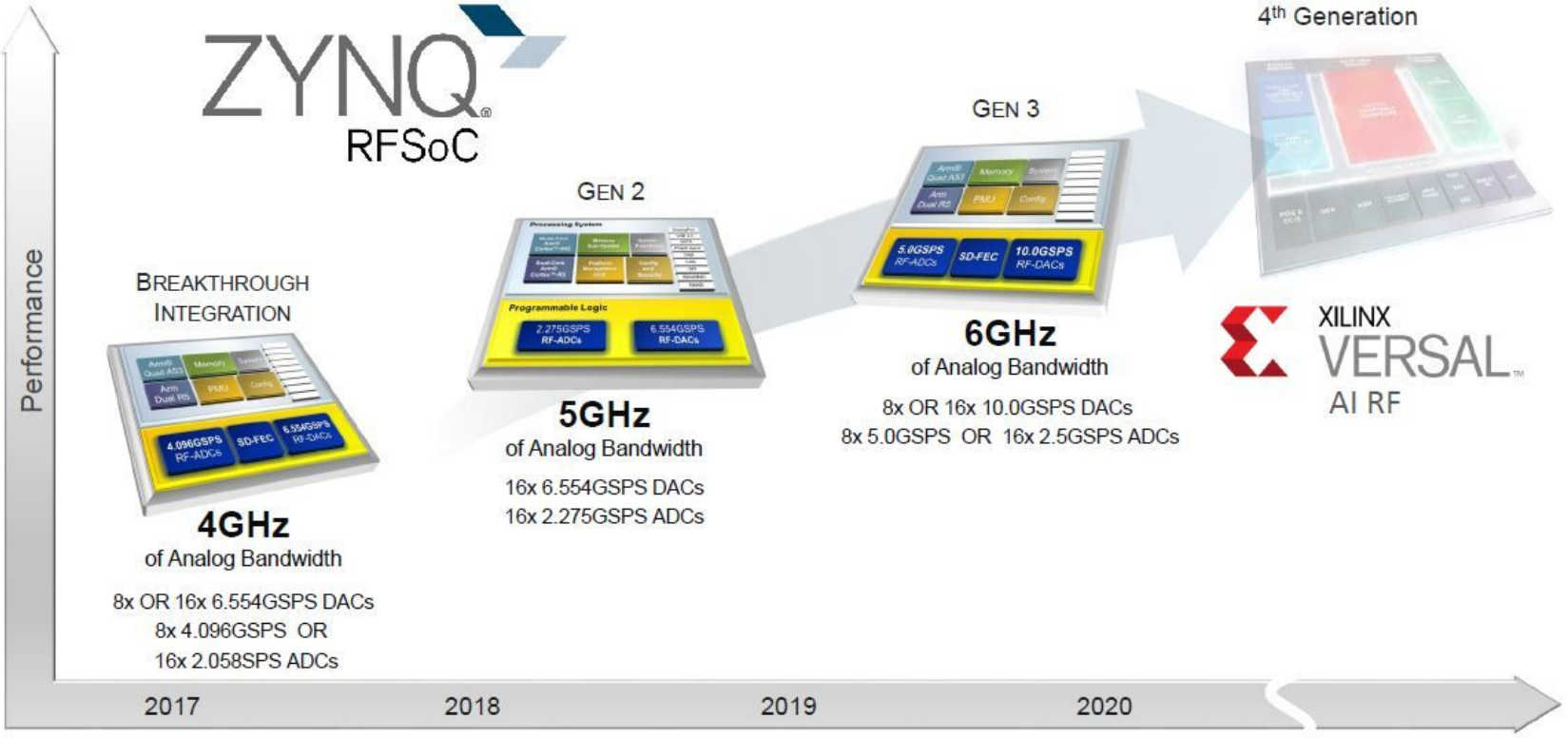
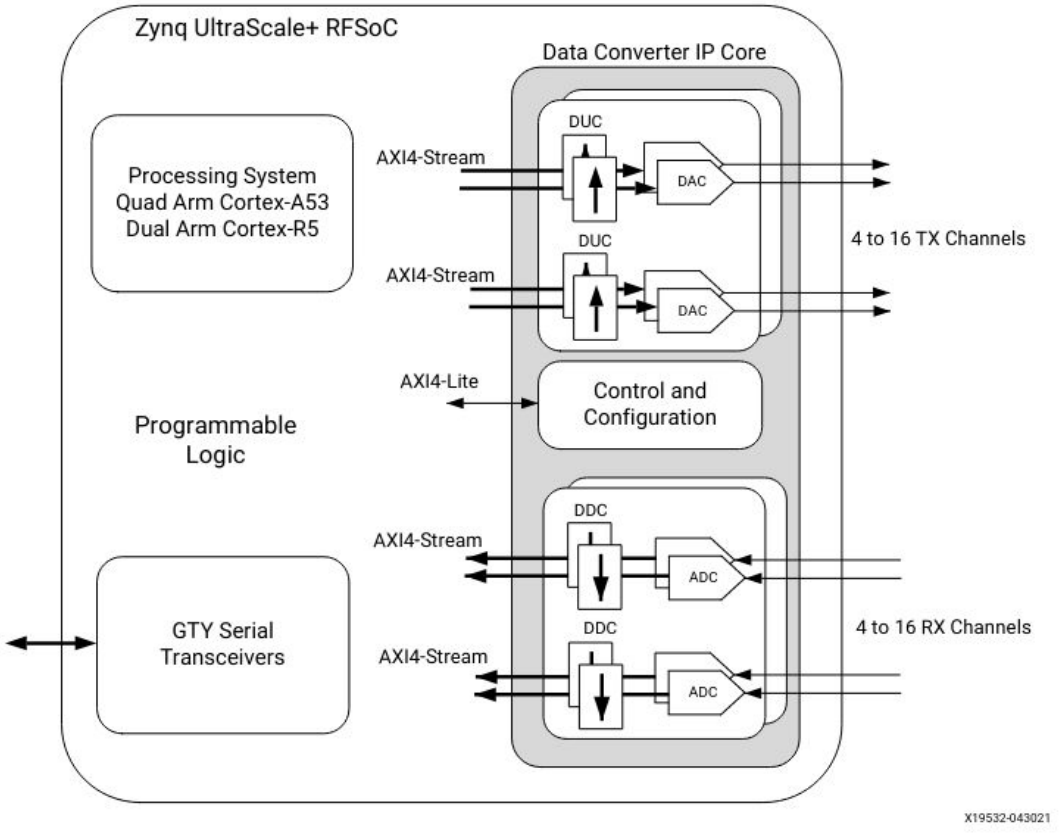


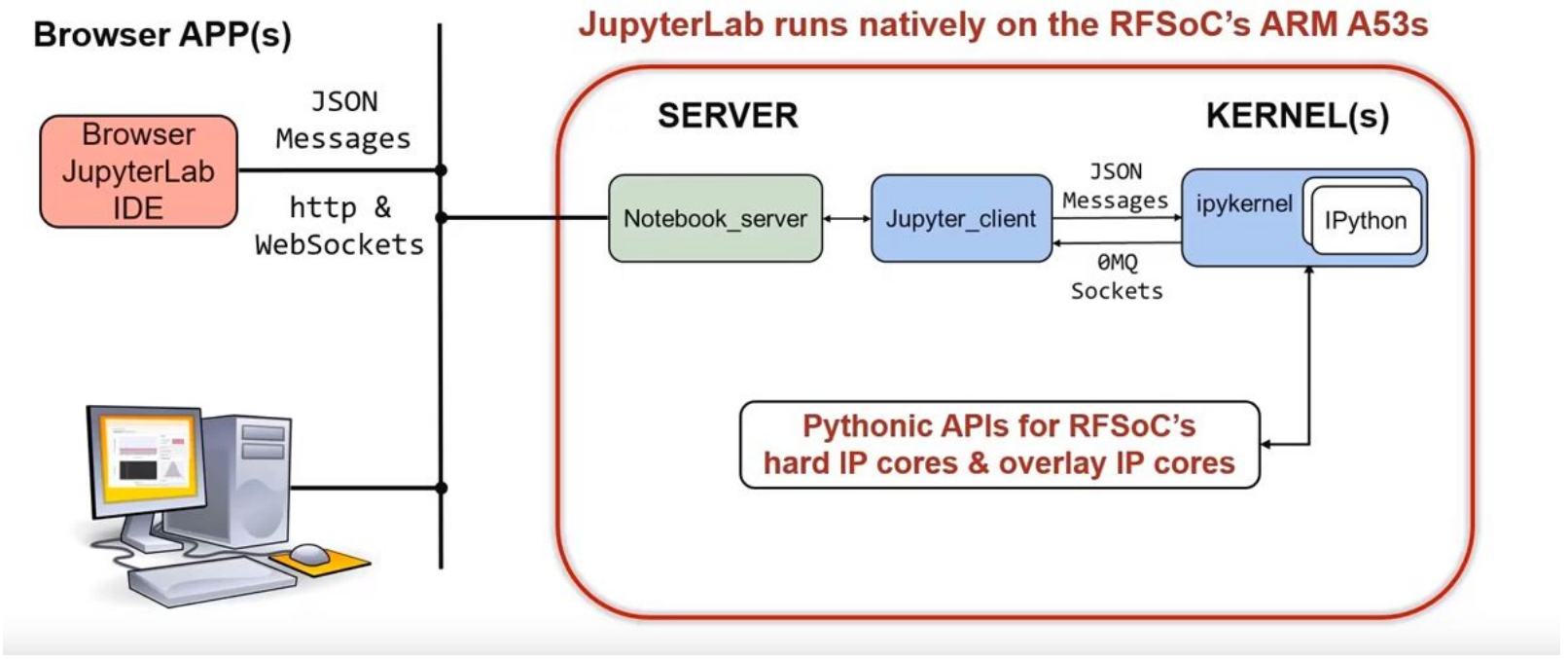
Figure 1: **Zynq UltraScale+ RFSoC RF Data Converter IP Core in Zynq UltraScale+ RFSoC (Gen 1/Gen 2/Gen 3)**



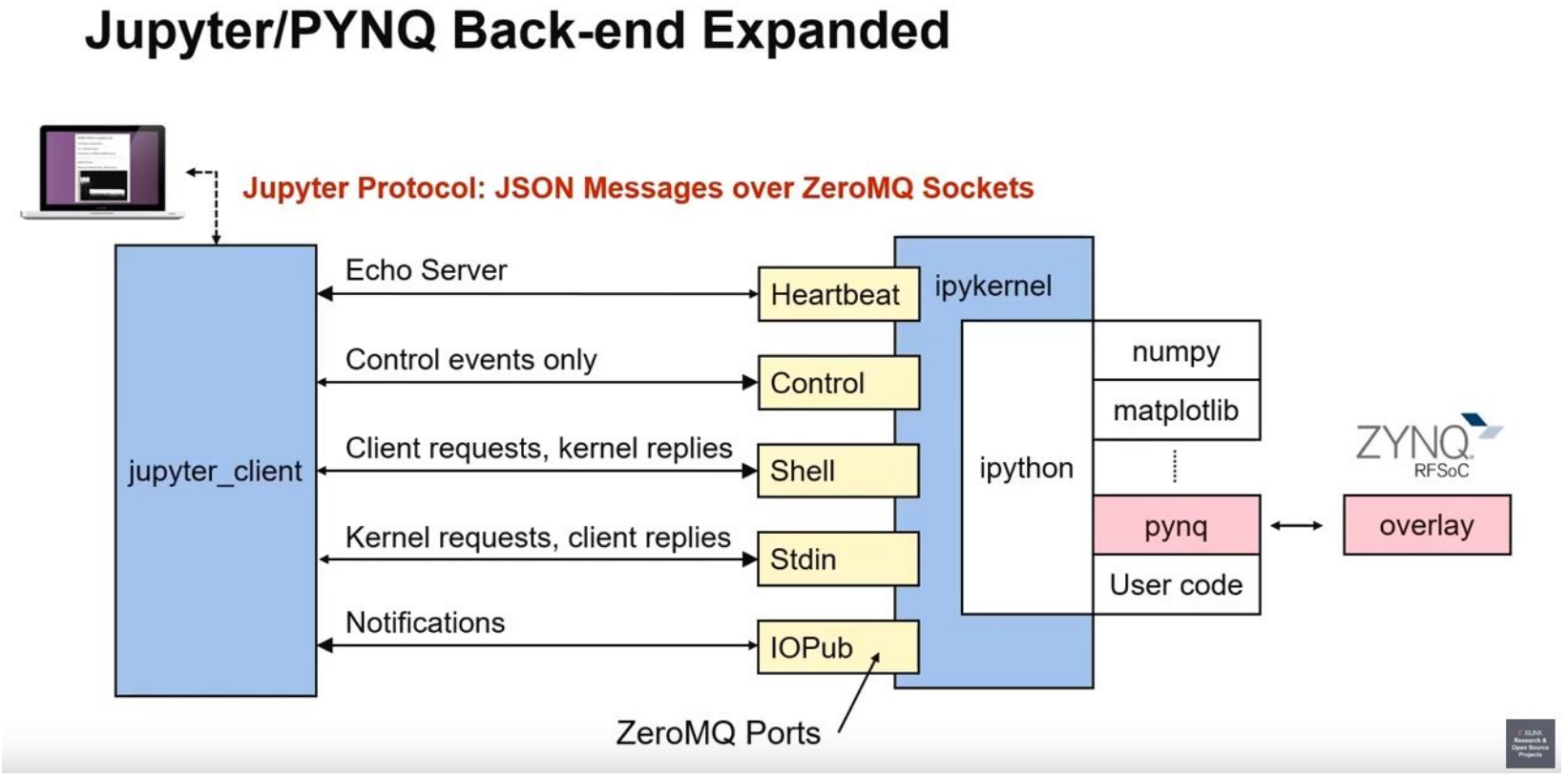
RFSoC Diagram

RFSoC PYNQ

RFSoC PYNQ = Embedded Jupyter Lab
+ Pythonic Integration of Hard & Overlay IPs

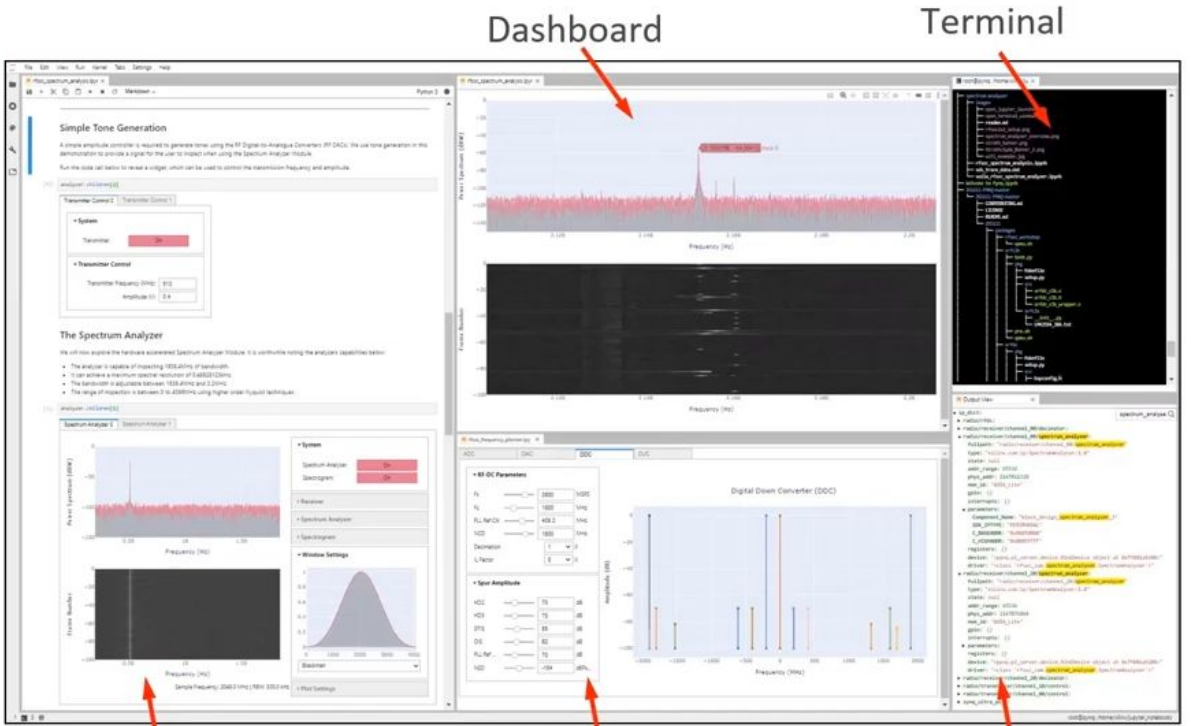


RFSoC PYNQ


Jupyter/PYNQ Back-end Expanded
Jupyter Protocol: JSON Messages over ZeroMQ Sockets
jupyter_client
Echo Server
Control events only
Client requests, kernel replies
Kernel requests, client replies
Notifications
Heartbeat
Control
Shell
Stdin
IOPub
ipykernel
ipython
numpy
matplotlib
pynq
User code
ZYNQ
RFSoC
overlay
ZeroMQ Ports

RFSoC PYNQ

Jupyter Notebooks to JupyterLab IDE



Next-generation IDE

Browser-based GUI

Multiple re-sizable frames in one browser window

Completely extensible

Jupyter Notebooks are one of many plug-ins available in JupyterLab

ZCU111

- Gen 1
- 8 x 12-bit ADCs 4.096 GSPS
- 8 x 14-bit DACs 6.554 GSPS
- PYNQ Support

ZCU208

- Gen 3
- 8 x 14-bit ADCs 5 GSPS
- 8 x 14-bit DACs 10 GSPS
- PYNQ NOT Supported (yet)