

Xilinx RFSoc

Roadmap to Meet Current and Future Market Needs

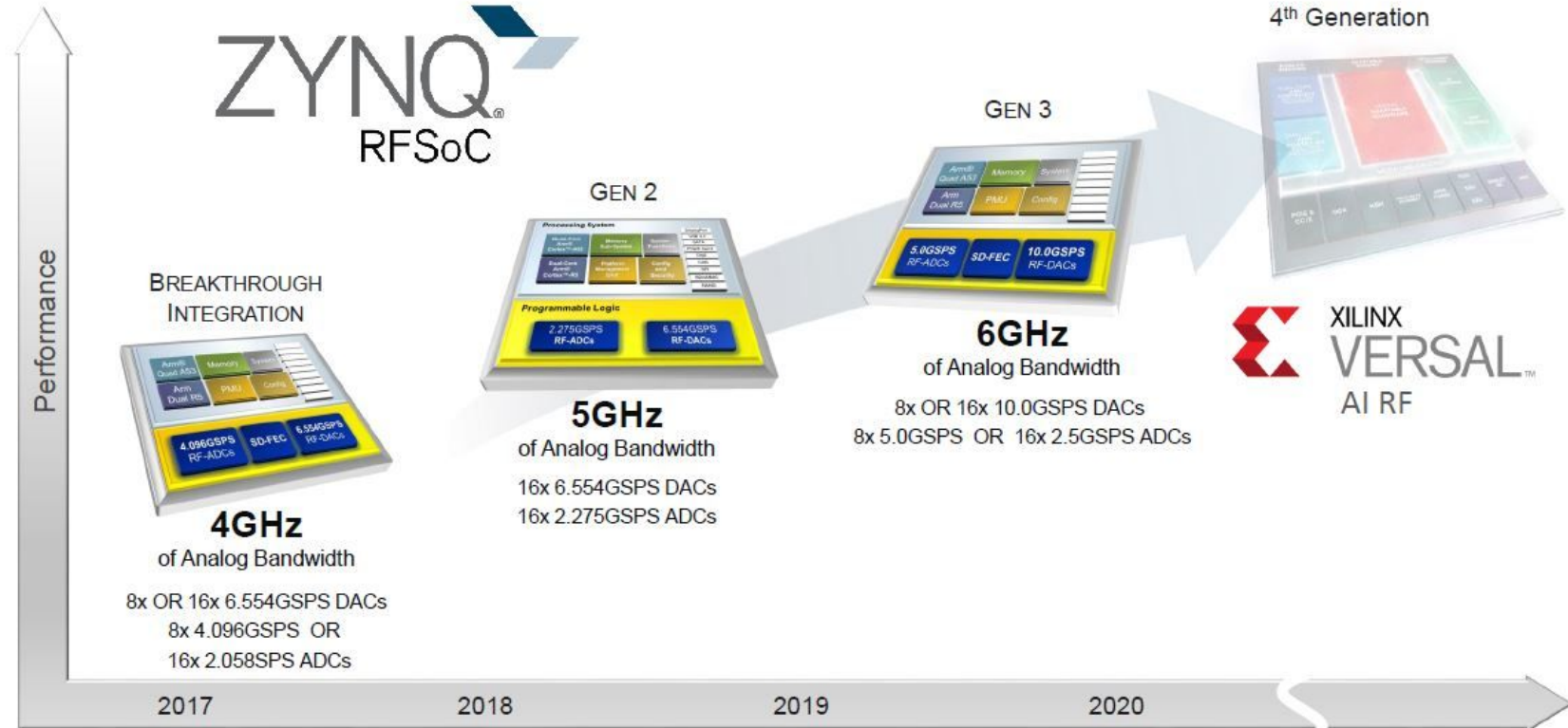
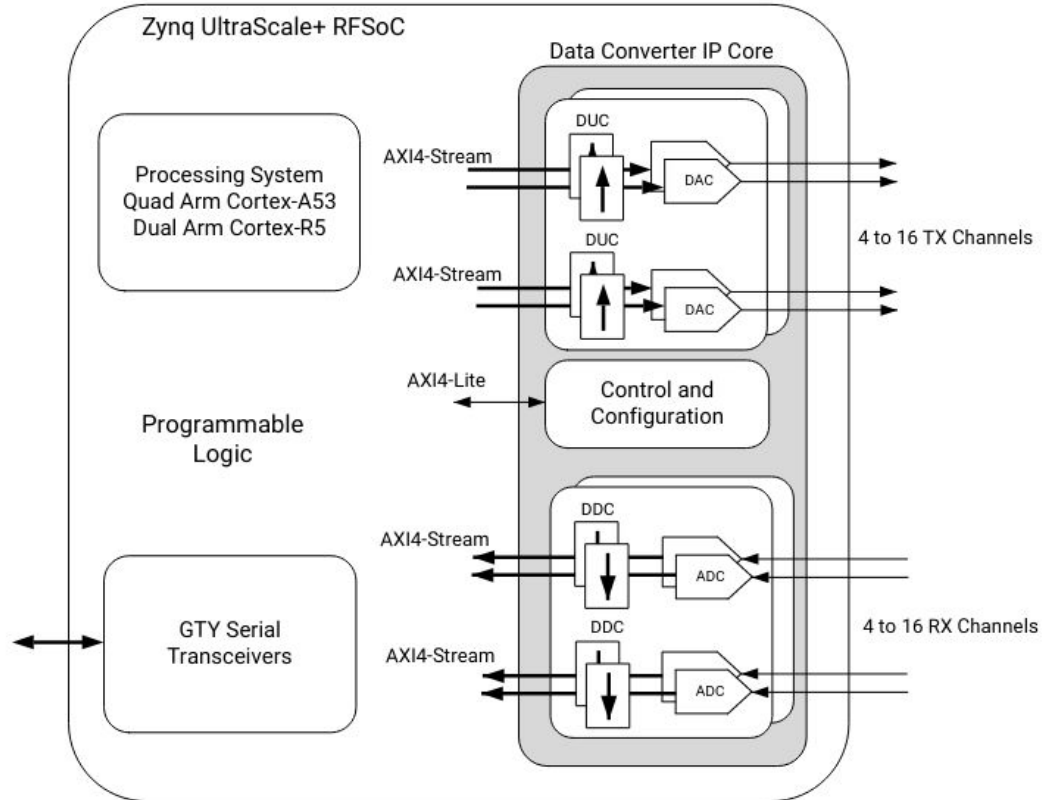


Figure 1: Zynq UltraScale+ RFSoc RF Data Converter IP Core in Zynq UltraScale+ RFSoc (Gen 1/Gen 2/Gen 3)

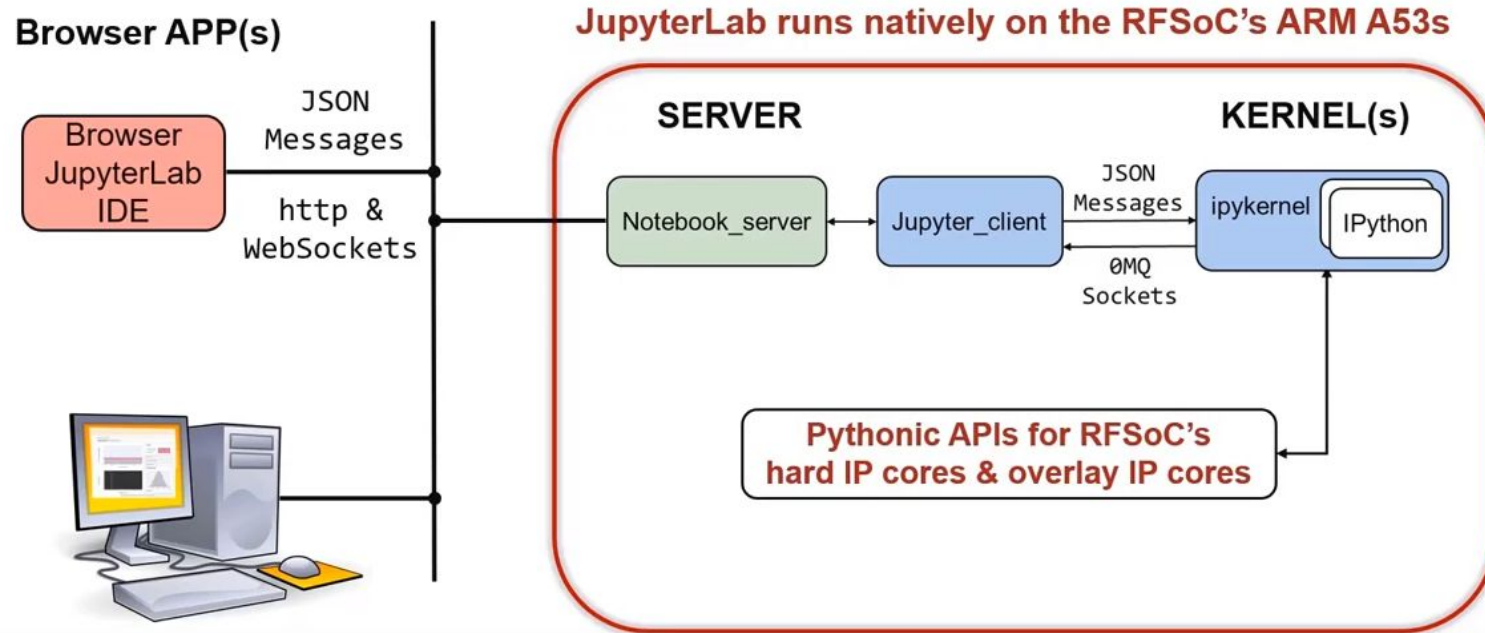


X19532-043021

RFSoc Diagram

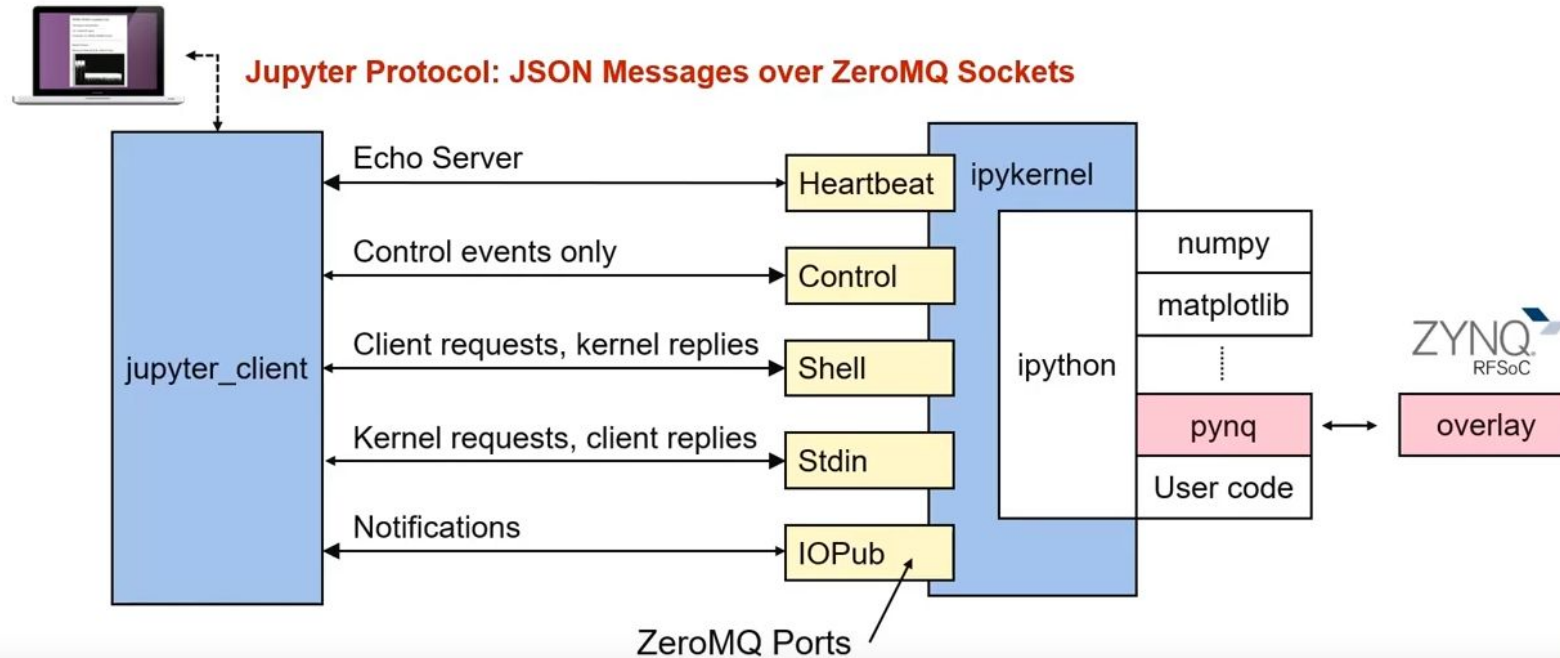
RFSoc PYNQ

**RFSoc PYNQ = Embedded Jupyter Lab
+ Pythonic Integration of Hard & Overlay IPs**



RFSoc PYNQ

Jupyter/PYNQ Back-end Expanded



RFSoc PYNQ

Jupyter Notebooks to JupyterLab IDE



Next-generation IDE

Browser-based GUI

Multiple re-sizable frames
in one browser window

Completely extensible

Jupyter Notebooks are
one of many plug-ins
available in JupyterLab

The screenshot displays the JupyterLab interface with three main panels:

- Jupyter notebook:** A notebook titled "Simple Tone Generation" with a "Spectrum Analyzer" widget. It shows a plot of "Power Spectral Density (dBm)" vs "Frequency (Hz)" with a prominent peak at 2.0 MHz.
- Frequency Planner Dashboard:** A dashboard with a "Digital Down Converter (DDC)" widget. It includes a "System" section with a "Spectrum Analyzer" plot and a "Window Settings" section with a "Bandwidth" plot. Below these are "RF DC Parameters" and "Sine Amplitude" sections with various numerical inputs.
- IP Introspection:** A terminal window showing a tree view of the system's IP addresses and their associated components, such as "axi4lite0", "axi4lite1", and "axi4lite2".

Jupyter notebook

Frequency Planner Dashboard

IP Introspection

ZCU111

- Gen 1
- 8 x 12-bit ADCs 4.096 GSPS
- 8 x 14-bit DACs 6.554 GSPS
- PYNQ Support

ZCU208

- Gen 3
- 8 x 14-bit ADCs 5 GSPS
- 8 x 14-bit DACs 10 GSPS
- PYNQ NOT Supported (yet)