





Qubit-0.0.1 - Activity Report - 06/04/2022

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Introduction



Extensible Architecture for Superconducting Quantum Computing - Thomas G. McConkey <u>https://uwspace.uwaterloo.ca/handle/10012/13464</u>

Design Goals

- •Test device comprised of four qubits capacitively coupled to a readout resonator.
- -Feedline with $Z_0 = 50 \ \Omega$
- Two readout resonators capacitively coupled to the feedline
- Two readout resonators inductively coupled to the feedline
- •Two qubits tunable via a dedicated control line

Design Snapshot



Note

- •Four qubits on the same chip
- •No tuning control lines for qubit Q3 and Q4 at the moment
- Qiskit Metal hack to simulate the substrate (the wirebond pad at the center is a sideeffect)

FBK Substrate



Feedline Impedance Matching



Design Analysis 1/3



The analysis are based on the EPR (Energy Participation Ratio)

Energy-participation quantization of Josephson circuits - Zlatko Minev https://arxiv.org/abs/2010.00620

Design Analysis 2/3

Qubit	Frequency (GHz)	a (MHz)	χ (MHz)	Readout Resonato	Frequency (GHz)
Q1	4.70	216.78	0.95	R1	5.01
Q2	5.34	288.29	0.66	R2	6.16
Q3	5.92	165.52	2.54	R3	6.45
Q4	5.69	150.05	0.65	R4	6.84

Note

• At the moment we don't have T1 since its analysis has a severe bug on Qiskit Metal

Design Analysis 3/3



Manufacturing Constraints

- Is it important to consider the SiO2 layer in our simulations?
- Are there any constraints on the JJ inductances?
- How much variance does have the manufactured JJ inductances?
- Can we design qubits with different JJ inductances on the same chip?
- Are there any constraints on the aluminum metallisation (e.g. qubits, resonators, feedline, gaps)?
- Does FBK already have a document with the specs to design 50 ohm feedlines?
- Which are the desired values of χ , α , frequencies, and qubit detunings?
- Which is the qubit minimum shunt capacitance that allows to neglect the JJ parasitic capacitance?

Thanks for your attention!