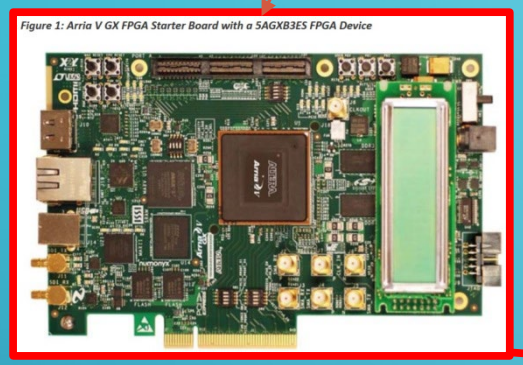
Quest for a replacement of the Intel/ALTERA ArriaVGX dev. kit

Angelo Cotta Ramusino

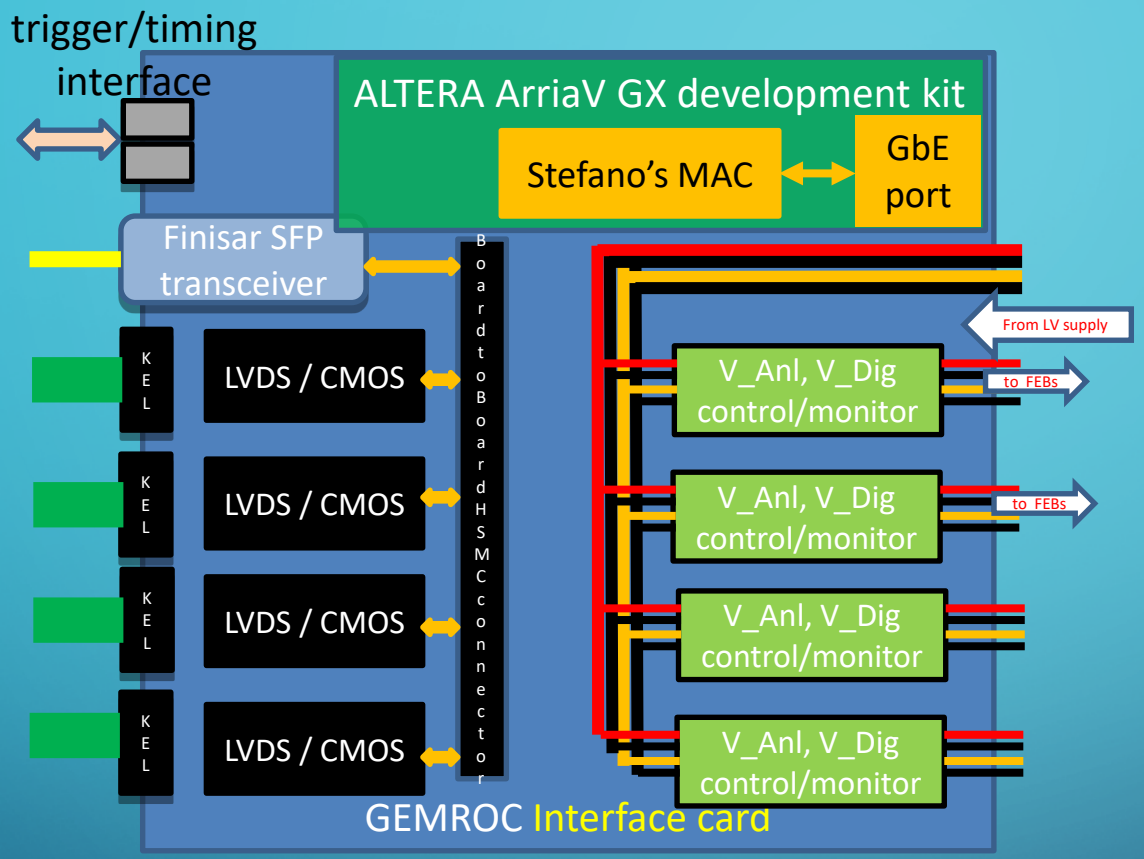
GEMROC: Off-detector readout card for BES-III CGEM-IT detector

GEMROC = GEMROC_InterFace Card (A.C.R.) + ArriaV GX development kit (DK-START-5AGXB3N) (development kit production discontinued in 2020)



GEMROC module dimensions: 334mm x 176mm x 44mm

GEMROC_InterFace Card block diagram



The GEMROC module LV fanout section has 2 power input:

- VCC_Anl
- VCC_Dig

driven by the DETECTOR LV power supply mainframe, one channel of which supplies two GEMROC modules.

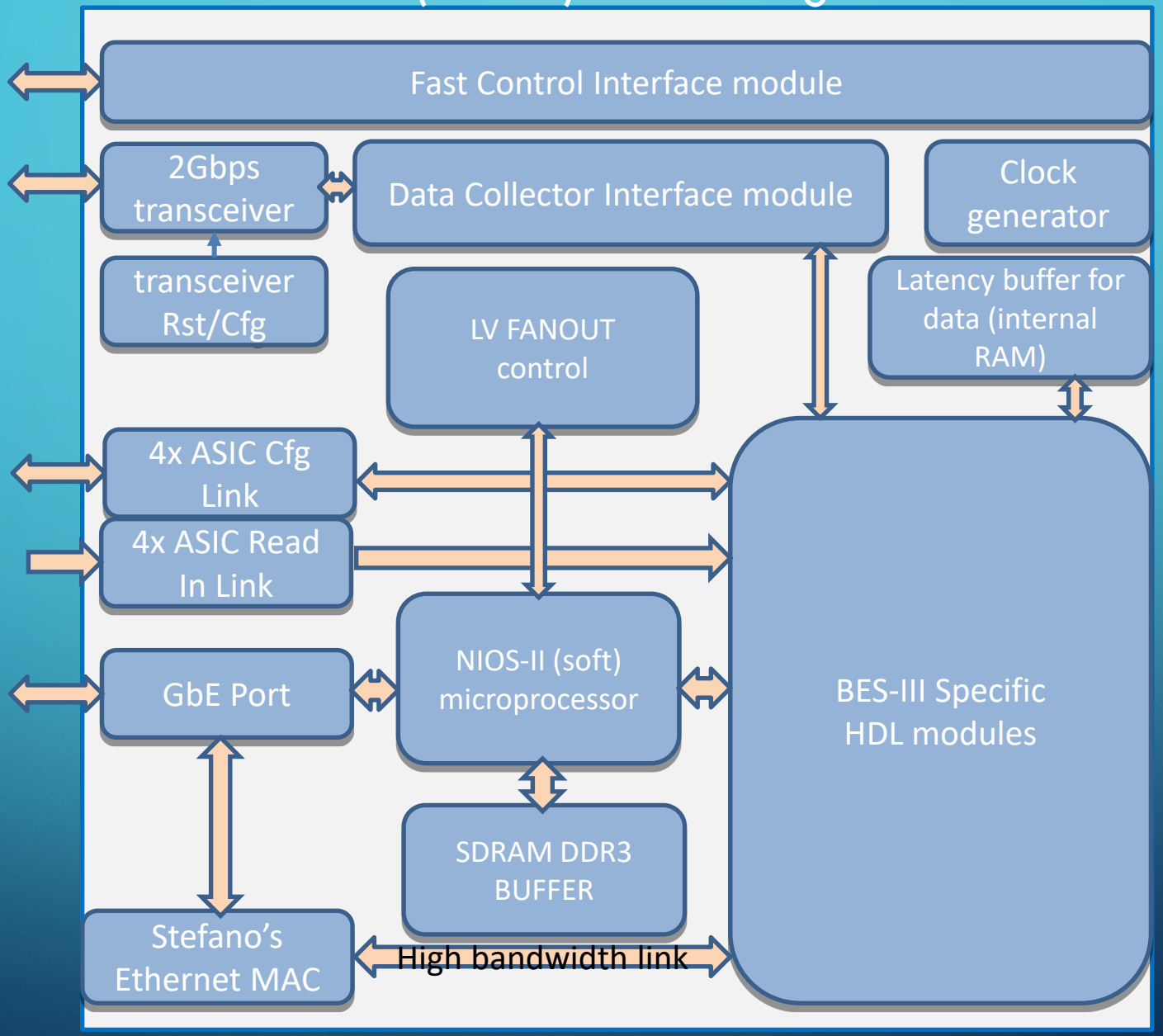
The GbE port of the FPGA module is used to receive commands to turn ON, turn OFF and read current for each of the 4 output power ports.

Power for the GEMROC itself comes from the independent "VCC_GEMROC" input

Through the MAC unit designed by **Stefano Chiozzi, INFN-FE**, the Ethernet port of the GEMROC module supports:

- static IP (example: 192.168.1.aaa, with aaa determined by Board ID)
- UDP communication for LV FANOUT control by SLOW control system
- UDP communication for TIGER configuration by DAQ/RUN control system (PROPOSAL)
- UDP communication for diagnostic TIGER data readout (as for DAC scan tasks)

GEMROC FPGA: firmware (A.C.R.) block diagram



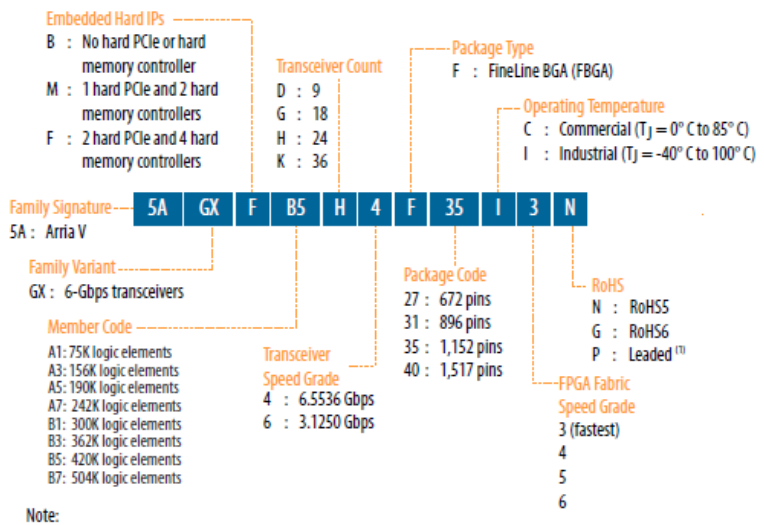
ARRIA V GX DEV. KIT: ALTERA PART NUMBER DK-START-5AGXB3N

FPGA device: 5AGXFB3H4F35C4N
Technology: TSMC's 28nm; Year launched 2011

Cost: EUR 791,93 (nov 2019)
PDN: Dec 2020 but ran out of distributor's stock months before

FIND A REPLACEMENT !!
(with, possibly, the same footprint)

Figure 1: Sample Ordering Code and Available Options for Arria V GX Devices



Note:
1. Contact Intel for availability.

Maximum Resources

Table 4: Maximum Resource Counts for Arria V GX Devices

Resource		Member Code							
		A1	A3	A5	A7	B1	B3	B5	B7
Logic Elements (LE) (K)		75	156	190	242	300	362	420	504
ALM		28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240
Register		113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960
Memory (Kb)	M10K	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140
	MLAB	463	961	1,173	1,448	1,852	2,098	2,532	2,906
Variable-precision DSP Block		240	396	600	800	920	1,045	1,092	1,156

Resource		Member Code							
		A1	A3	A5	A7	B1	B3	B5	B7
18 x 18 Multiplier		480	792	1,200	1,600	1,840	2,090	2,184	2,312
PLL		10	10	12	12	12	12	16	16
6 Gbps Transceiver		9	9	24	24	24	24	36	36
GPIO(3)		416	416	544	544	704	704	704	704
LVDS	Transmitter	67	67	120	120	160	160	160	160
	Receiver	80	80	136	136	176	176	176	176
PCIe Hard IP Block		1	1	2	2	2	2	2	2
Hard Memory Controller		2	2	4	4	4	4	4	4

Related Information
High-Speed Differential I/O Interfaces and DPA in Arria V Devices chapter, Arria V Device Handbook
Provides the number of LVDS channels in each device package.

Package Plan

Table 5: Package Plan for Arria V GX Devices

Member Code	F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)		F1517 (40 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
A1	336	9	416	9	—	—	—	—
A3	336	9	416	9	—	—	—	—
A5	336	9	384	18	544	24	—	—
A7	336	9	384	18	544	24	—	—
B1	—	—	384	18	544	24	704	24
B3	—	—	384	18	544	24	704	24
B5	—	—	—	—	544	24	704	36
B7	—	—	—	—	544	24	704	36

CANDIDATES FOR THE REPLACEMENT OF THE ARRIA V GX DEV. KIT (NOT SAME FOOTPRINT UNFORTUNATELY)

1) Cyclone V GT dev. kit Intel DK-DEV-5CGTD9N:
   - onboard FPGA: 5CGTFD9E5F35C7N; year launched: 2011; TSMC's 28nm technology
   - Status: active; cost: 1.162,73€ (current, Digikey)
   - *porting of GEMROC FPGA firmware (A.C.R.): fits with timing closure warnings*

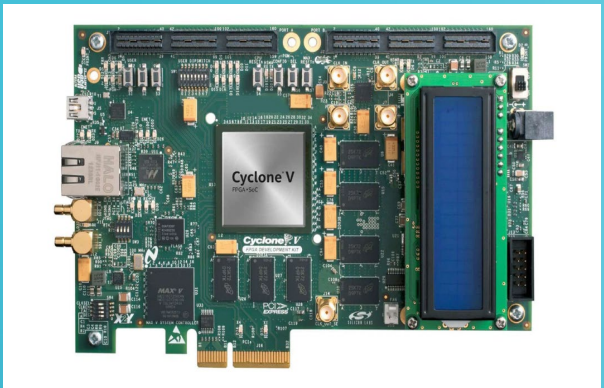
2) Cyclone V SX SoC dev. kit Critical Link MitySOM-5CSX:
   - onboard FPGA: 5CSXFC6C6U23C7N (SoC); year launched: 2012
   - Status: active; cost: 804,69€ (current, Digikey)
   - *porting of GEMROC FPGA firmware (A.C.R.): unsuccessful due to insufficient I/O*

3) Cyclone V SX SoC dev. kit Intel DK-DEV-5CSXC6N:
   - onboard FPGA: 5CSXFC6D6F31C6N (SoC) ; year launched: 2011
   - Status: active; cost: 1.606,71€ (current, Digikey)
   - *porting of GEMROC FPGA firmware (A.C.R.): fits with timing closure warnings for more pessimistic timing corners*

4) Cyclone 10 GX dev. kit Trenz TEI0006-03-220-5I:
   - onboard FPGA: 10CX220YF780I5G; year launched: 2017; TSMC's 20nm technology
   - Status: active; cost: 498.00€ (current, Trenz)
   - accessory carrier board Trenz TEIB0006-02 cost: 179,00€ (current, Trenz)
   - *porting of GEMROC FPGA firmware (A.C.R.): in progress – needs Quartus Pro Edition*

5) Cyclone 10 GX dev. kit Intel DK-DEV-10CX220-A:
   - onboard FPGA: 10CX220YF780E5G; year launched: 2017; TSMC's 20nm technology
   - Status: active; cost: 1.074,12€ (current, Digikey)
   - *porting of GEMROC FPGA firmware (A.C.R.): in progress – needs Quartus Pro Edition*

1) Cyclone V GT dev. kit Intel DK-DEV-5CGTD9N



DK-DEV-5CGTD9N

Codice Digi-Key	544-2781-ND
Produttore	Intel
Codice produttore	DK-DEV-5CGTD9N
Descrizione	CYCLONE V GT DEVELOPMENT KIT
Descrizione dettagliata	Cyclone V GT series FPGA Scheda di valutazione
Riferimento cliente	Riferimento cliente
Scheda tecnica	Scheda tecnica

Questa immagine può variare dall'originale. Per i particolari consulti la scheda tecnica.

44 in magazzino

Spedizione immediata

QUANTITÀ

Quantità

Aggiungi al carrello

Aggiungi all'elenco

Tutti i prezzi sono in EUR

Scatola

QTÀ	PREZZO UNITARIO	PREZZO TOT
1	€ 1.162,73000	€ 1.162,73

Prezzo unitario IVA esclusa: € 1.162,73000

Prezzo unitario IVA inclusa: € 1.418,53060

Attributi del prodotto

TIPO	DESCRIZIONE	SELEZIONA
Categoria	Schede di sviluppo, kit, programmatori Schede di valutazione - Embedded - Logica complessa (FPGA, CPLD)	
Produttore	Intel	
Serie	Cyclone® V GT	
Contenitore	Scatola	
Stato componente	Attivo	
Tipo	FPGA	
Da utilizzare con/Prodotti correlati	Cyclone V GT	
Dotazione	Scheda/e	
Codice componente base	DK-DEV	

PRO of Cyclone V GT dev. kit:

- dev. kit status: active
- same outline as the Arria V GX dev. kit to be replaced
- current GEMROC firmware fits the onboard FPGA (with timing closure warning)

CONS of Cyclone V GT dev. kit:

- onboard FPGA is mature. Status reported on the Intel web site: Launched in 2011
- development kit has different number/position of I/O connectors <-> not same footprint as the Arria V GX dev. kit to be replaced
- can’t be adapted to the GEMROC module without redesigning the enclosure
- cost

1) Cyclone V GT dev. kit Intel DK-DEV-5CGTD9N

FPGA device: 5CGTFD9E5F35C7N

QUARTUS PRIME (STANDARD VERSION) COMPILATION RESULTS:

Flow summary:

Timing closure report: paths with failing (probably recoverable) timing closure in all parameter corners

Table 1–3. Maximum Resource Counts for Cyclone V GX and GT Devices—*Preliminary*

Resource	Cyclone V GX Device					Cyclone V GT Device		
	5CGXC3	5CGXC4	5CGXC5	5CGXC7	5CGXC9	5CGTD5	5CGTD7	5CGTD9
ALM	11,698	18,868	28,868	56,415	113,585	28,868	56,415	113,585
LE	31,000	50,000	76,500	149,500	301,000	76,500	149,500	301,000
Block Memory (Kb)	1,400	2,500	3,800	6,500	11,600	3,800	6,500	11,600
MLAB Memory (Kb)	147	295	440	836	1,717	440	836	1,717
Variable-precision DSP Block	42	70	124	156	342	124	156	342
18 x 19 Multiplier	84	140	248	312	684	248	312	684
Fractional PLL (1)	4	6	6	7	8	6	7	8
3-Gbps Transceiver	3	6	6	9	12	—	—	—
5-Gbps Transceiver	—	—	—	—	—	6	9	12
GPIO	224	368	368	480	560	368	480	560
LVDS	48	90	100	122	122	100	122	122
PCIe Hard IP Block	1	2	2	2	2	2	2	2
Hard Memory Controller	1	2	2	2	2	2	2	2

Note to Table 1–3:

(1) The maximum fractional PLLs listed include general purpose PLLs and transceiver PLLs.

Table 1–6. Package Plan for Cyclone V E, GX, and GT Devices—*Preliminary* (1)

Device	F256 (17 mm)		U324 (15 mm)		U484 (19 mm)		F484 (23 mm)		F672 (27 mm)		F896 (31 mm)		F1152 (35 mm)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
5CEA2	144	—	176	—	288	—	288	—	—	—	—	—	—	—
5CEA4	144	—	176	—	288	—	288	—	—	—	—	—	—	—
5CEA5	—	—	—	—	272	—	272	—	—	—	—	—	—	—
5CEA7	—	—	—	—	240	—	240	—	336	—	480	—	—	—
5CEA9	—	—	—	—	—	—	224	—	336	—	448	—	—	—
5CGXC3 (2)	—	—	112	3	208	3	208	3	—	—	—	—	—	—
5CGXC4 (2)	—	—	—	—	224	6	240	6	336	6	—	—	—	—
5CGXC5 (2)	—	—	—	—	224	6	240	6	336	6	—	—	—	—
5CGXC7 (2)	—	—	—	—	240	6	240	6	336	9	480	9	—	—
5CGXC9 (2)	—	—	—	—	—	—	224	6	336	9	448	12	560	12
5CGTD5 (3)	—	—	—	—	240	6	240	6	368	6	—	—	—	—
5CGTD7 (3)	—	—	—	—	240	6	240	6	336	9	480	9	—	—
5CGTD9 (3)	—	—	—	—	—	—	224	6	336	9	448	12	560	12

Notes to Table 1–6:

(1) The arrows indicate the package vertical migration capability. You can also migrate your design across device densities in the same packaging option if the devices have the same dedicated pins, configuration pins, and power pins.

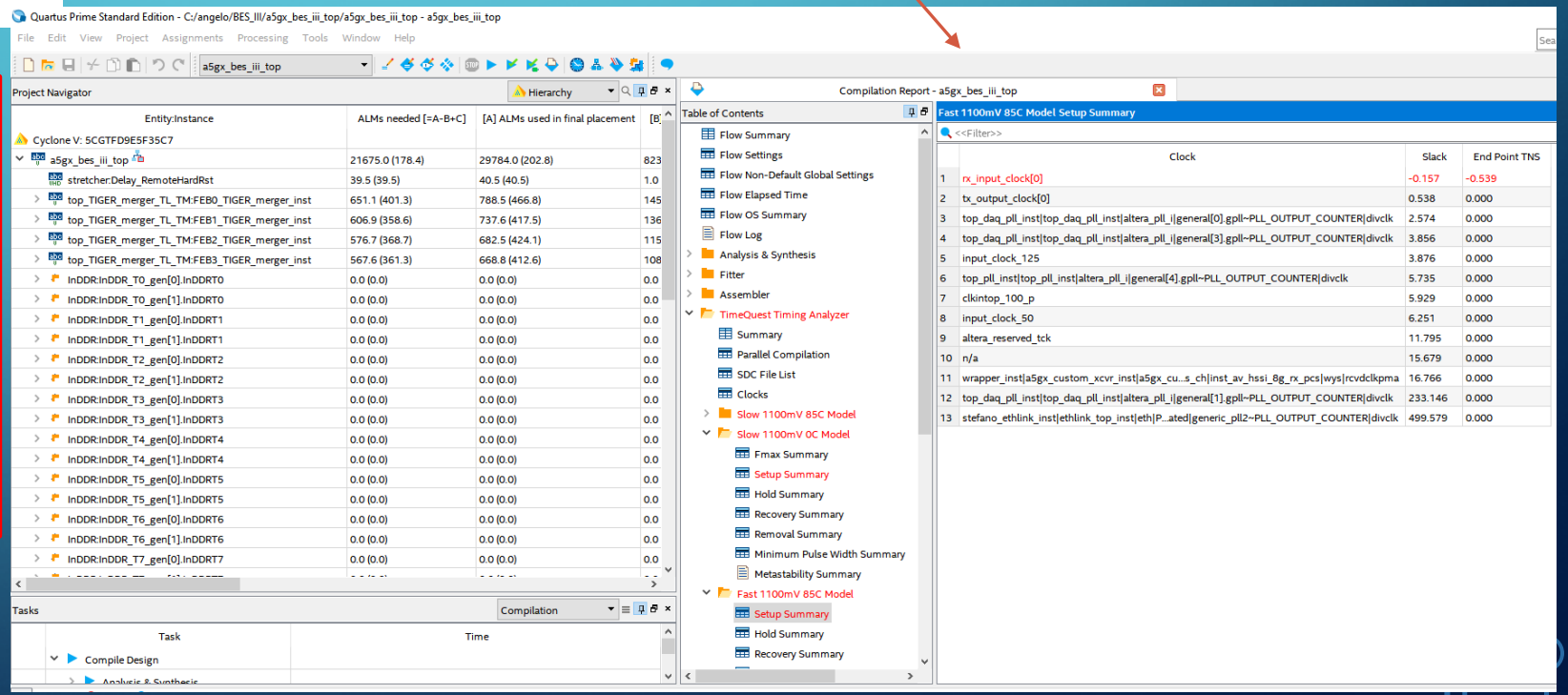
(2) The transceiver counts listed are for 3-Gbps transceivers.

(3) The transceiver counts listed are for 5-Gbps transceivers.

Flow Summary

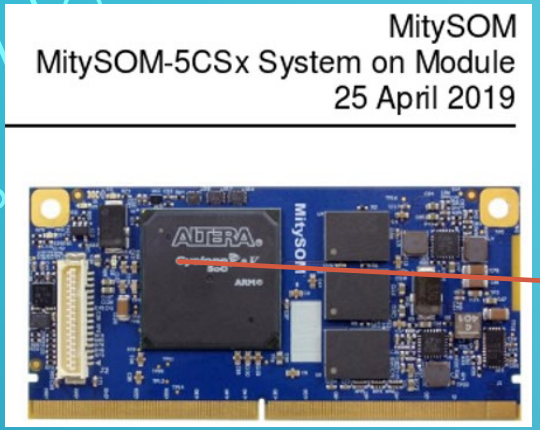
<<Filter>>

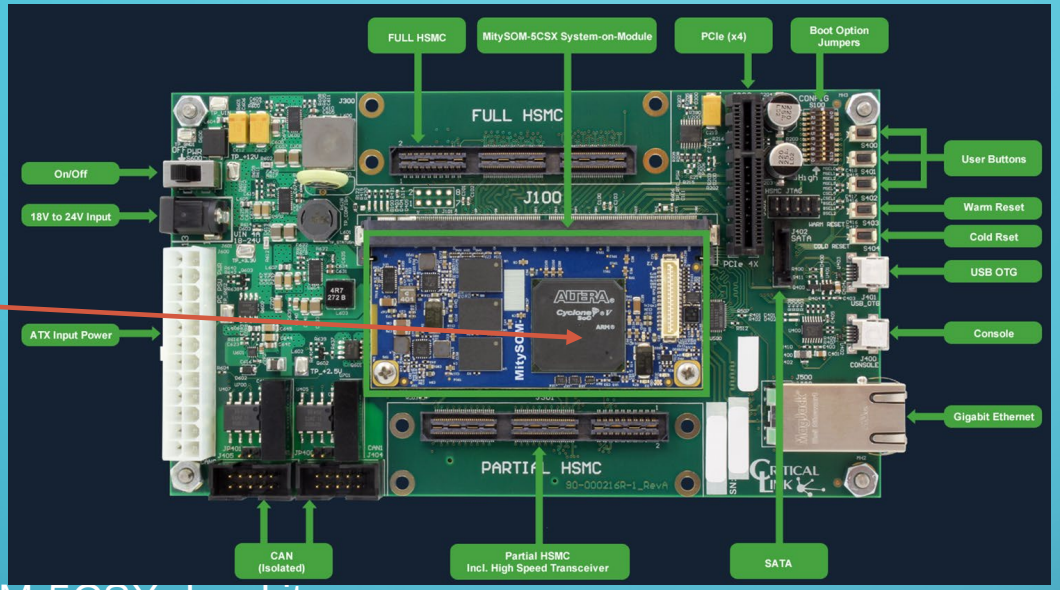
Flow Status	Successful - Mon Jan 10 15:05:12 2022
Quartus Prime Version	16.1.0 Build 196 10/24/2016 SJ Standard Edition
Revision Name	a5gx_bes_iii_top
Top-level Entity Name	a5gx_bes_iii_top
Family	Cyclone V
Device	5CGTFD9E5F35C7
Timing Models	Final
Logic utilization (in ALMs)	21,675 / 113,560 (19 %)
Total registers	49230
Total pins	179 / 616 (29 %)
Total virtual pins	0
Total block memory bits	4,354,756 / 12,492,800 (35 %)
Total DSP Blocks	3 / 342 (< 1 %)
Total HSSI RX PCSs	1 / 12 (8 %)
Total HSSI PMA RX Deserializers	1 / 12 (8 %)
Total HSSI TX PCSs	1 / 12 (8 %)
Total HSSI PMA TX Serializers	1 / 12 (8 %)
Total PLLs	5 / 20 (25 %)
Total DLLs	0 / 4 (0 %)

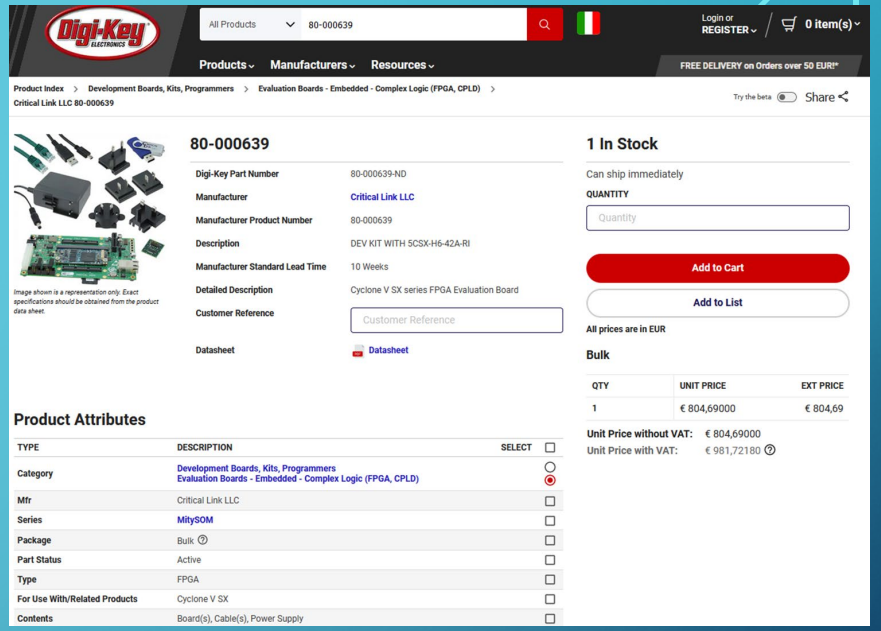


2) Cyclone V SX SoC dev. kit Critical Link MitySOM-5CSX

FPGA device: 5CSXFC6C6U23C7N







PRO of MitySOM-5CSX dev. kit:

- dev. kit status: active
- Similar outline as the Arria V GX dev. kit to be replaced
- **current GEMROC firmware DOES NOT FIT on the onboard FPGA due to I/O pin count limitation of the onboard FPGA (but it might be used for the GEMROC Fanout modules)**
- cost

CONS of MitySOM-5CSX dev. kit:

- onboard FPGA is mature. Status reported on the Intel web site: Launched in 2011
- development kit has different number/position of I/O connectors <-> not same footprint as the Arria V GX dev. kit to be replaced
- **could be adapted to the GEMROC module with little redesigning the enclosure**

2) Cyclone V SX SoC dev. kit Critical Link MitySOM-5CSX

FPGA device: 5CSXFC6C6U23C7N

Resource count of the SOM Module's FPGA would fit the GEMROCformware design but not the FPGA's pin count.

Table 1–5. Maximum Resource Counts for Cyclone V SX and ST Devices—*Preliminary* (Part 1 of 2)

Resource	Cyclone V SX Device			Cyclone V ST Device	
	5CSXC4	5CSXC5	5CSXC6	5CSTD5	5CSTD6
ALM	15,094	32,075	41,509	32,075	41,509
LE	40,000	85,000	110,000	85,000	110,000
Block Memory (Kb)	2,240	3,972	5,140	3,972	5,140
MLAB Memory (Kb)	220	480	621	480	621
Variable-precision DSP Block	58	87	112	87	112
18 x 19 Multiplier	116	174	224	174	224
FPGA Fractional PLL (1)	5	6	6	6	6
HPS PLL	3	3	3	3	3
3-Gbps Transceiver	6	9	9	—	—
5-Gbps Transceiver	—	—	—	9	9
FPGA GPIO	124	288	288	288	288
HPS I/O	188	188	188	188	188
LVDS	31	72	72	72	72

Table 1–5. Maximum Resource Counts for Cyclone V SX and ST Devices—*Preliminary* (Part 2 of 2)

Resource	Cyclone V SX Device			Cyclone V ST Device	
	5CSXC4	5CSXC5	5CSXC6	5CSTD5	5CSTD6
PCIe Hard IP Block	2	2	2	2	2
FPGA Memory Controller	1	1	1	1	1
HPS Memory Controller	1	1	1	1	1
ARM Cortex-A9 MPCore Processor	Dual-core	Dual-core	Dual-core	Dual-core	Dual-core

Note to Table 1–5:

(1) The maximum FPGA fractional PLLs listed include FPGA general purpose PLLs and transceiver PLLs.

Table 1–7. Package Plan for Cyclone V SE, SX, and ST Devices—*Preliminary* (1)

Device	U484 (19 mm)			U672 (23 mm)			F896 (31 mm)		
	GPIO	XCVR	HPS I/O	GPIO	XCVR	HPS I/O	GPIO	XCVR	HPS I/O
5CSEA2	66	—	161	124	—	188	—	—	—
5CSEA4	66	—	161	124	—	188	—	—	—
5CSEA5	66	—	161	124	—	188	288	—	188
5CSEA6	66	—	161	124	—	188	288	—	188
5CSXC4 (2)	—	—	—	124	6	188	—	—	—
5CSXC5 (2)	—	—	—	124	6	188	288	9	188
5CSXC6 (2)	—	—	—	124	6	188	288	9	188
5CSTD5 (3)	—	—	—	—	—	—	288	9	188
5CSTD6 (3)	—	—	—	—	—	—	288	9	188

Notes to Table 1–7:

(1) The arrows indicate the package vertical migration capability. You can also migrate your design across device densities in the same packaging option if the devices have the same dedicated pins, configuration pins, and power pins.

(2) The transceiver counts listed are for 3-Gbps transceivers.

(3) The transceiver counts listed are for 5-Gbps transceivers.

Critical Link, LLC
www.CriticalLink.com

MitySOM
MitySOM-5CSx System on Module
25 April 2019

FEATURES

- Intel Cyclone V - U672 SoC
  - **Up To Dual ARM Cortex- A9 MPU**
  - 925MHz Max clock speed
  - Dual NEON SIMD Coprocessors
  - 32 KB L1 Program Cache (per core)
  - 32 KB L1 Data Cache (per core)
  - 512 KB L2 Cache (shared)
  - 64 KB on-chip RAM
  - ECC Support
  - **Up To 133 User FPGA I/O Pins**
  - **44 CPU I/O Pins**
  - **6 High speed transceivers (SX only)**
- **Cyclone V Processor Choices**
  - Cyclone V SX (3.125 Gbps transceivers)
  - Cyclone V SE
- **Memory**
  - Up To 2GB DDR3 CPU RAM x32 bits + ECC
  - Up To 512MB DDR3 FPGA RAM x8 bits (optional)
  - Up To 272MB QPSI NOR FLASH
- **Mechanical**
  - 314-Pin Card Edge Connector
  - Small 82mm (3.2") x 39mm (1.5") size
- **Hard Processor System (HPS)**
  - Selection of boot sources
  - Up to 2 10/100/1000 Mbps Ethernet MACs
  - Up to 2 USB 2.0 OTG Ports
  - Up to 2 CAN Interfaces
  - Up to 2 UARTs
  - 1 MMC/SD/SDIO
  - Up to 4 I2C controllers
  - Up to 2 master/2 slave SPI
  - 3 HPS PLLs

Critical Link, LLC
www.CriticalLink.com

MitySOM-5CSX Development Kit
6 August 2014

FEATURES

MitySOM-5CSX Development Board

MitySOM-5CSX SoM Module

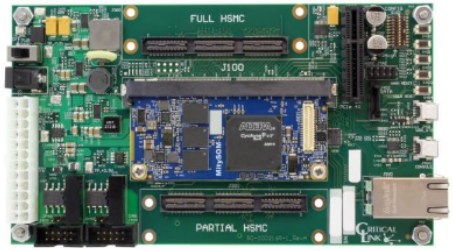
Additional Hardware Included:
- UART to USB Cable
- Ethernet Cable
- AC to DC 24V 2.7A Adapter

Integrated +2.5V/+3.3V/+5V/+12V Power Supplies

ATX Power Supply Compatible

Digital Interfaces:
- 10/100/1000 MBit Ethernet Interface
- Debug UART to USB
- USB OTG Interface
- Dual Electrically Isolated CAN Bus Interfaces
- SD/MMC Card Socket

Expansion
- Full HSMC Interface
- Partial HSMC Interface
- PCI-e x4

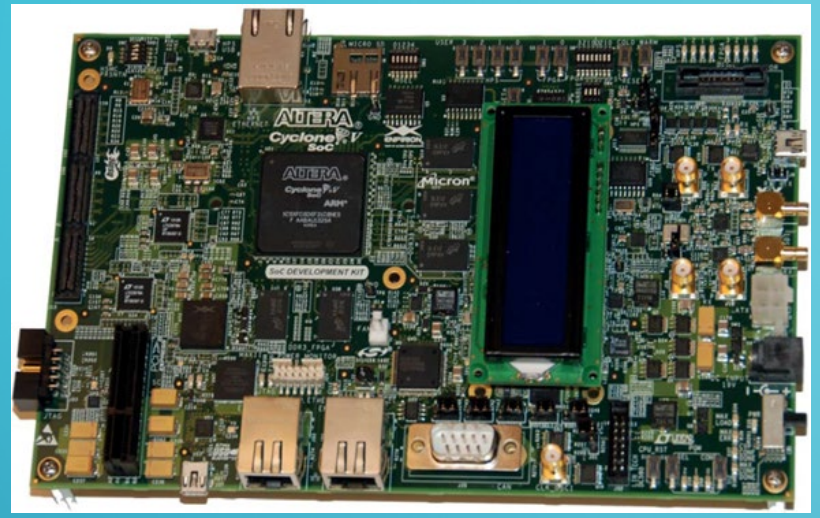


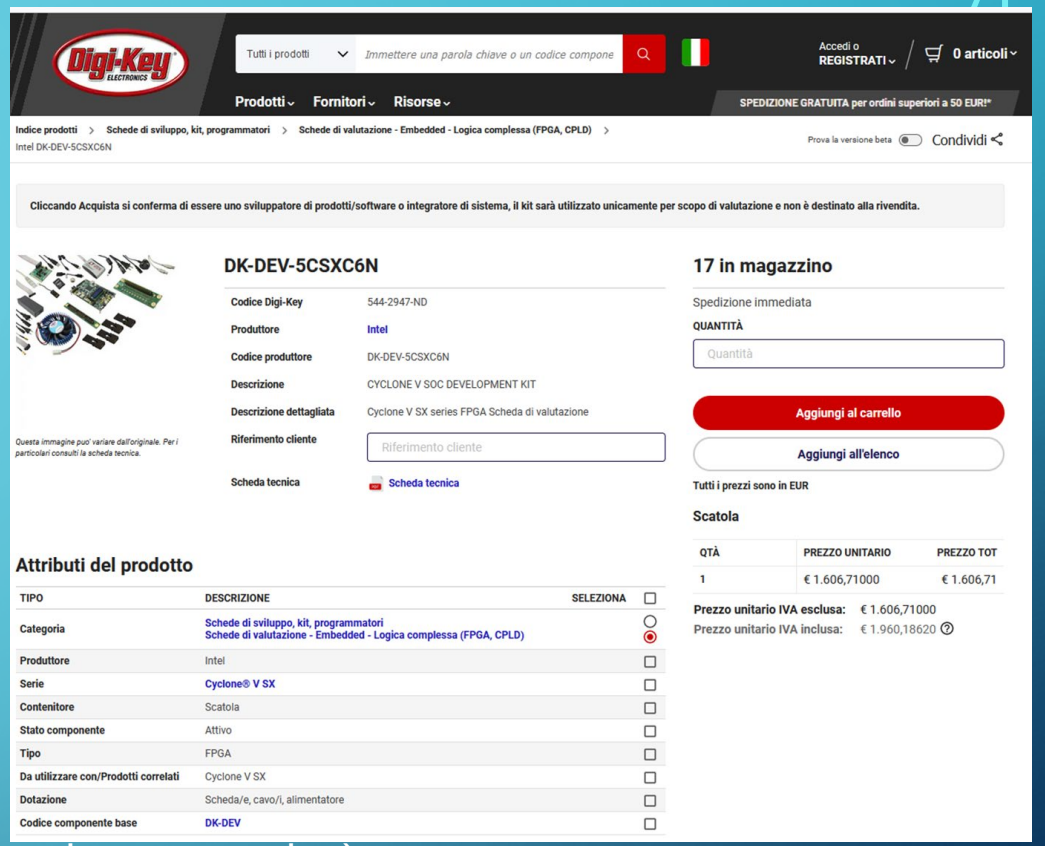
Software and Documentation:
- Linux Kernel
- uBoot
- Development Environment - Virtual Machine
- Development Board Schematics
- Development Board Gerber Files
- Development Board BOM

APPLICATIONS
- MitySOM-5CSX Evaluation
- Test and Measurement
- Factory Automation
- Industrial Automation
- Embedded Instrumentation
- Test and Measurement
- Rapid Prototyping

3) Cyclone V SX SoC dev. kit Intel DK-DEV-5CSXC6N

FPGA device: 5CSXFC6D6F31C6N





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Prodotti | Fornitori | Risorse | SPEDIZIONE GRATUITA per ordini superiori a 50 EUR!*

Indice prodotti > Schede di sviluppo, kit, programmatori > Schede di valutazione - Embedded - Logica complessa (FPGA, CPLD) > Intel DK-DEV-5CSXC6N

Prova la versione beta | Condividi

Cliccando Acquista si conferma di essere uno sviluppatore di prodotti/software o integratore di sistema, il kit sarà utilizzato unicamente per scopo di valutazione e non è destinato alla rivendita.

Questa immagine può variare dall'originale. Per i particolari consulti la scheda tecnica.

DK-DEV-5CSXC6N

Codice Digi-Key	544-2947-ND
Produttore	Intel
Codice produttore	DK-DEV-5CSXC6N
Descrizione	CYCLONE V SOC DEVELOPMENT KIT
Descrizione dettagliata	Cyclone V SX series FPGA Scheda di valutazione
Riferimento cliente	Riferimento cliente
Scheda tecnica	Scheda tecnica

17 in magazzino

Spedizione immediata

QUANTITÀ: Quantità

Aggiungi al carrello

Aggiungi all'elenco

Tutti i prezzi sono in EUR

Scatola

QTÀ	PREZZO UNITARIO	PREZZO TOT
1	€ 1.606,71000	€ 1.606,71

Prezzo unitario IVA esclusa: € 1.606,71000

Prezzo unitario IVA inclusa: € 1.960,18620

Attributi del prodotto

TIPO	DESCRIZIONE	SELEZIONA
Categoria	Schede di sviluppo, kit, programmatori Schede di valutazione - Embedded - Logica complessa (FPGA, CPLD)	
Produttore	Intel	
Serie	Cyclone® V SX	
Contenitore	Scatola	
Stato componente	Attivo	
Tipo	FPGA	
Da utilizzare con/Prodotti correlati	Cyclone V SX	
Dotazione	Scheda/e, cavo/i, alimentatore	
Codice componente base	DK-DEV	

PRO of Cyclone V SX dev. Kit Intel DK-DEV-5CSXC6N:

- dev. kit status: active
- current GEMROC firmware fits the onboard FPGA (with timing closure warning)

CONS of Cyclone V SX dev. Kit Intel DK-DEV-5CSXC6N:

- onboard FPGA is mature. Status reported on the Intel web site: Launched in 2011
- development kit has different outline and number/position of I/O connectors <-> not same footprint as the Arria V GX dev. kit to be replaced
- can't be adapted to the GEMROC module without redesigning the enclosure / using an HSMC to HSMC cable adapter
- cost

3) Cyclone V SX SoC dev. kit Intel DK-DEV-5CSXC6N

FPGA device: 5CSXFC6D6F31C6N

Table 1–5. Maximum Resource Counts for Cyclone V SX and ST Devices—*Preliminary* (Part 1 of 2)

Resource	Cyclone V SX Device			Cyclone V ST Device	
	5CSXC4	5CSXC5	5CSXC6	5CSTD5	5CSTD6
ALM	15,094	32,075	41,509	32,075	41,509
LE	40,000	85,000	110,000	85,000	110,000
Block Memory (Kb)	2,240	3,972	5,140	3,972	5,140
MLAB Memory (Kb)	220	480	621	480	621
Variable-precision DSP Block	58	87	112	87	112
18 x 19 Multiplier	116	174	224	174	224
FPGA Fractional PLL (1)	5	6	6	6	6
HPS PLL	3	3	3	3	3
3-Gbps Transceiver	6	9	9	—	—
5-Gbps Transceiver	—	—	—	9	9
FPGA GPIO	124	288	288	288	288
HPS I/O	188	188	188	188	188
LVDS	31	72	72	72	72

Table 1–5. Maximum Resource Counts for Cyclone V SX and ST Devices—*Preliminary* (Part 2 of 2)

Resource	Cyclone V SX Device			Cyclone V ST Device	
	5CSXC4	5CSXC5	5CSXC6	5CSTD5	5CSTD
PCIe Hard IP Block	2	2	2	2	2
FPGA Memory Controller	1	1	1	1	1
HPS Memory Controller	1	1	1	1	1
ARM Cortex-A9 MPCore Processor	Dual-core	Dual-core	Dual-core	Dual-core	Dual-co

Note to Table 1–5:

(1) The maximum FPGA fractional PLLs listed include FPGA general purpose PLLs and transceiver PLLs.

Table 1–7. Package Plan for Cyclone V SE, SX, and ST Devices—*Preliminary* (1)

Device	U484 (19 mm)			U672 (23 mm)			F896 (31 mm)		
	GPIO	XCVR	HPS I/O	GPIO	XCVR	HPS I/O	GPIO	XCVR	HPS I/O
5CSEA2	66	—	161	124	—	188	—	—	—
5CSEA4	66	—	161	124	—	188	—	—	—
5CSEA5	66	—	161	124	—	188	288	—	188
5CSEA6	66	—	161	124	—	188	288	—	188
5CSXC4 (2)	—	—	—	124	6	188	—	—	—
5CSXC5 (2)	—	—	—	124	6	188	288	9	188
5CSXC6 (2)	—	—	—	124	6	188	288	9	188
5CSTD5 (3)	—	—	—	—	—	—	288	9	188
5CSTD6 (3)	—	—	—	—	—	—	288	9	188

Notes to Table 1–7:

(1) The arrows indicate the package vertical migration capability. You can also migrate your design across device densities in the same packaging option if the devices have the same dedicated pins, configuration pins, and power pins.

(2) The transceiver counts listed are for 3-Gbps transceivers.

(3) The transceiver counts listed are for 5-Gbps transceivers.

QUARTUS PRIME (STANDARD VERSION) COMPILATION RESULTS:

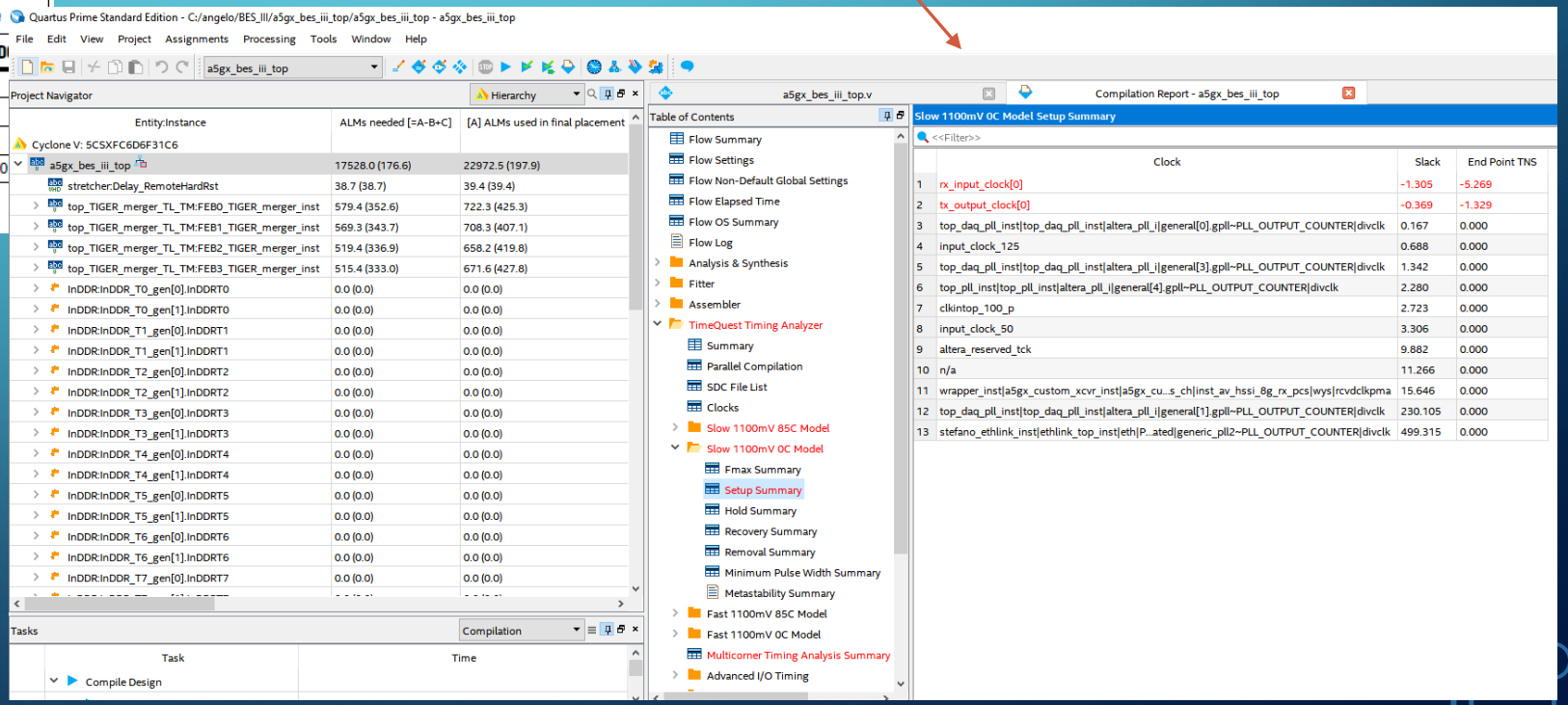
Flow summary:

Timing closure report: paths with failing (probably recoverable) timing closure only for more pessimistic corners

Flow Summary

<<Filter>>

Flow Status	Successful - Thu Feb 03 09:59:48 2022
Quartus Prime Version	16.1.0 Build 196 10/24/2016 SJ Standard Edition
Revision Name	a5gx_bes_iii_top
Top-level Entity Name	a5gx_bes_iii_top
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	17,528 / 41,910 (42 %)
Total registers	35487
Total pins	179 / 499 (36 %)
Total virtual pins	0
Total block memory bits	4,067,396 / 5,662,720 (72 %)
Total DSP Blocks	3 / 112 (3 %)
Total HSSI RX PCSs	1 / 9 (11 %)
Total HSSI PMA RX Deserializers	1 / 9 (11 %)
Total HSSI TX PCSs	1 / 9 (11 %)
Total HSSI PMA TX Serializers	1 / 9 (11 %)
Total PLLs	5 / 15 (33 %)
Total DLLs	0 / 4 (0 %)



4) Cyclone 10 GX dev. kit Trenz TEI0006-03-220-5I

FPGA device: 10CX220YF780I5G

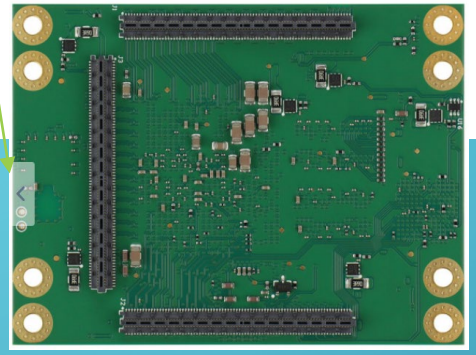
https://shop.trenz-electronic.de/en/Products/Trenz-Electronic/

TEM0005 - Microsemi SF2
LXO2000 - Lattice XO2-4000
Digilent
GOWIN Semiconductor
MEGA65
MYIR
OnSite Broadcast
Opsero
Sundance

Series	Device Family	Carrier Board	Launch Year	Expected EOL	Expected Life Cycle
TEI0001	MAX 10 FPGA	-	2014	2029	15
TEI0003	Cyclone 10	-	2017	2032	15
TEI0006	Cyclone 10	TEIB0006	2017	2032	15
TEI0009	Cyclone 10	-	2017	2032	15
TEI0010	MAX 10 FPGA	-	2014	2029	15
TEI0180	AGILEX	-	2019	2034	15

FPGA Module with Intel Cyclone 10 GX 10CX220, 2 GByte DDR3L, 6 x 8 cm

trenz electronic



€498.00 (592.62 € gross) *

Prices plus VAT plus shipping costs

expected to be available on 05-Aug-2022

1 | Add to shopping cart

Remember

Order number: TEI0006-03-220-5I
In Stock: 0
Article status: Full production

Quantity	Unit price
To 9	€498.00 (592.62 € gross) *
From 10	€448.20 (533.36 € gross) *
From 25	€448.20 (533.36 € gross) *

Contacts with Trenz to see if prototypes could be obtained sooner. Lead time is due to contingent semiconductors shortage

NOTE: porting of GEMROC firmware onto this platform in progress (A.C.R.): moving to Quartus Pro 20.4 (QSys → Platform Developer) requires updating all currently instantiated Intel/ALTERA IP blocks

Product information "FPGA Module with Intel Cyclone 10 GX 10CX220, 2 GByte DDR3L, 6 x 8 cm"

The predecessor of this article is TEI0006-02-220-5I. All changes are in the Product Change Notification (PCN).

The Trenz Electronic TEI0006 is an industrial grade module based on Intel Cyclone 10 GX. The Intel Cyclone 10 GX device family delivers higher core, transceiver, and I/O performance than the previous generation of low cost FPGAs.

Key Features

- Intel Cyclone 10 GX Industrial [10CX220YF780I5G]
  - Package: FBGA-780
  - Speed Grade: 5 (Fastest)
  - Temperature: -40°C to 100°C
  - Package compatible device, 10CX150 and 10CX105 as assembly variant on request
- 2 x SDRAM DDR3L memory IC 8 Gbit (1 GByte), Half rate: 533 MHz; Quarter rate: max. 800 MHz
- 2 x SPI Flash, 1 Gbit (128 MByte)
- 1 x Gigabit Ethernet
- Programmable oscillator
- Intel MAX 10 as system controller (CPLD)
- 2 KBit EEPROM memory
- 4 x User LEDs
- I/O interfaces: 226/94/46 (IO's/DIFF. Pairs/LVDS Pairs)
- Board to Board (B2B) connection: plug-on module with 3 x 160-pin Samtec Razor Beam (ST5) connectors
- 5 V power supply
- size: 6 x 8 cm

PRO of Cyclone 10 GX dev. kit Trenz TEI0006-03-220-5I:

- dev. kit status: active;
- onboard FPGA (20nm TSMC) launched in 2017 with EOL in 2032
- small outline: 6cm x 8cm
- cost

CONS of Cyclone 10 GX dev. kit Trenz TEI0006-03-220-5I:

- neither the module itself nor the motherboard carrying the module (see next slide) have number/position of I/O connectors compatible the Arria V GX dev. kit to be replaced
- a dedicated adapter to the GEMROC module would have to be designed; it could be made to fit the existing GEMROC module enclosure

4) Cyclone 10 GX dev. kit Trenz TEI0006-03-220-5I

FPGA device: 10CX220YF780I5G

Intel® Cyclone® 10 GX Device Overview
683485 | 2019.04.01

Intel Cyclone 10 GX Maximum Resources

Table 4. Maximum Resource Counts for Intel Cyclone 10 GX Devices

Resource		Product Line			
		10CX085	10CX105	10CX150	10CX220
Logic Elements (LE) (K)		85	104	150	220
ALM		31,000	38,000	54,770	80,330
Register		124,000	152,000	219,080	321,320
Memory (Kb)	M20K	5,820	7,640	9,500	11,740
	MLAB	653	799	1,152	1,690
Variable-precision DSP Block		84	125	156	192
18 x 19 Multiplier		168	250	312	384
Hard Floating-point Arithmetic		Yes	Yes	Yes	Yes
PLL	Fractional Synthesis	2	4	4	4
	I/O	4	6	6	6
12.5 Gbps Transceiver		6	12	12	12
GPIO (2)		216	284	284	284
LVDS Pair (3)		84	118	118	118
PCIe Hard IP Block		1	1	1	1
Hard Memory Interfaces		1	2	2	2

Intel Cyclone 10 GX Package Plan

Table 5. Package Plan for Intel Cyclone 10 GX Devices

The GPIO numbers include the I/O pins in the LVDS and 3 VI/O banks. In each device package, there is one 3 VI/O bank (48 pins).

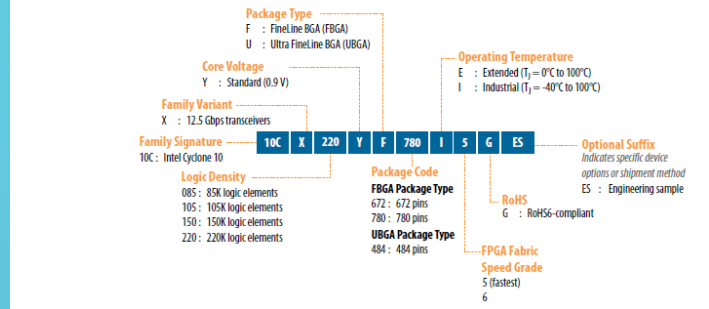
Product Line	Type	U484 484-pin UBGA			F672 672-pin FBGA			F780 780-pin FBGA		
	Size	19 mm × 19 mm			27 mm × 27 mm			29 mm × 29 mm		
	Ball Pitch	0.8 mm			1.0 mm			1.0 mm		
	I/O Type	GPIO	LVDS	XCVR	GPIO	LVDS	XCVR	GPIO	LVDS	XCVR
10CX085		188	70	6	216	84	6	—	—	—
10CX105		188	70	6	236	94	10	284	118	12
10CX150		188	70	6	236	94	10	284	118	12
10CX220		188	70	6	236	94	10	284	118	12

(2) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime Pro Edition software, the number of user I/Os includes transceiver I/Os.

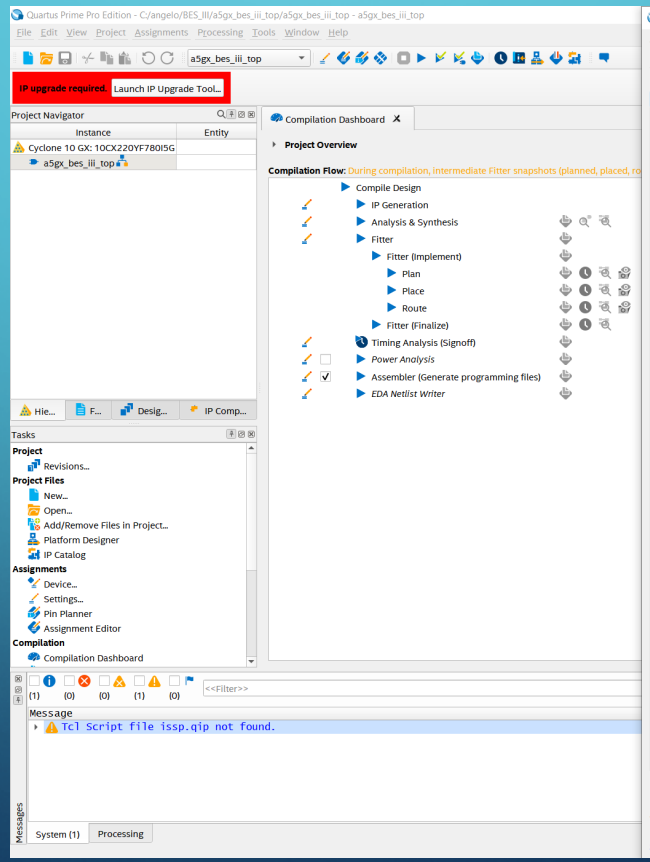
(3) Each LVDS I/O pair can be used as differential input or output.

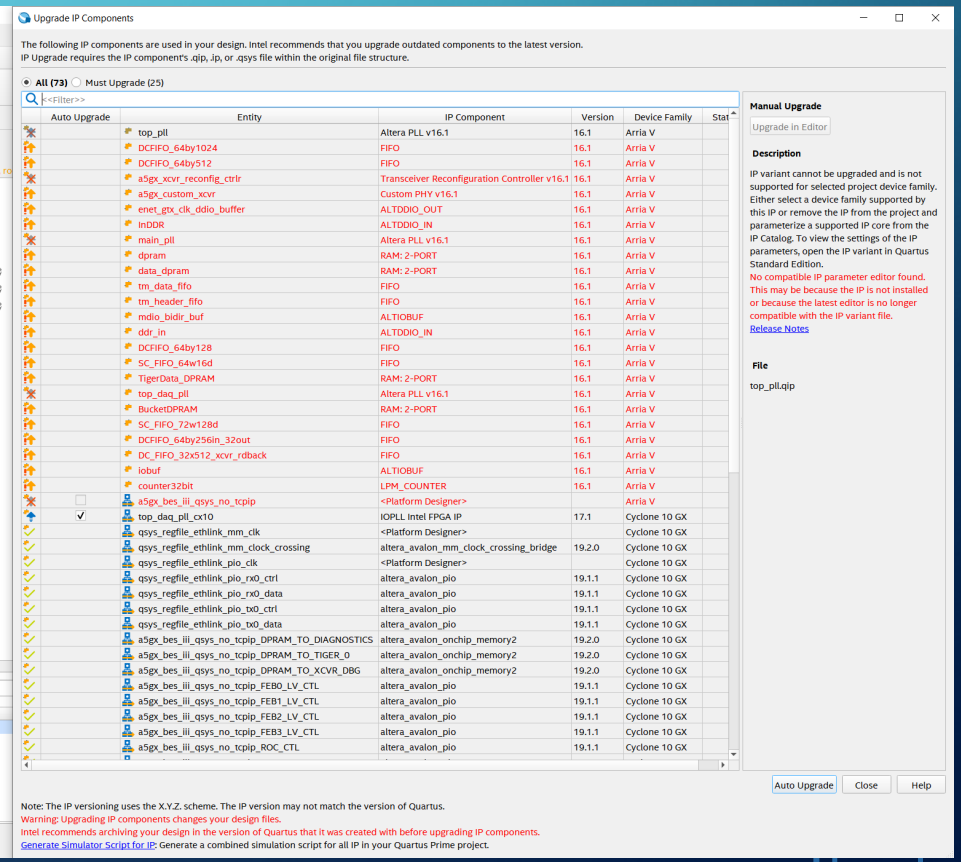
Intel Cyclone 10 GX Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Cyclone 10 GX Devices



QUARTUS PRIME PRO EDITION 20.4 COMPILATION RESULTS: MANUAL IP UPGRADE IS REQUIRED (work in progress)





4bis) Cyclone 10 GX dev. kit Trenz TEI0006-03-ALC13A

FPGA device: 10CX105YF780E5G

Product information "FPGA Module with Intel Cyclone 10 GX 10CX105, 128 MByte DDR3L, 8 x 6 cm"

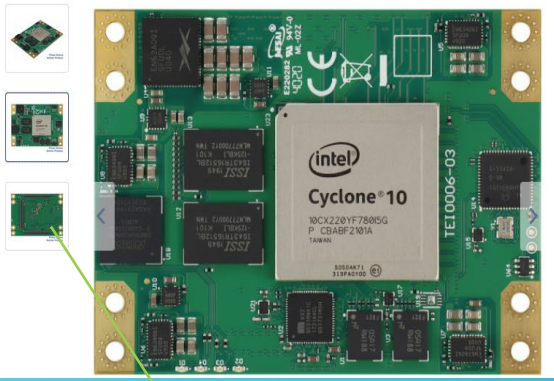
The Trenz Electronic TEI0006 is an industrial grade module based on Intel Cyclone 10 GX. The Intel Cyclone 10 GX device family delivers higher core, transceiver, and I/O performance than the previous generation of low cost FPGAs.

Key Features

- Intel Cyclone 10 GX Industrial [10CX105YF780E5G]
  - Package: FBGA-780
  - Speed Grade: 5 (Fastest)
  - Temperature: -40°C to 100°C
  - Package compatible device, 10CX150 and 10CX105 as assembly variant on request
- 128 MByte DDR3L SDRAM
- 2 x SPI Flash, 1 Gbit (total: 256 MByte)
- 1 x Gigabit Ethernet
- Programmable oscillator
- Intel MAX 10 as system controller (CPLD)
- 2 KBit EEPROM memory
- 4 x User LEDs
- I/O interfaces: 226/94/46 (IO's/DIFF. Pairs/LVDS Pairs)
- Board to Board (B2B) connection: plug-on module with 3 x 160-pin Samtec Razor Beam (ST5) connectors
- 5 V power supply
- size: 6 x 8 cm

FPGA Module with Intel Cyclone 10 GX 10CX105, 128 MByte DDR3L, 8 x 6 cm

trenz electronic



€299.00 (355.81 € gross) *

Prices plus VAT plus shipping costs

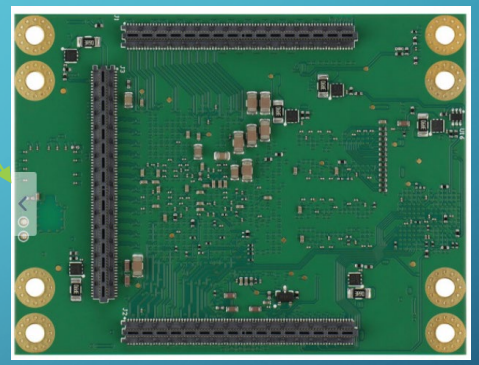
Possible to order, delivery time on request.

1 | Add to shopping cart

Remember

Order number: TEI0006-03-ALC13A
In Stock: 0
Article status: Full production

Quantity	Unit price
To 9	€299.00 (355.81 € gross) *
From 10	€269.10 (320.23 € gross) *



A less performant, same footprint version of the Trenz Cyclone 10 GX dev. kit of the previous slide exist

It could be matched to less demanding applications

PROs of Cyclone 10 GX dev. kit Trenz TEI0006-03-ALC13A:

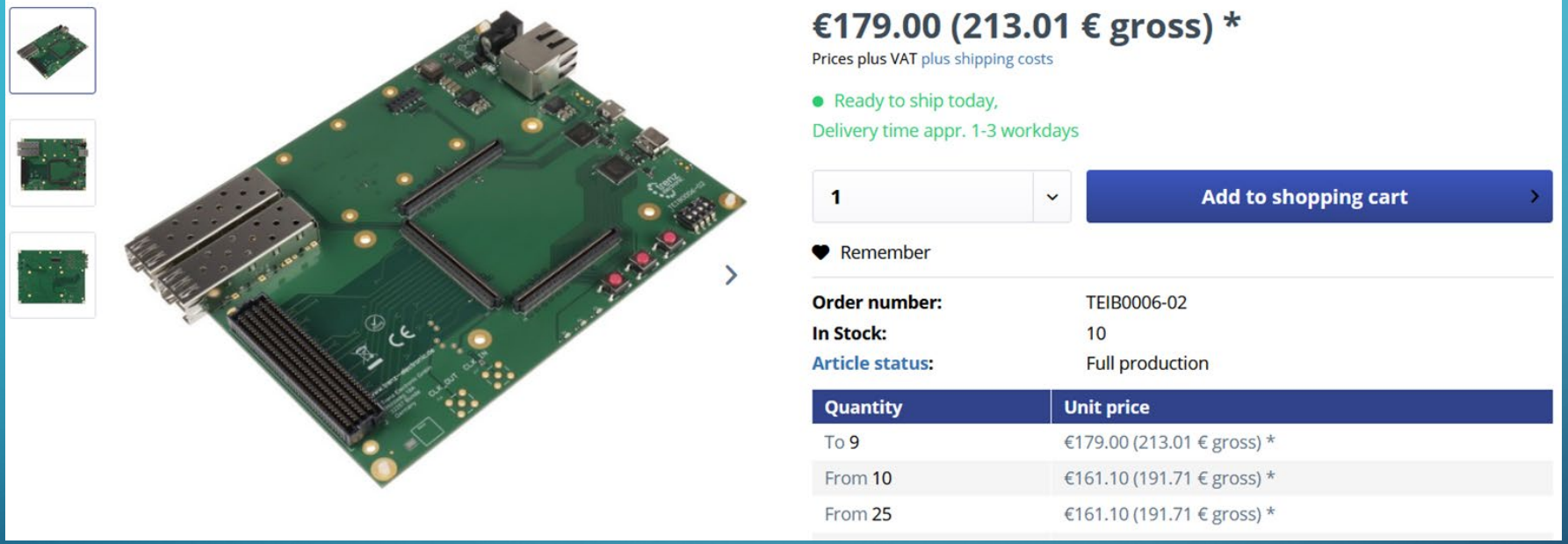
- dev. kit status: active;
- onboard FPGA (20nm TSMC) launched in 2017 with EOL in 2032
- small outline: 6cm x 8cm
- cost

4ter) Cyclone 10 GX dev. kit Trenz carrier board

The simple and functional carrier board shown below provides expansion ports (Ethernet, SFP, FMC) to the Cyclone 10 GX modules presented in the previous slides

Baseboard for Trenz Electronic TEI0006 Intel Cyclone 10 GX

trenz electronic



€179.00 (213.01 € gross) *

Prices plus VAT plus shipping costs

Ready to ship today,
Delivery time appr. 1-3 workdays

1 | Add to shopping cart

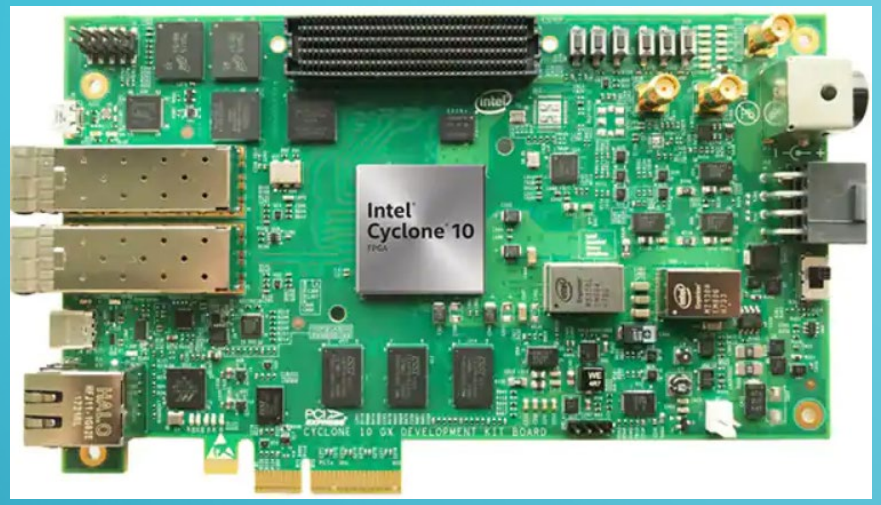
Remember

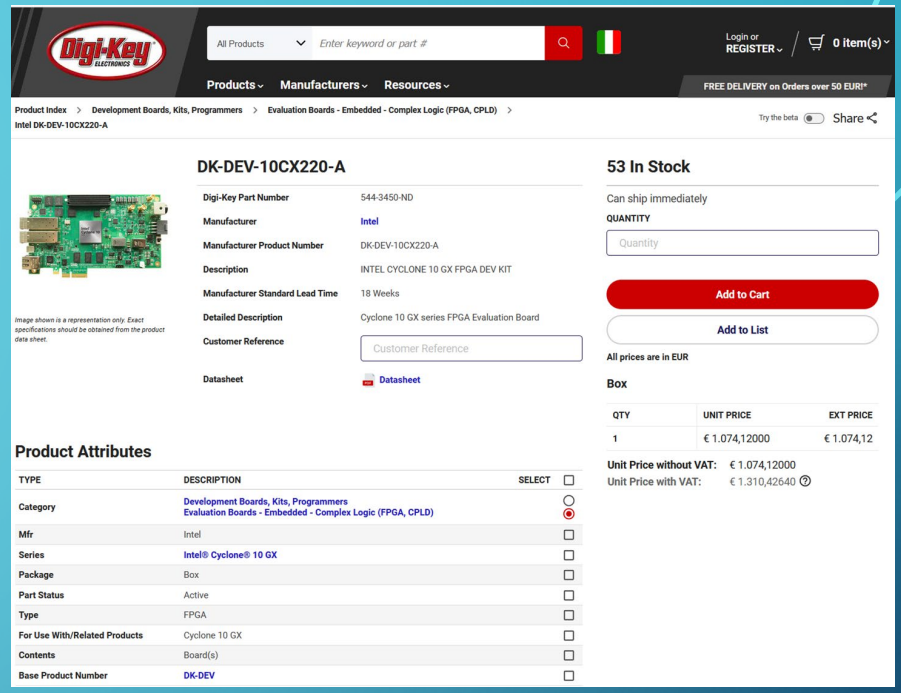
Order number:	TEIB0006-02
In Stock:	10
Article status:	Full production

Quantity	Unit price
To 9	€179.00 (213.01 € gross) *
From 10	€161.10 (191.71 € gross) *
From 25	€161.10 (191.71 € gross) *

5) Cyclone 10 GX dev. kit Intel DK-DEV-10CX220-A

FPGA device: 10CX220YF780E5G





NOTE: porting of GEMROC firmware onto this platform in progress (A.C.R.): moving to Quartus Pro 20.4 (QSys → Platform Developer) requires updating all currently instantiated Intel/ALTERA IP blocks

PRO of Cyclone 10 GX dev. kit Intel DK-DEV-10CX220-A:

- dev. kit status: active;
- onboard FPGA (20nm TSMC) launched in 2017 with EOL in 2032
- similar outline as the Arria V GX dev. kit to be replaced
- cost

CONS of Cyclone 10 GX dev. kit Intel DK-DEV-10CX220-A:

- the module has a footprint NOT COMPATIBLE, for number/position of I/O connectors, with the Arria V GX dev. kit to be replaced
- a dedicated adapter to the GEMROC module would have to be designed; it could probably be made to fit the existing GEMROC module enclosure

5) Cyclone 10 GX dev. kit Intel DK-DEV-10CX220-A

FPGA device: 10CX220YF780E5G

Intel® Cyclone® 10 GX Device Overview
683485 | 2019.04.01

intel

Intel Cyclone 10 GX Maximum Resources

Table 4. Maximum Resource Counts for Intel Cyclone 10 GX Devices

Resource		Product Line			
		10CX085	10CX105	10CX150	10CX220
Logic Elements (LE) (K)		85	104	150	220
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Register		124,000	152,000	219,080	321,320
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	MLAB	653	799	1,152	1,690
Variable-precision DSP Block		84	125	156	192
18 x 19 Multiplier		168	250	312	384
Hard Floating-point Arithmetic		Yes	Yes	Yes	Yes
PLL	Fractional Synthesis	2	4	4	4
	I/O	4	6	6	6
12.5 Gbps Transceiver		6	12	12	12
GPIO (2)		216	284	284	284
LVDS Pair (3)		84	118	118	118
PCIe Hard IP Block		1	1	1	1
Hard Memory Interfaces		1	2	2	2

Intel Cyclone 10 GX Package Plan

Table 5. Package Plan for Intel Cyclone 10 GX Devices

The GPIO numbers include the I/O pins in the LVDS and 3 VI/O banks. In each device package, there is one 3 VI/O bank (48 pins).

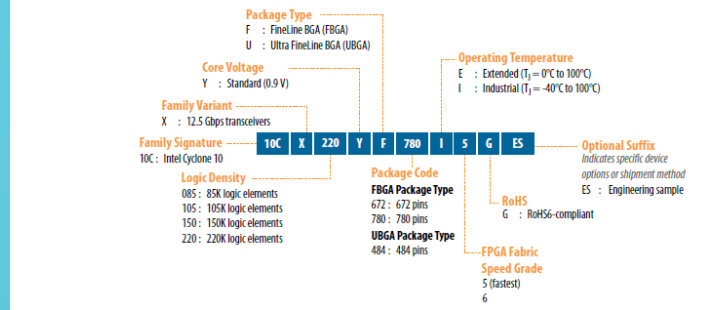
Product Line	Type	U484 484-pin UBGA			F672 672-pin FBGA			F780 780-pin FBGA		
	Size	19 mm × 19 mm			27 mm × 27 mm			29 mm × 29 mm		
	Ball Pitch	0.8 mm			1.0 mm			1.0 mm		
	I/O Type	GPIO	LVDS	XCVR	GPIO	LVDS	XCVR	GPIO	LVDS	XCVR
10CX085		188	70	6	216	84	6	—	—	—
10CX105		188	70	6	236	94	10	284	118	12
10CX150		188	70	6	236	94	10	284	118	12
10CX220		188	70	6	236	94	10	284	118	12

(2) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime Pro Edition software, the number of user I/Os includes transceiver I/Os.

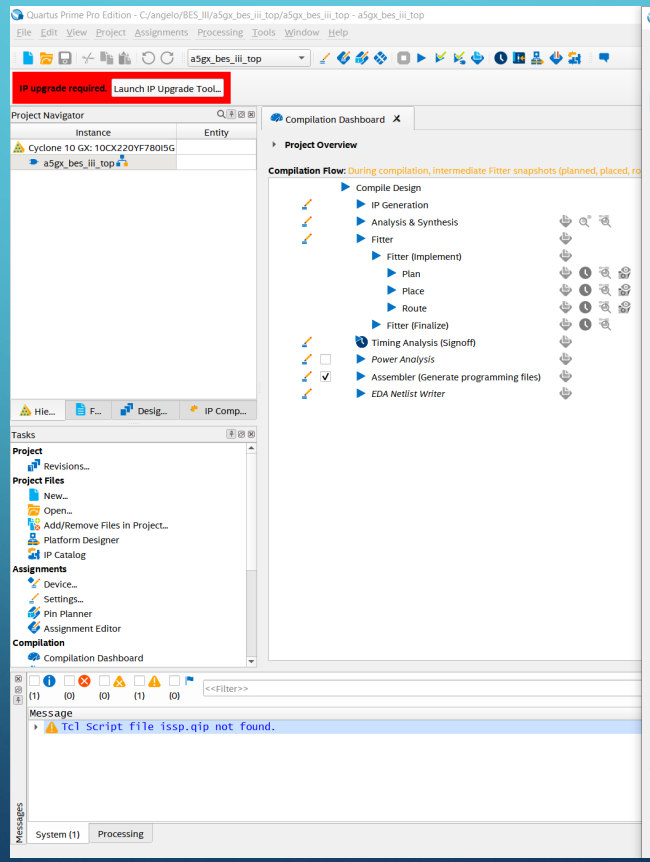
(3) Each LVDS I/O pair can be used as differential input or output.

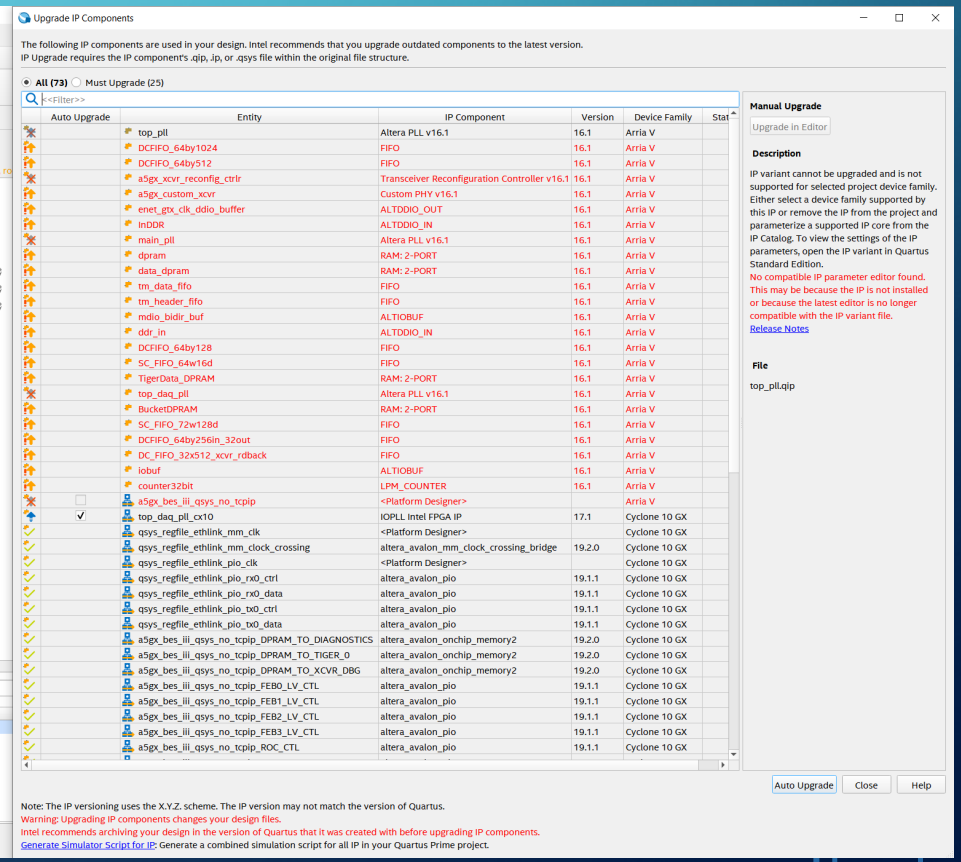
Intel Cyclone 10 GX Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Cyclone 10 GX Devices



QUARTUS PRIME PRO EDITION 20.4 COMPILATION RESULTS: MANUAL IP UPGRADE IS REQUIRED (work in progress)

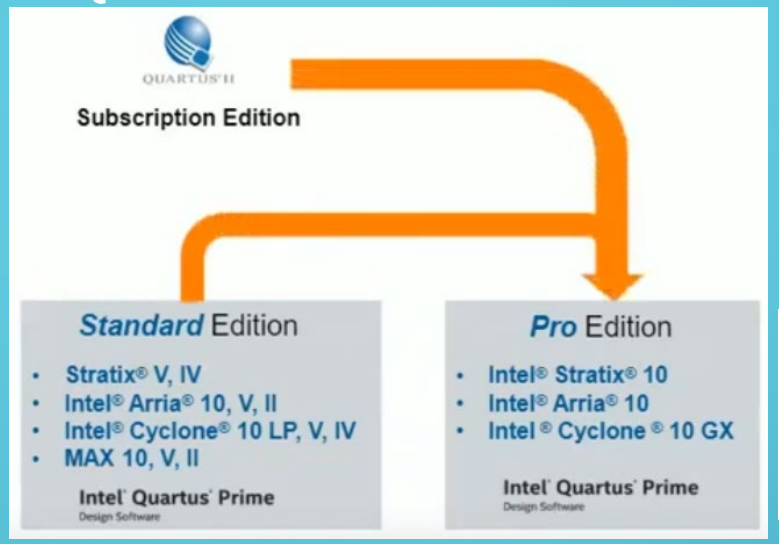




Migrating designs to the Intel Quartus Pro Edition

Intel® Quartus® Prime Standard Edition

The Intel® Quartus® Prime Standard Edition Software includes extensive support for earlier device families in addition to the Intel® Cyclone® 10 LP device family.



Intel® Quartus® Prime Pro Edition

The Intel® Quartus® Prime Pro Edition Software is optimized to support the advanced features in next-generation FPGAs and SoCs with the Intel® Agilex™, Intel® Stratix® 10, Intel® Arria® 10, and Intel® Cyclone® 10 GX device families.

https://www.youtube.com › watch

Platform Designer in the Intel® Quartus® Prime Pro Edition ...

Platform Designer, available in the Pro Edition of the Intel® Quartus® Prime software, expands the ease of use, flexibilit...

YouTube · Intel FPGA · 1 feb 2018

10 momenti chiave in questo video

Mancanti: ~~migrating~~ | Deve includere: migrating

https://www.youtube.com › watch

Migrating to the Intel® Quartus® Prime Pro Edition Software

... **software** is designed to take your advanced FPGA **designs** to the next ... In most cases, **migrating** an existing Intel...

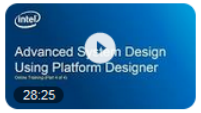
YouTube · Intel FPGA · 21 ago 2018

In questo video What is Quartus Prime?

Mancanti: ~~qsys~~ | Deve includere: qsys

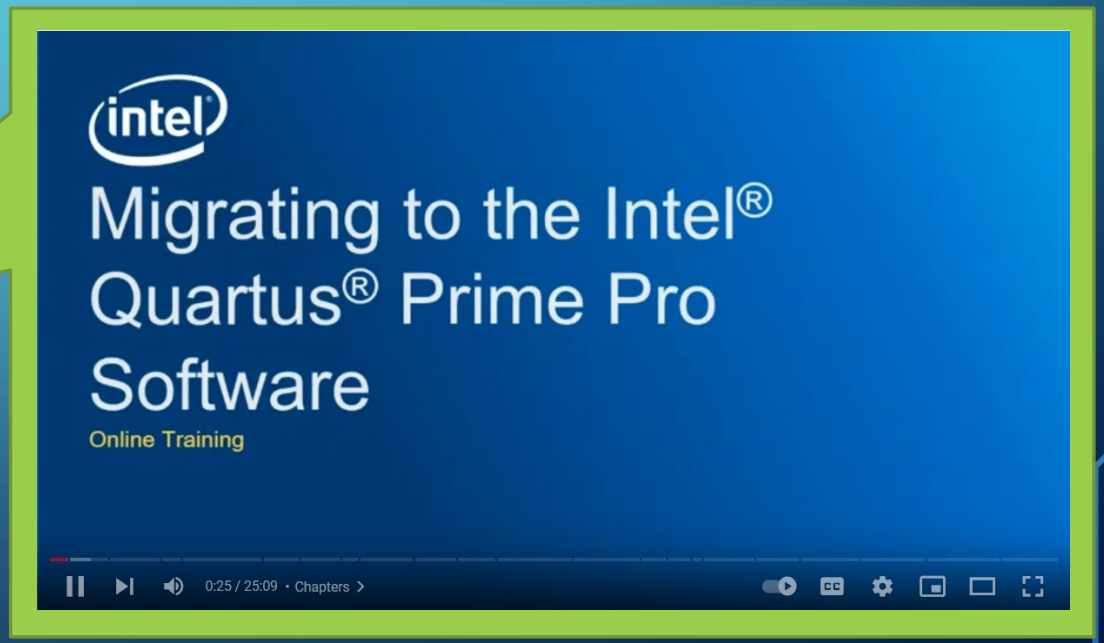
https://www.youtube.com › watch

Advanced System Design Using Platform Designer - YouTube



This training is part 4 of 4. The **Platform Designer** system integration tool saves significant time by automatically...

YouTube · Intel FPGA · 17 ago 2018



Migrating designs to the Intel Quartus Pro Edition

Update Assignments to Reference Instances Only

Other Intel® Quartus® Prime software products

- Assignments to instantiated entities must reference both entity and instance names in project hierarchy
- Example: `entity_a:a|entity_b:b|entity_c:c`

Quartus Prime Pro Edition

- Entity names should no longer be used in assignments; use instance names only
- Entity names still accepted by the compiler (for now) but are ignored and generate warning messages
- Example: `a|b|c`

Action: remove entity names from existing assignments directly in **.qsf** file or through Assignment Editor, and avoid using them in new assignments

Check Entity Name Use in **.sdc** and Related Scripts

Other Intel® Quartus® Prime software products

- Supports use of both entity and instances names for constraints, similar to their use in project assignments

Intel Quartus Prime Pro Edition

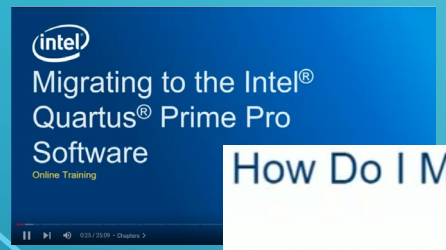
- Continues to support use of both entity and instance names with no generated warnings
- However, certain commands in scripts that perform custom name processing return strings without entity names
- Processing of returned strings must reflect this

```
set_false_path -to [get_registers
    "counter:*|*:acc"]
```

- `get_registers` example that works in all Quartus products due to wildcard use:

Check References to Synthesized Node Names

- Names may change significantly between other Intel® Quartus® Prime software product projects and Intel Quartus Prime Pro Edition
  - Names never guaranteed to remain consistent in other Quartus software products
  - More significant changes when moving to Pro Edition
- Example: `foo~123` may synthesize in Pro Edition as `foo.567`
- Check **.qsf**, **.sdc**, and Tcl script references to synthesized nodes
- Use Node Finder to help locate and fix
- Also check names of duplicated registers and PLL clock outputs



How Do I Migrate?

- Update your project assignments (.qsf), timing constraints (.sdc), and Tcl scripts
- Regenerate your IP
- Adjust your RTL for the new Intel® Quartus® Prime Pro synthesis engine

Why Regenerate IP?

In other Intel® Quartus® Prime Software products

- Proprietary Verilog configuration scheme used in the top level of all IP cores and Platform Designer for synthesis
- Prevents ambiguous instantiation errors during synthesis due to identical naming or multiple instantiations of RTL entities
- Still potential for such errors during simulation, requiring a fix
  - Create separate Verilog configuration
  - Delete duplicate entities
  - Rename conflicting entities

In Intel Quartus Prime Pro Edition

- Proprietary Verilog configuration not used or supported
- All variants of a particular core (even with identical parameterization and functionality) compiled into the same library for entire project
  - Example: all variants of Intel® Arria® 10 PCIe* core compiled into **altera_pcie_a10_hip_151** library
- Simulation and synthesis file sets instantiate entities identically
- Generated IP file directory structure now matches compilation library

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Conclusione:

Penso sia meglio partire da un progetto di esempio in Quartus Prime Pro edition ed integrare i moduli specifici di BES-III dedicati mano a mano….

How Do I Migrate?

- Update your project assignments (.qsf), timing constraints (.sdc), and Tcl scripts
- Regenerate your IP
- Adjust your RTL for the new Intel® Quartus® Prime Pro synthesis engine
  - Discussed in free online training "Using the synthesis engine in the Quartus Prime Software"
  - http://wl.altera.com/education/training/courses/OSYNQPRO