PSD Trigger
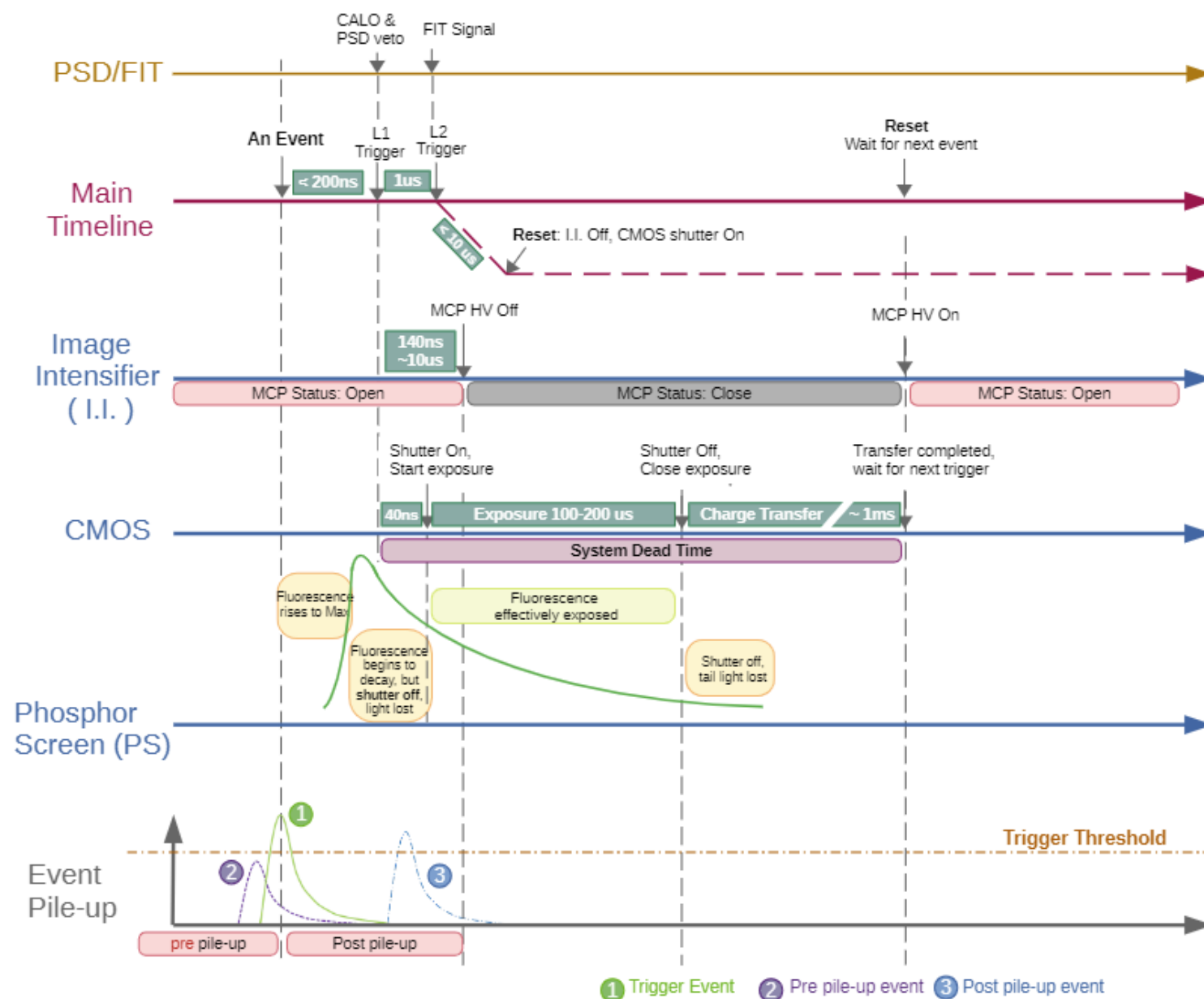
From the draft of the trigger chapter from Jorge, Ming and many others

PSD Logic

▶ The example is done assuming the tile option but for the bar option the logic is almost the same

▶ The size and position of

Analog

Digital

β-Chip

FPGA

Tile/bar trigger signal

L1 TRG

< 200ns