PSD trigger design

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PSD trigger for baseline LEG (L1)

- Baseline LEG, which requires low energy deposition in CALO and PSD veto to suppress mainly the proton background
  - at least 0.35 GeV deposited in the top or in any CALO lateral shell and the combined veto of the bottom shell (E < 0.1 GeV) and the PSD sides (E<0.001 GeV)
  - Expected trigger rates for downward-going particles include p, He, C, O, e- is 4.5Hz(Ave.) and 28.7(Max.)
  - A fast signal, within 200 ns, is required in order to avoid light losses in the CALO IsCMOS camera.

Composition of L1 latency

- Front part (FEE of a specific subtrigger)
  - The CALO PM front part latency includes the PMT transit time (30-50 ns) and the front electronics processing time (10-15 ns). The sum of the CALO PMT front part latency is around 40-65 ns.
- Back part(main trigger board)
  - the alignment compensation
  - the logic processing time
  - the distribution cable latency

as shown in table 1.7. In order to ensure a total L1 latency within 175 ns, the front part latency(L1 FEE latency) of the subtriggers involved in L1 need to be in the range of 40-65 ns, such as CALO PM and PSD veto.

Table 1.7 Composition of L1 latency

composition	latency [ns]
front part	
CALO PM	40-65
PSD	40-65
back part	
alignment compensation	0-10
BEE logic	50-80
cable	15-20
SUM	175

The L1-L2 idea

- In baseline L1, the physics triggers(HE and LEG), should be around 100 Hz, by taking account of the camera readout dead time(1.25ms)
- The advanced trigger design is based on the inclusion of a second level trigger (L2), with a higher latency (~1 μs) compared to the baseline (L1) trigger signal, which incorporates additional information to provide an efficient extension of the energy range for specific samples
- The multilevel trigger design releases the strong constraints on the maximum L1 rate, which can routinely work at ~1 kHz with a negligible dead time (~1%), provided that the L2 reduces the final trigger rate to ~100 Hz
  - by fast rest for all(a large part) of those passed L2

PSD trigger for advanced high Z (L2)

- A Z > 2 trigger based on a high threshold discriminator on the PSD signals can be used to suppress the dominant proton and helium contributions, while keeping most of the low energy heavy nucleus by a reduction of HE threshold(i.e. 2GeV)
- The implementation of the high Z trigger logic will mainly depend on the final latency of the high Z PSD signals.
  - if PSD is able to generate a high Z trigger signal within 200 ns (in parallel with the veto signal), it will be directly included in the L1 logic.
  - Otherwise, the high Z trigger could be incorporated in the L2

PSD DAQ

- Events passed only L1, normal DAQ for all readout systems
- Events passed both L1 and L2
  - Fast reset of all events for those slow readout systems, i.e. the camera
  - A scaled events could be recorded by those fast readout systems
    - with negligible live time loss (i.e. < 1%)
    - the scale factor depends on the readout dead time

Back-splash effect

Back-splash effect will greatly degrade the PID performances.

In order to suppress the back splash effect, ~100 ps time resolution is required.

Working plan

- End of 2022, check low delay timing for LEG
- Middle of 2023, sign IDS
- End of 2024, global verification
  - Protocol, timing and logic, efficiency