

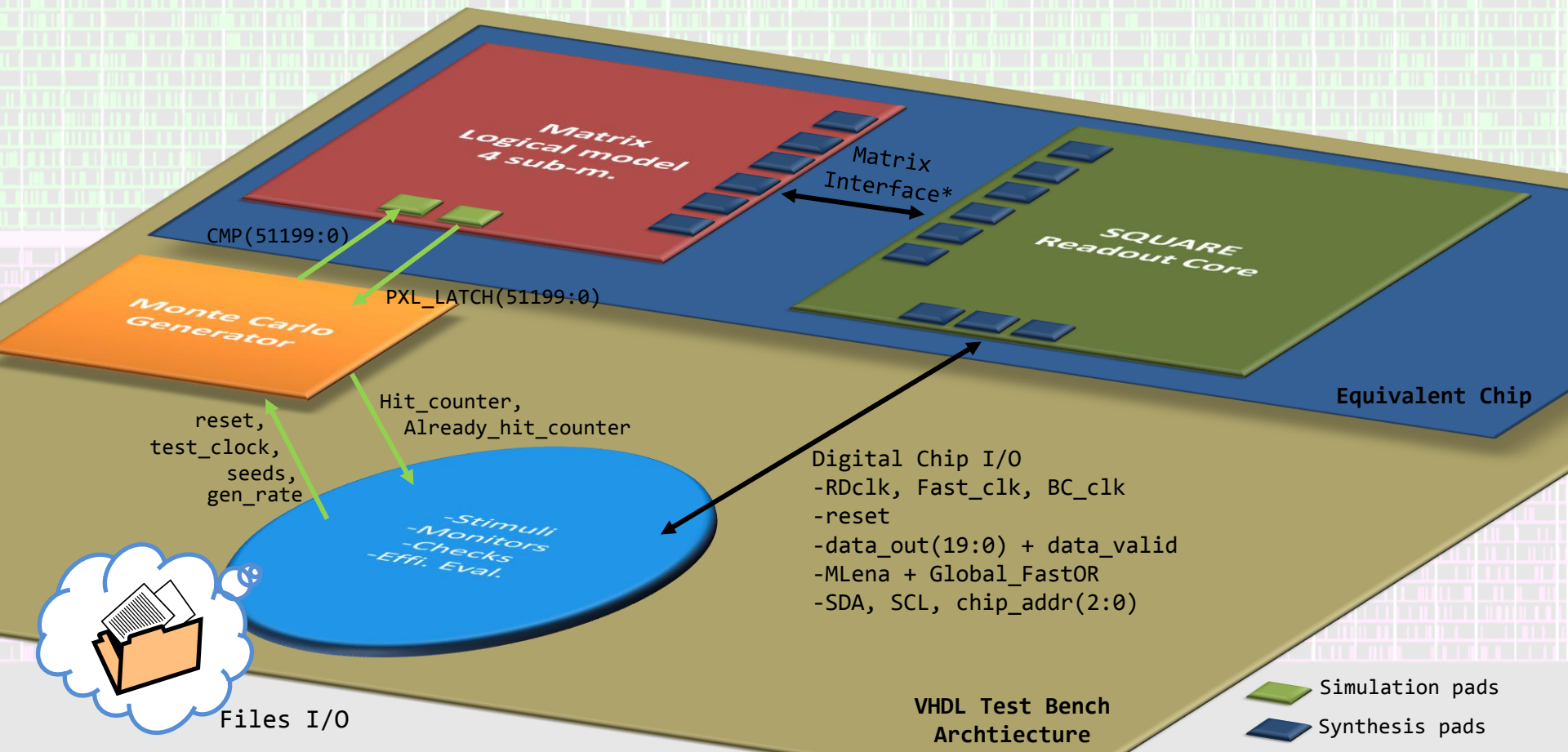
Simulation Meeting

Summary

- Simulation Environment
- Physical Events Simulations
- Matrix Interface
- Masks, Reset, Registers & Configurations

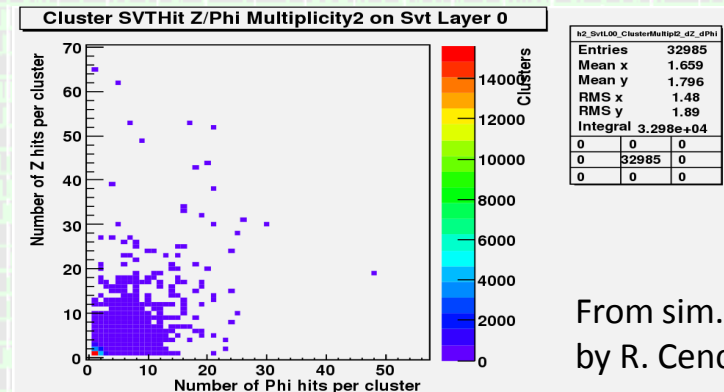
Simulation Environment

- Simulation Tool: **Modelsim SE 6.3f**
- Simulation components
 - **Readout Core Arch. SQUARE** (.vhd synthesizable code)
 - **Monte Carlo Generator** (.vhd **NOT** synthesizable code)
 - **Matrix Behavioral Model** (.vhd code)
 - **Test Bench** (.vhd code)

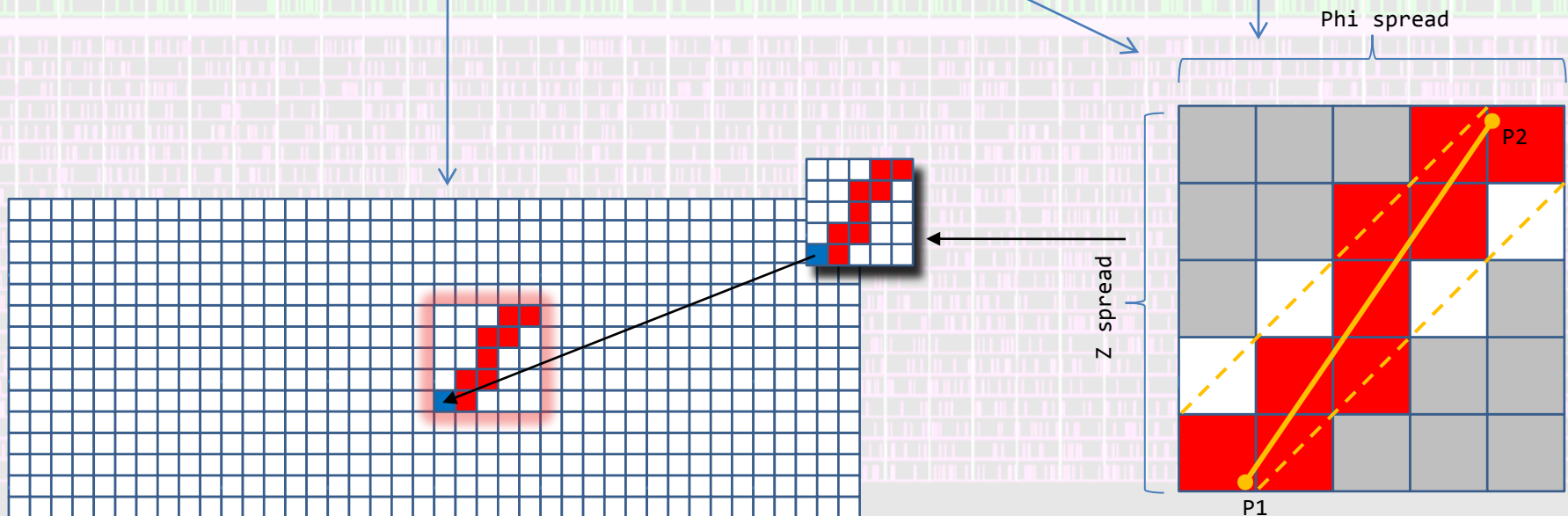


Physical Events Simulation

- Monte Carlo generator
 - Stand Alone version (independent from Matrix logical model)
 - Generation of clustered events
 - Knobs: 
 - Cluster dispersion distribution in (z,phi)
 - Physical time resolution (test_clock), hit/miss thresholds = Global hit rate
 - Arbitrary pattern extraction by geometrical rules
 - Pattern check (grey pixels are forbidden)
 - Pattern application to a random pixel of the matrix



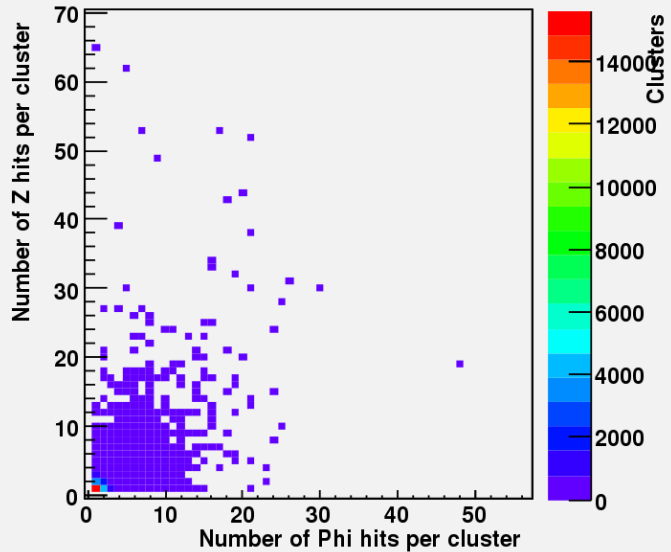
Cluster spread
extraction
Es. (5,5)



Cluster Pattern Extraction

Implemented cluster spread distribution zeta/phi from physics simulations (by R.Cenci)

Cluster SVTHit Z/Phi Multiplicity2 on Svt Layer 0

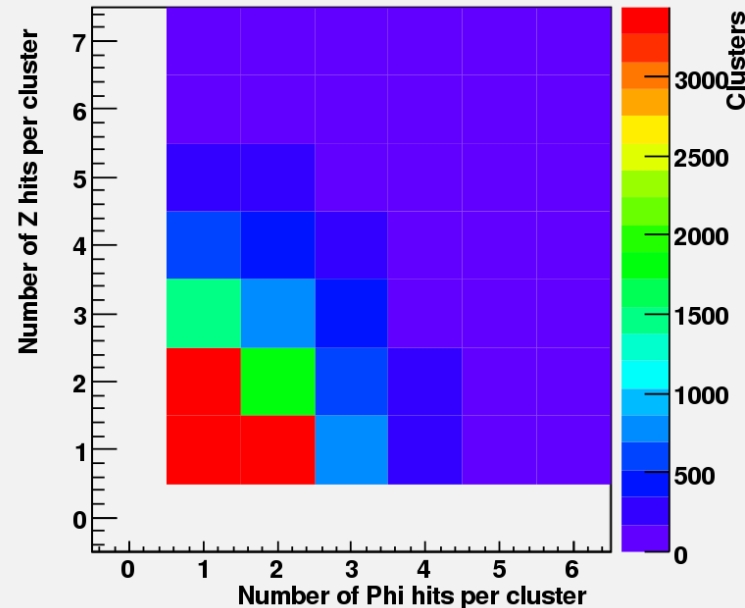


h2_SvtL00_ClusterMultiplicity2_dZ_dPhi		
Entries	32985	
Mean x	1.659	
Mean y	1.796	
RMS x	1.48	
RMS y	1.89	
Integral	3.298e+04	
0	0	0
0	32985	0
0	0	0

%	1	2	3	4	phi
1	47,27520	12,65198	2,46868	0,70666	...
2	10,62458	5,80757	1,76511	0,55545	
3	4,31710	2,30513	1,06770	0,40116	
4	2,00580	1,15102	0,57397	0,26538	
zeta	...				

Zoom/Equalize

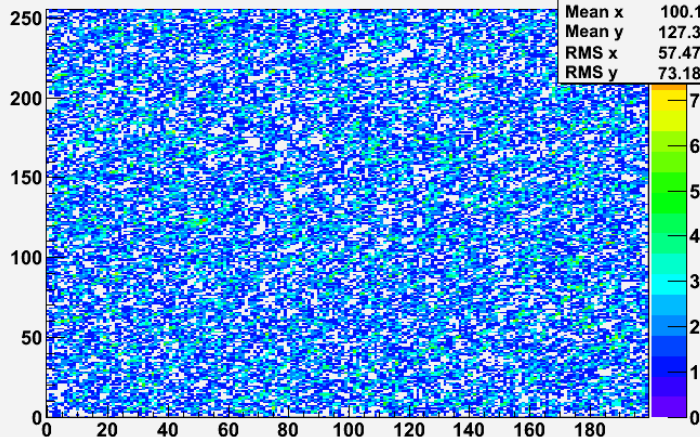
Cluster SVTHit Z/Phi Multiplicity2 on Svt Layer 0



h2_SvtL00_ClusterMultiplicity2_dZ_dPhi		
Entries	32985	
Mean x	1.507	
Mean y	1.635	
RMS x	0.883	
RMS y	1.093	
Integral	3.221e+04	
0	249	172
0	32208	356
0	0	0

Implemented and simulated

Readout hit dispersion



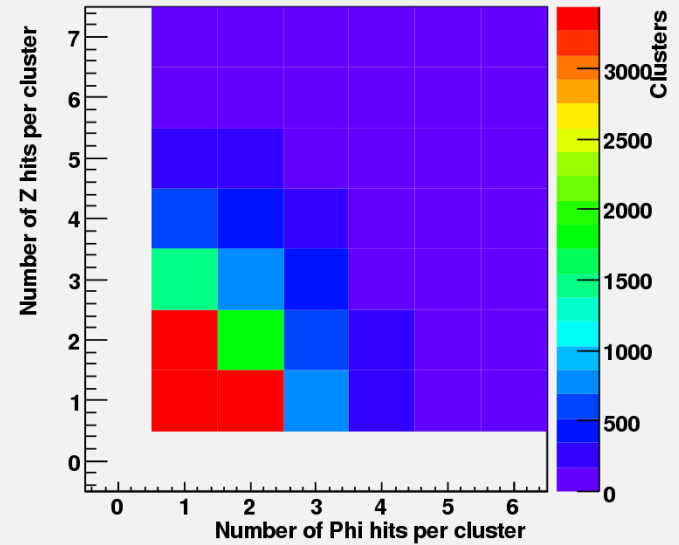
out_spread	
Entries	68787
Mean x	100.1
Mean y	127.3
RMS x	57.47
RMS y	73.18

About optimization: 69k hits → ~58k words
Zone compression factor ~ 15%

Matrix Orientation

Z axis

Cluster SVTHit Z/Phi Multiplicity2 on Svt Layer 0



256x200 pixel matrix

Submatrix 4

Submatrix 3

Submatrix 2

Submatrix 1

Zones

Readout

Phi axis

Matrix Interface

--CHIP TOP Entity

CHIP I/O PADS

--READOUT CORE Entity

```

reset      : in  std_logic;
RDclk      : in  std_logic;
fast_clk   : in  std_logic;
BC_clk     : in  std_logic;
--DATA output
data_out    : out std_logic_vector(19 downto 0);
data_valid  : out std_logic;
--Slow Control interface
SDA         : inout std_logic;
SCL         : in  std_logic;
chip_addr   : in  std_logic_vector(2 downto 0);
--Matrix external controls
ML_ena      : in  std_logic;
GlobalFastOR : out std_logic;
--Matrix interface
ColReadEna_b : out std_logic_vector(MAT_X_SIZE-1 downto 0);
LatchEna_b   : out std_logic_vector(MAT_X_SIZE-1 downto 0);
Mask_Write_b : out std_logic_vector(MAT_Y_SIZE-1 downto 0);
MaskColSel_b : out std_logic_vector(MAT_X_SIZE-1 downto 0);
TSCNT        : out std_logic_vector(TS_WIDTH-1 downto 0);
TSREQ        : out std_logic_vector(N_XSUBMAT*TS_WIDTH-1 downto 0);
FastOr       : in  std_logic_vector(MAT_X_SIZE-1 downto 0);
PIX_DATA_M0  : in  std_logic_vector(SUBMAT_Y_SIZE-1 downto 0);
PIX_DATA_M1  : in  std_logic_vector(SUBMAT_Y_SIZE-1 downto 0);
PIX_DATA_M2  : in  std_logic_vector(SUBMAT_Y_SIZE-1 downto 0);
PIX_DATA_M3  : in  std_logic_vector(SUBMAT_Y_SIZE-1 downto 0);

```

--MATRIX Entity

```

ColReadEna_b : in  std_logic_vector(MAT_X_SIZE-1 downto 0);
LatchEna_b   : in  std_logic_vector(MAT_X_SIZE-1 downto 0);
Mask_Write_b : in  std_logic_vector(MAT_Y_SIZE-1 downto 0);
MaskColSel_b : in  std_logic_vector(MAT_X_SIZE-1 downto 0);
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PIX_DATA_M2  : out std_logic_vector(SUBMAT_Y_SIZE-1 downto 0);
PIX_DATA_M3  : out std_logic_vector(SUBMAT_Y_SIZE-1 downto 0);

```

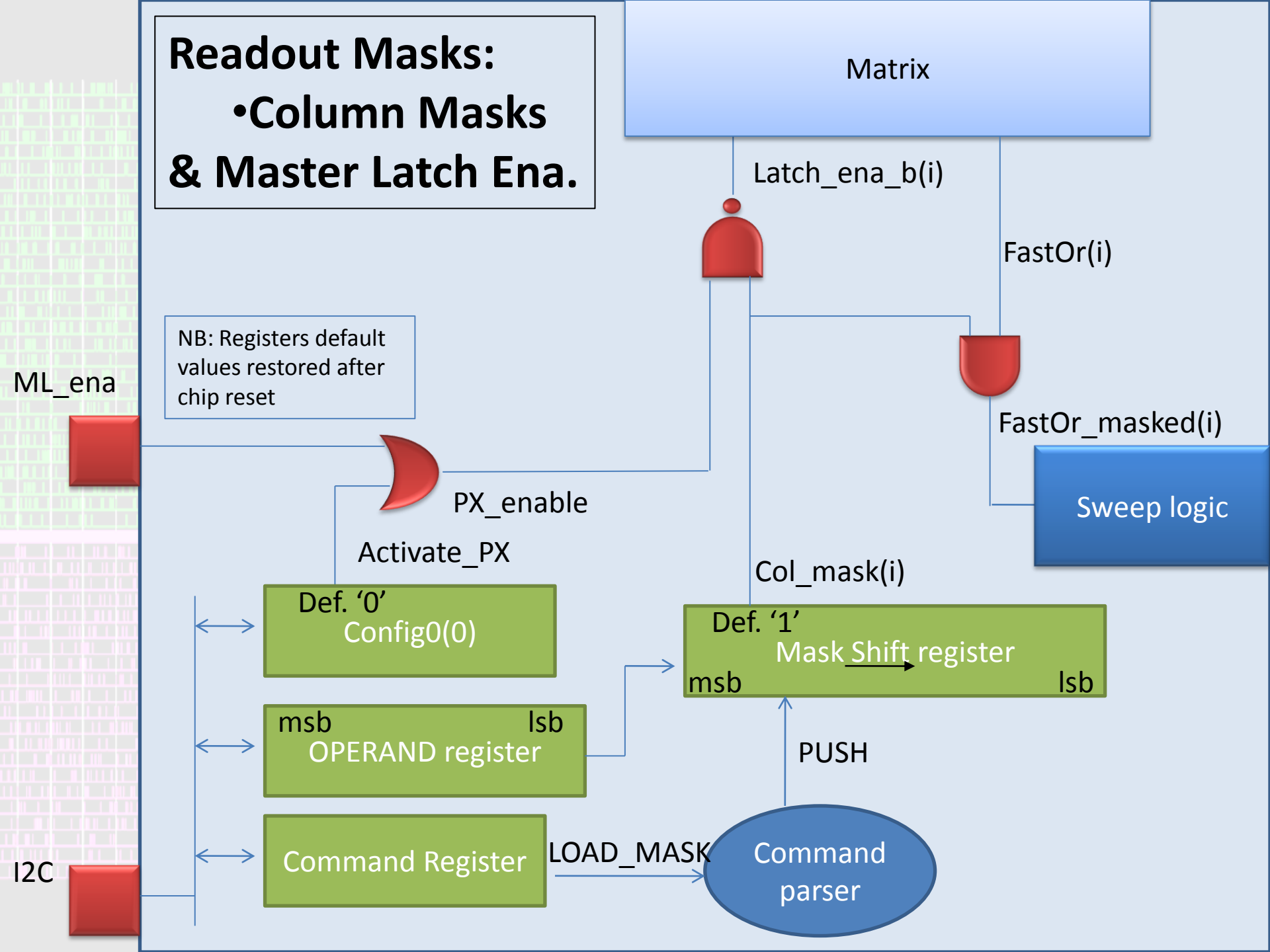


Readout Masks:

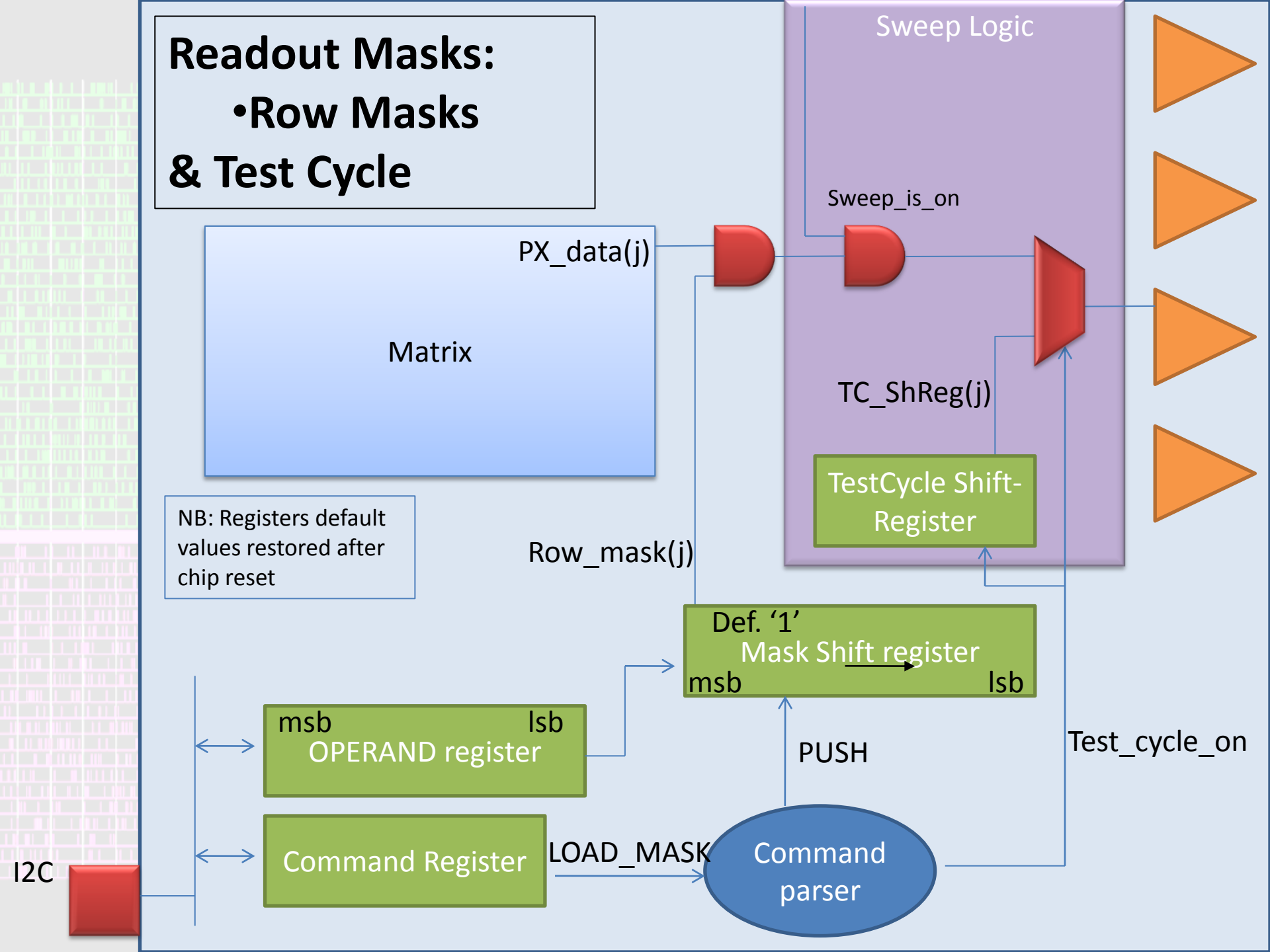
- Column Masks

& Master Latch Ena.

NB: Registers default values restored after chip reset



Readout Masks: •Row Masks & Test Cycle

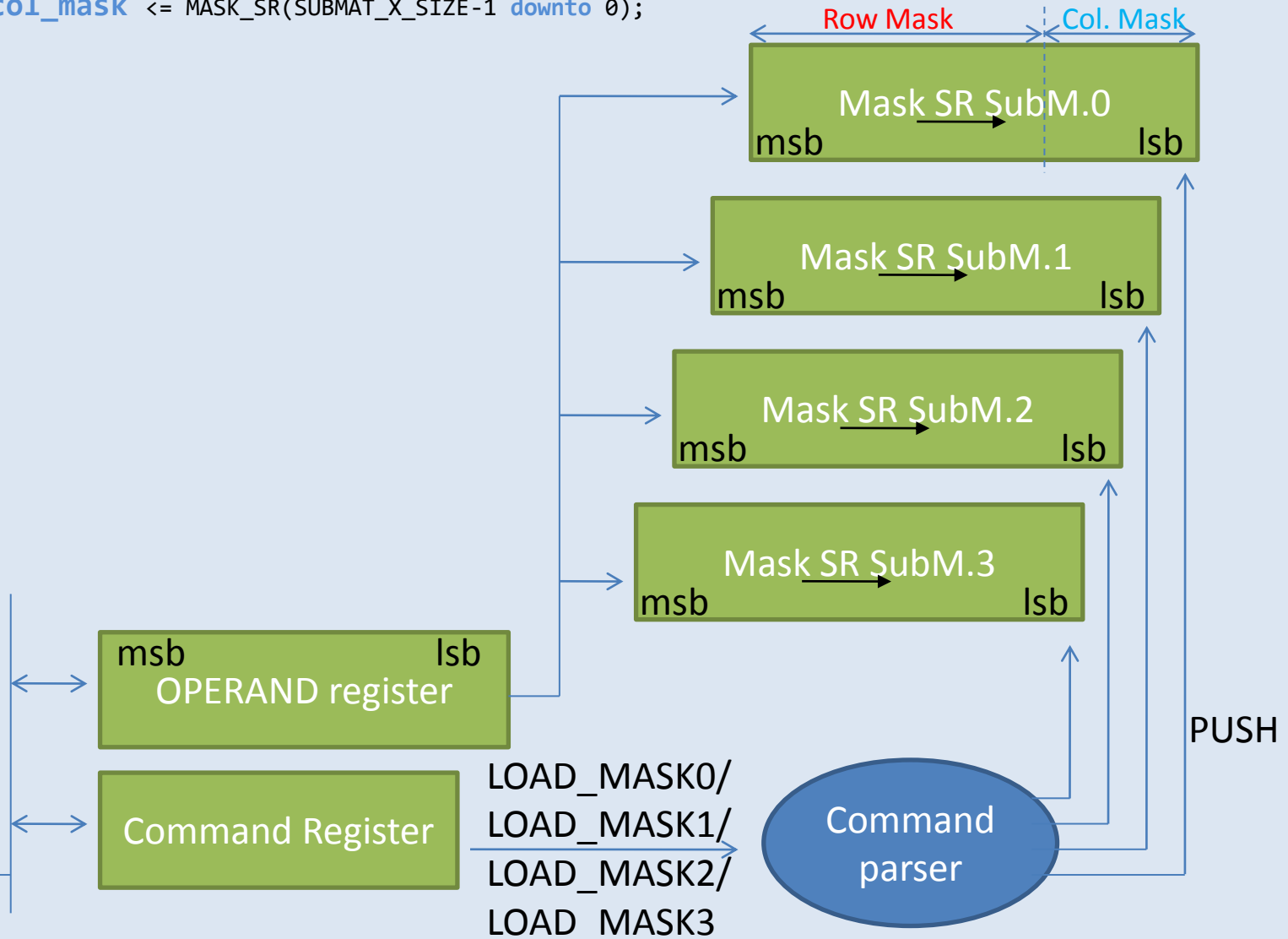


Readout Masks:

•Details of Mask Shift Registers

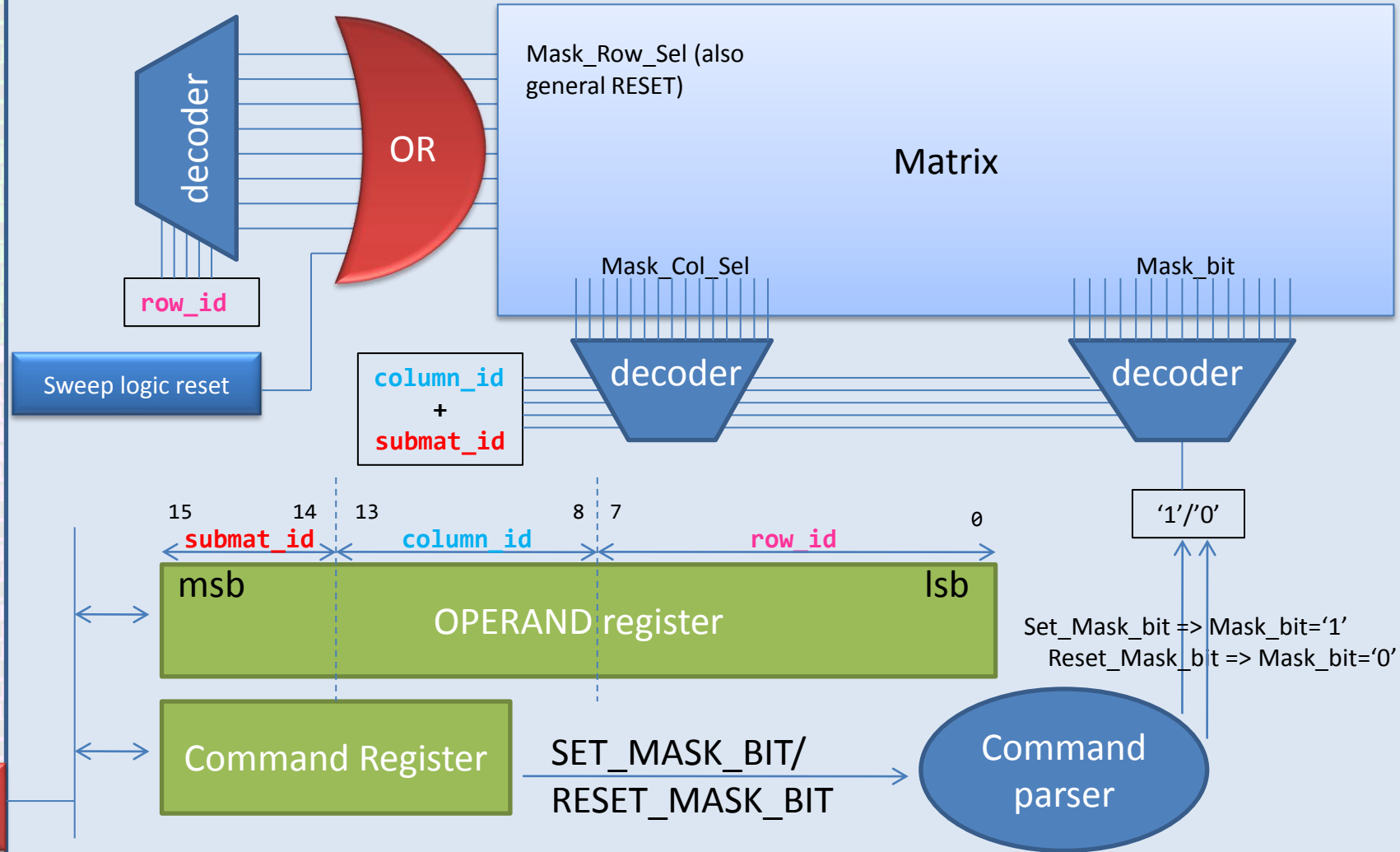
```
row_mask <= MASK_SR(SUBMAT_X_SIZE+SUBMAT_Y_SIZE-1 downto SUBMAT_X_SIZE);
```

```
col_mask <= MASK_SR(SUBMAT_X_SIZE-1 downto 0);
```



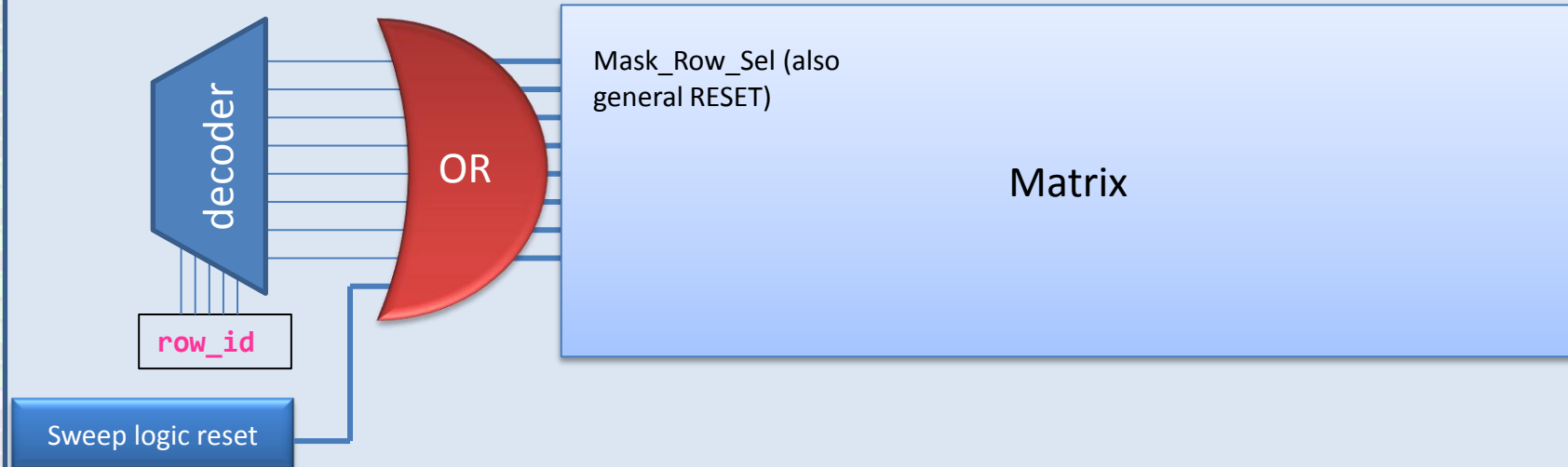
Matrix Masks & Matrix resets

```
submat_id <= OPERAND(15 downto 14);  
column_id <= OPERAND(13 downto 8);  
row_id <= OPERAND(7 downto 0);
```



Matrix Masks & Matrix resets

```
submat_id <= OPERAND(15 downto 14);  
column_id <= OPERAND(13 downto 8);  
row_id <= OPERAND(7 downto 0);
```



When reset goes low, the general matrix reset is kept active for a certain amount of time.
How long?

Readout Registers

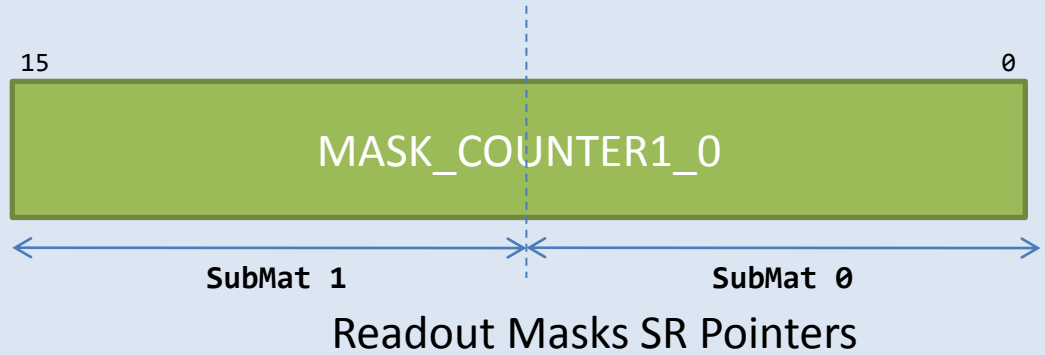
16-bit registers, 16 RO & 16 R/W registers

-- READ ONLY REGISTERS

1. MSK_COUNTER1_0
2. MSK_COUNTER3_2
3. ERROR_FLAGS
4. HIT_RATE
5. BCLOST_COUNT0
6. BCLOST_COUNT1
7. BCLOST_COUNT2
8. BCLOST_COUNT3
9. B1_FILL_LEVEL0
10. B1_FILL_LEVEL1
11. B1_FILL_LEVEL2
12. B1_FILL_LEVEL3
13. B1_MEAN_FILL0
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-- READ/WRITE REGISTERS

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4. CONFIG_1
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6. TRIG_LATENCY*
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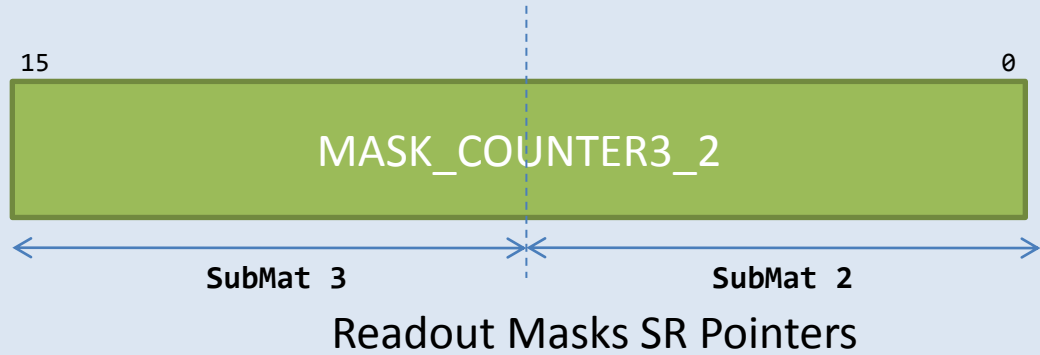
Increment +1 on each LOAD_MASK operation

Readout Registers

16-bit registers, 16 RO & 16 R/W registers

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Increment +1 on each LOAD_MASK operation

-- READ/WRITE REGISTERS

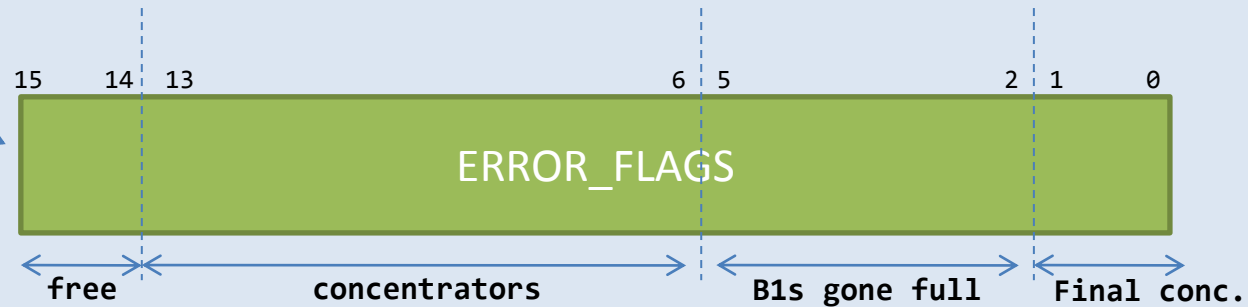
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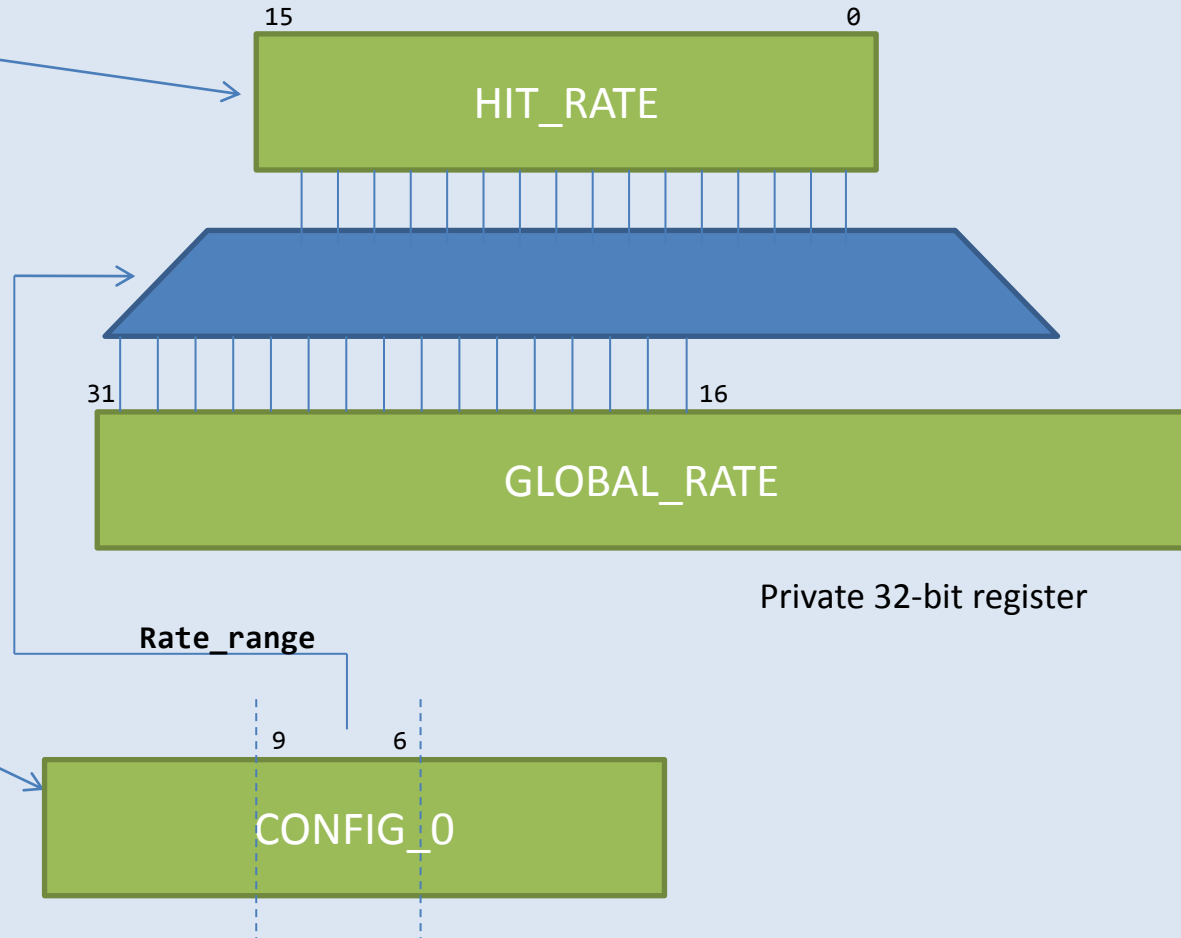
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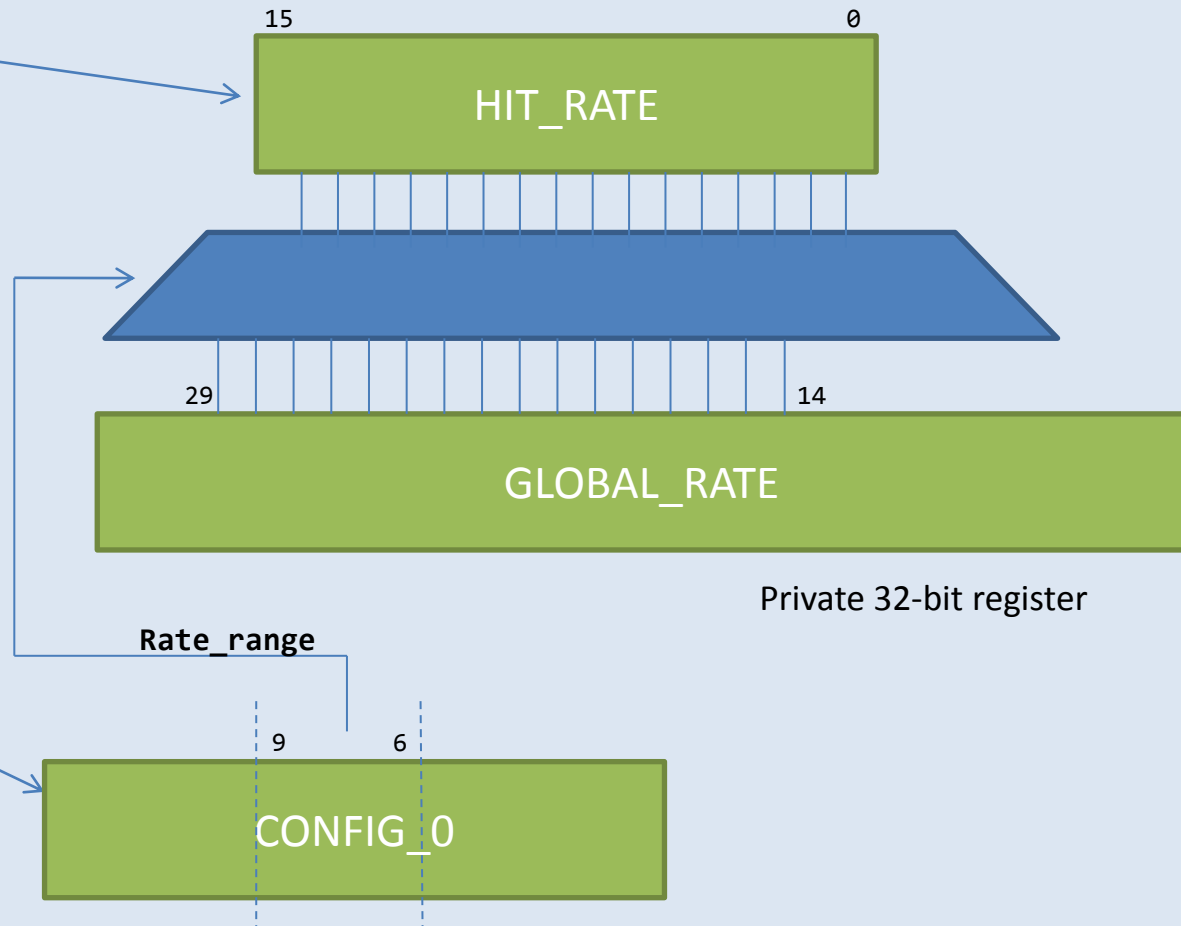
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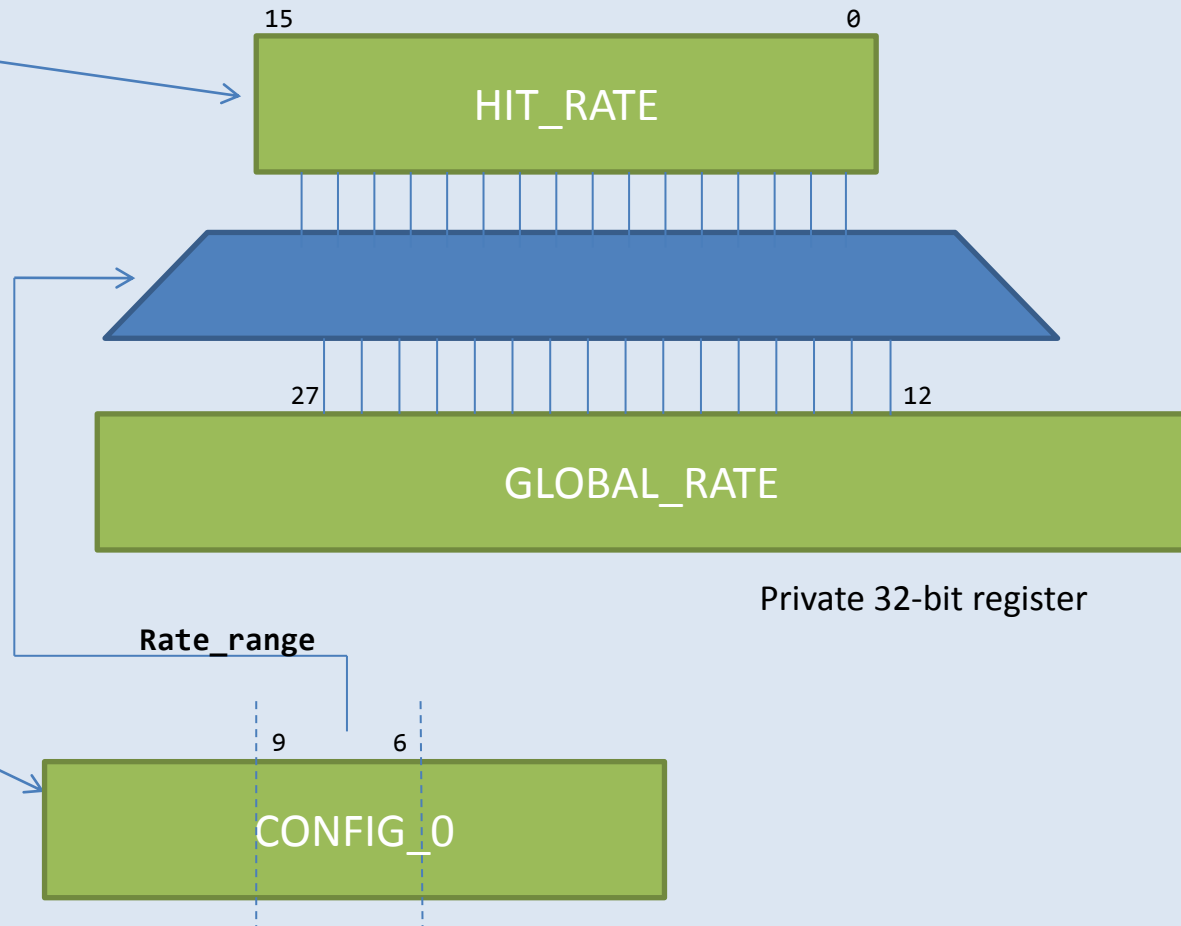
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Readout Registers

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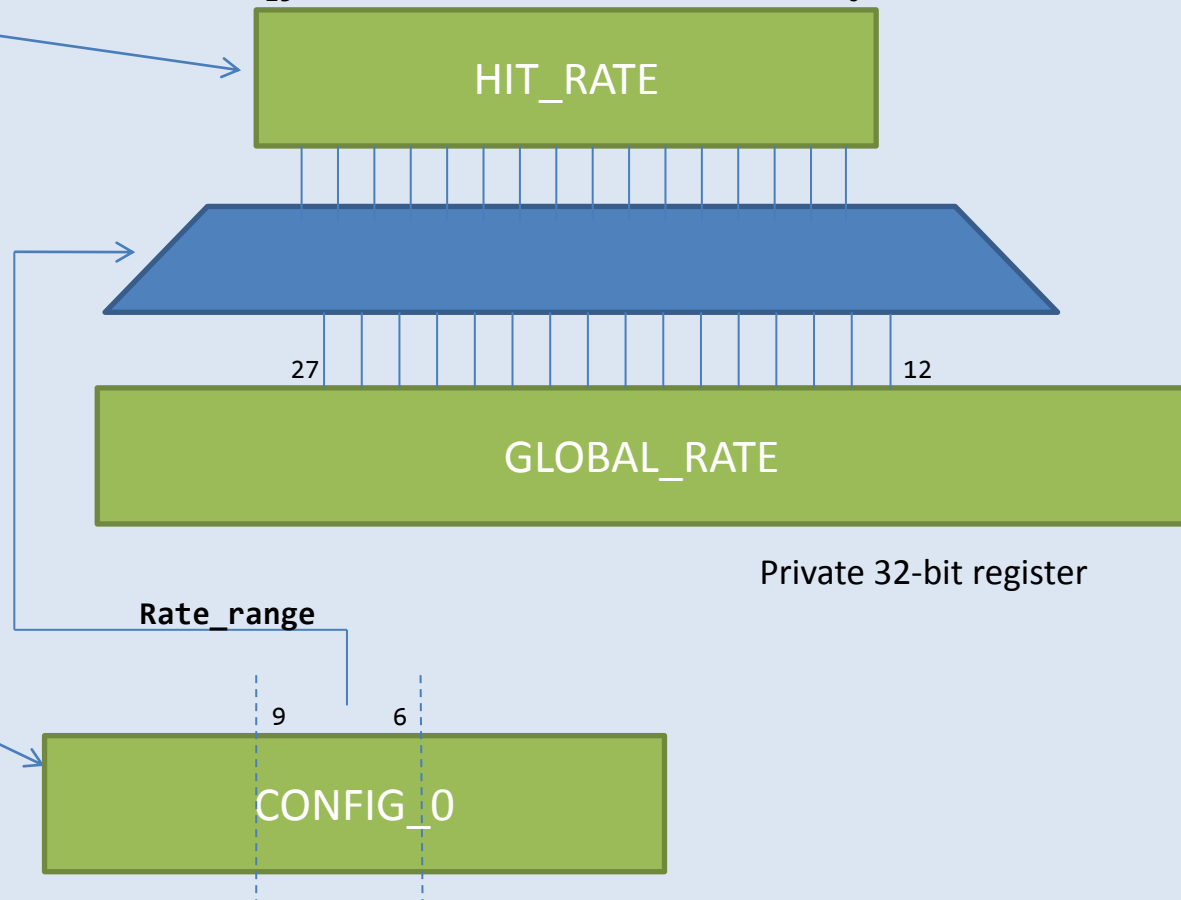
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Unsigned, expressed in:
 $\text{counts} / (5 \cdot 2^{16} \cdot T_{RDclk} / \text{SUBMAT_Y_SIZE})$



Readout Registers

16-bit registers, 16 RO & 16 R/W registers

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} Unused in SQUARE Architecture

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Unsigned, represents the current used memory in B1n



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16. ...

15

0

COMMAND_REGISTER

--COMMAND LIST

NO_CMD(default)	:= x"0000";
LOAD_MASK0	:= x"0002";
LOAD_MASK1	:= x"1002";
LOAD_MASK2	:= x"2002";
LOAD_MASK3	:= x"3002";
RESET_TIME_COUNTER	:= x"0003";
CYCLE_TEST	:= x"0004";
SET_MASK_BIT	:= x"0005";
RESET_MASK_BIT	:= x"0006";

Readout Registers

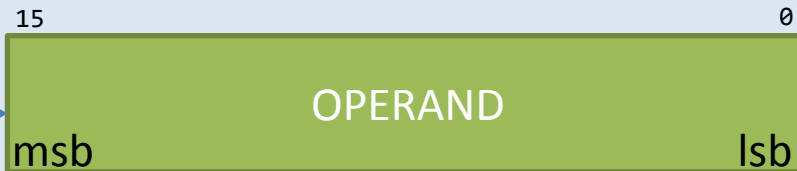
16-bit registers, 16 RO & 16 R/W registers

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Readout Registers

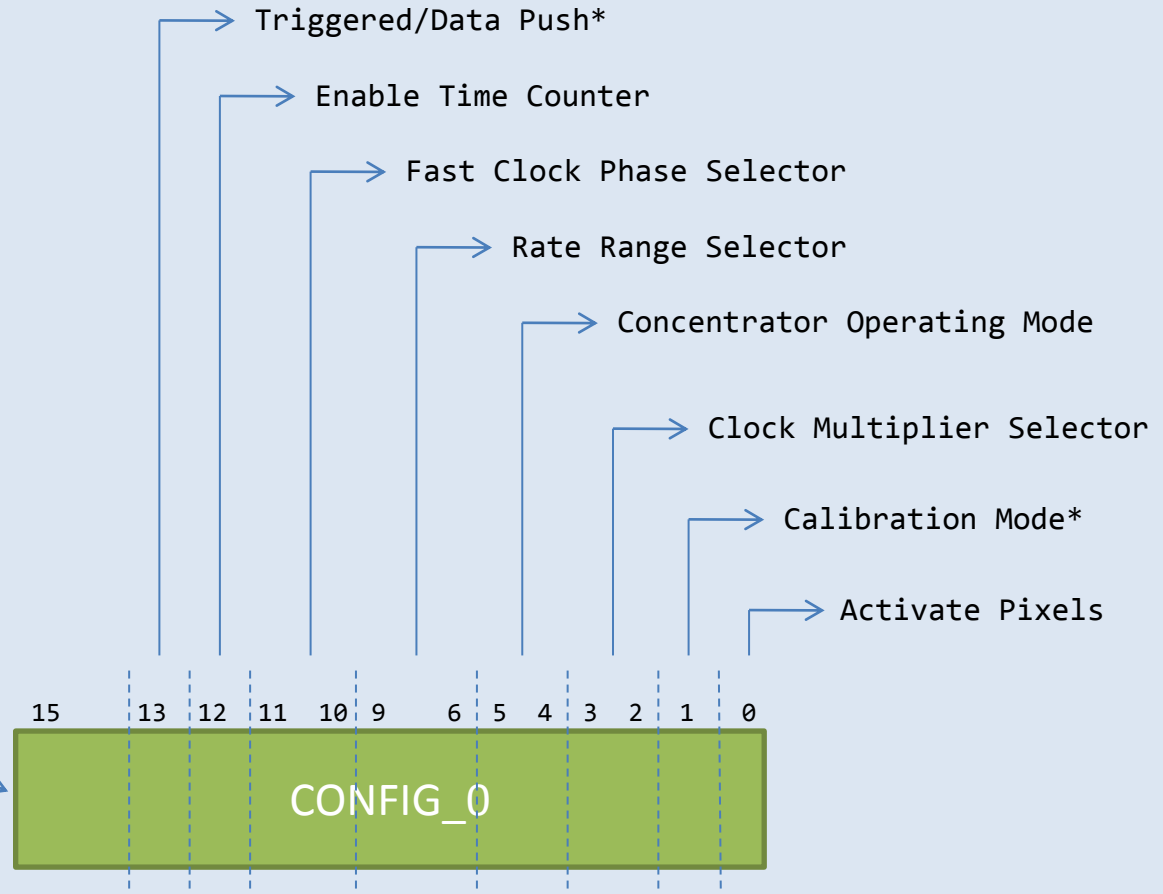
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6. BCLOST_COUNT1
7. BCLOST_COUNT2
8. BCLOST_COUNT3
9. B1_FILL_LEVEL0
10. B1_FILL_LEVEL1
11. B1_FILL_LEVEL2
12. B1_FILL_LEVEL3
13. B1_MEAN_FILL0
14. B1_MEAN_FILL1
15. B1_MEAN_FILL2
16. B1_MEAN_FILL3

-- READ/WRITE REGISTERS

1. COMMAND_REGISTER
2. OPERAND
3. CONFIG_0
4. CONFIG_1
5. FLUSH_TIMEOUT
6. TRIG_LATENCY*
7. ...
8. ...
9. ...
10. ...
11. ...
12. ...
13. ...
14. ...
15. ...
16. ...

→ Unused in SQUARE Architecture

Readout Registers

16-bit registers, 16 RO & 16 R/W registers

-- READ ONLY REGISTERS

1. MSK_COUNTER1_0
2. MSK_COUNTER3_2
3. ERROR_FLAGS
4. HIT_RATE
5. BCLOST_COUNT0
6. BCLOST_COUNT1
7. BCLOST_COUNT2
8. BCLOST_COUNT3
9. B1_FILL_LEVEL0
10. B1_FILL_LEVEL1
11. B1_FILL_LEVEL2
12. B1_FILL_LEVEL3
13. B1_MEAN_FILL0
14. B1_MEAN_FILL1
15. B1_MEAN_FILL2
16. B1_MEAN_FILL3

-- READ/WRITE REGISTERS

1. COMMAND_REGISTER
2. OPERAND
3. CONFIG_0
4. CONFIG_1
5. FLUSH_TIMEOUT
6. TRIG_LATENCY*
7. ...
8. ...
9. ...
10. ...
11. ...
12. ...
13. ...
14. ...
15. ...
16. ...

→ Concentrator Time Out before Flush Data
Def. 256 (x"0100")
Expressed in fast clock periods

Readout Registers

16-bit registers, 16 RO & 16 R/W registers

-- READ ONLY REGISTERS

1. MSK_COUNTER1_0
2. MSK_COUNTER3_2
3. ERROR_FLAGS
4. HIT_RATE
5. BCLOST_COUNT0
6. BCLOST_COUNT1
7. BCLOST_COUNT2
8. BCLOST_COUNT3
9. B1_FILL_LEVEL0
10. B1_FILL_LEVEL1
11. B1_FILL_LEVEL2
12. B1_FILL_LEVEL3
13. B1_MEAN_FILL0
14. B1_MEAN_FILL1
15. B1_MEAN_FILL2
16. B1_MEAN_FILL3

-- READ/WRITE REGISTERS

1. COMMAND_REGISTER
2. OPERAND
3. CONFIG_0
4. CONFIG_1
5. FLUSH_TIMEOUT
6. TRIG_LATENCY*
7. ...
8. ...
9. ...
10. ...
11. ...
12. ...
13. ...
14. ...
15. ...
16. ...

Unused in SQUARE Architecture

TO DO:

verify that **EACH** required/requested/desiderata operation on chip is affordable with the presented logic.

- Calibrations..
- tests, (ML_ena, resets, mask...)
- ...