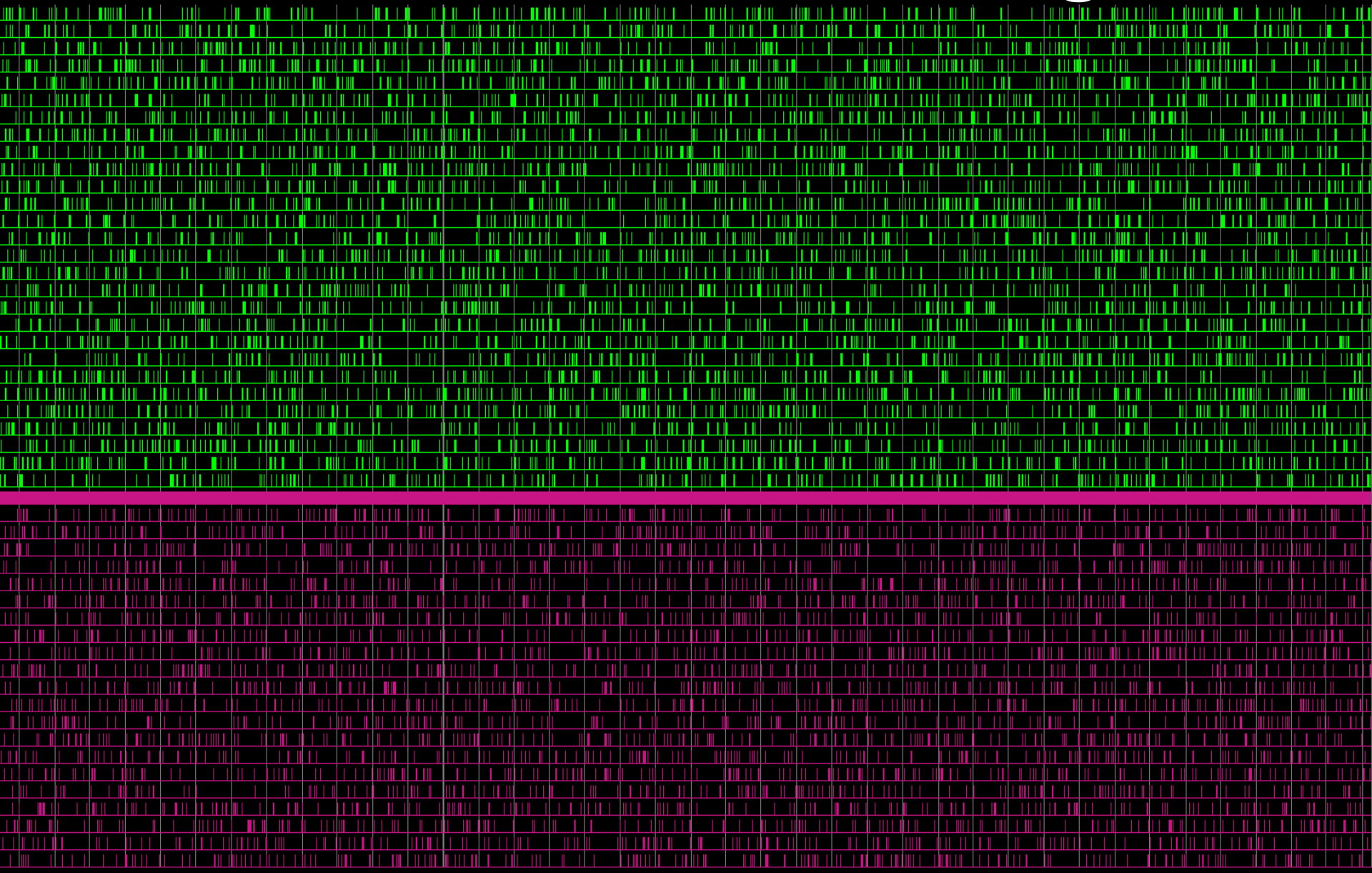
Simulation Meeting



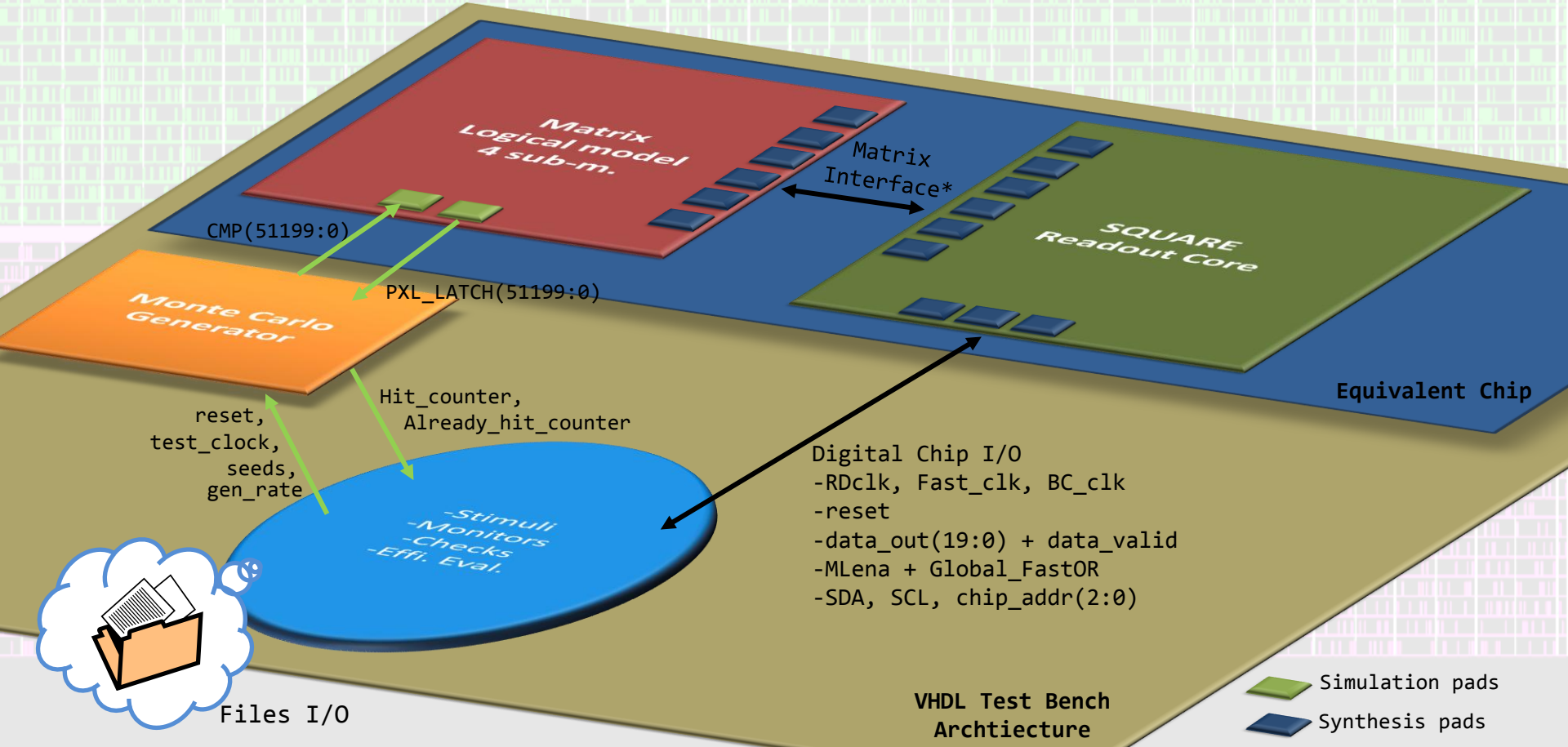
24-09-2010 F.M.Giorgi

Summary

- Simulation Environment
- Physical Events Simulations
- Matrix Interface
- Masks, Reset, Registers & Configurations

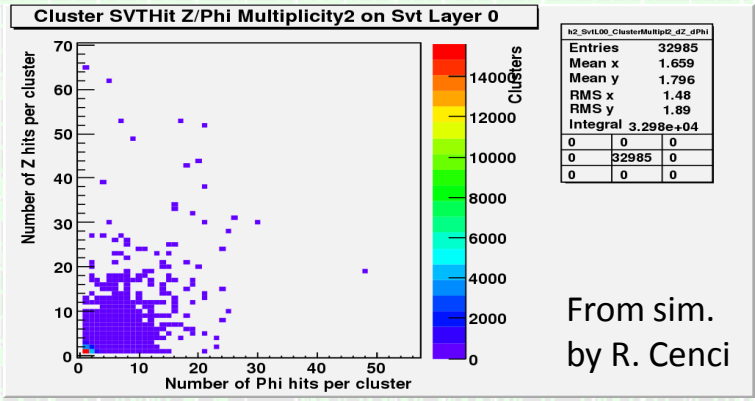
Simulation Environment

- Simulation Tool: **Modelsim SE 6.3f**
- Simulation components
  - **Readout Core Arch. SQUARE** (.vhd synthesizable code)
  - **Monte Carlo Generator** (.vhd NOT synthesizable code)
  - **Matrix Behavioral Model** (.vhd code)
  - **Test Bench** (.vhd code)



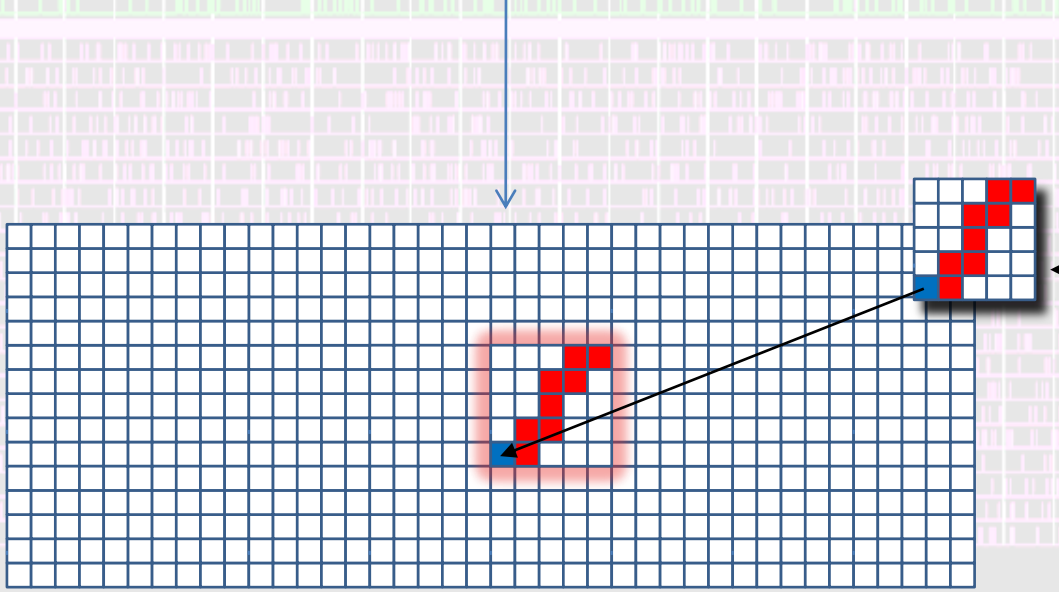
Physical Events Simulation

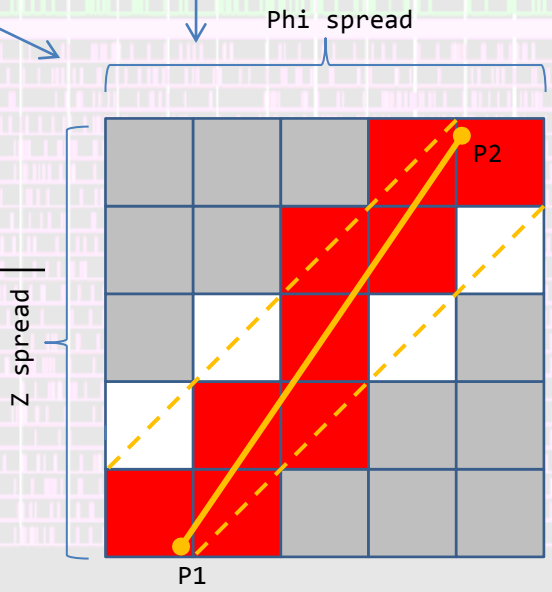
- Monte Carlo generator
  - Stand Alone version (independent from Matrix logical model)
  - Generation of clustered events
  - Knobs: 
    - Cluster dispersion distribution in (z,phi)
    - Physical time resolution (test_clock), hit/miss thresholds =Global hit rate
  - Arbitrary pattern extraction by geometrical rules
  - Pattern check (grey pixels are forbidden)
  - Pattern application to a random pixel of the matrix



From sim. by R. Cenci

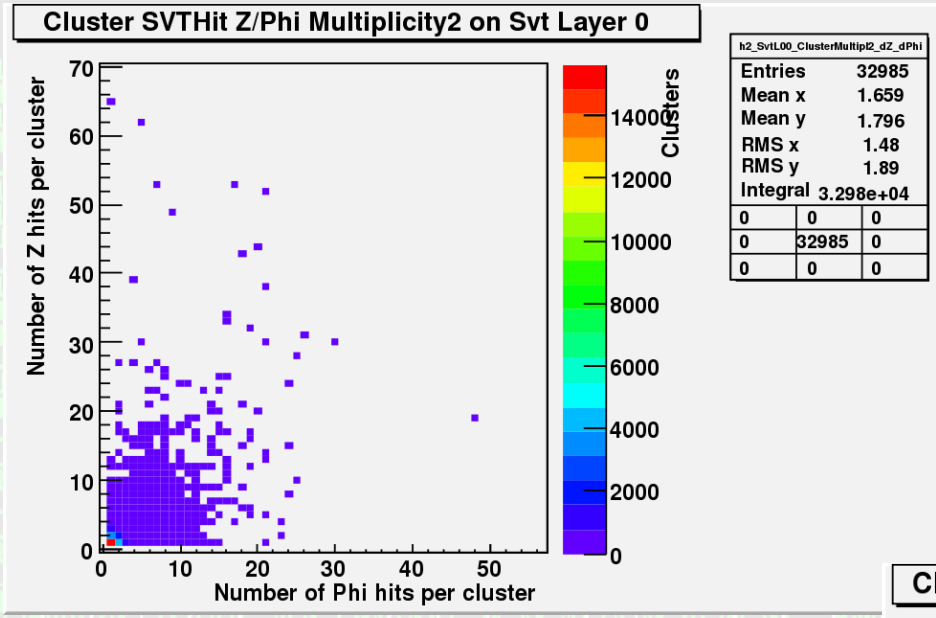
Cluster spread extraction Es. (5,5)





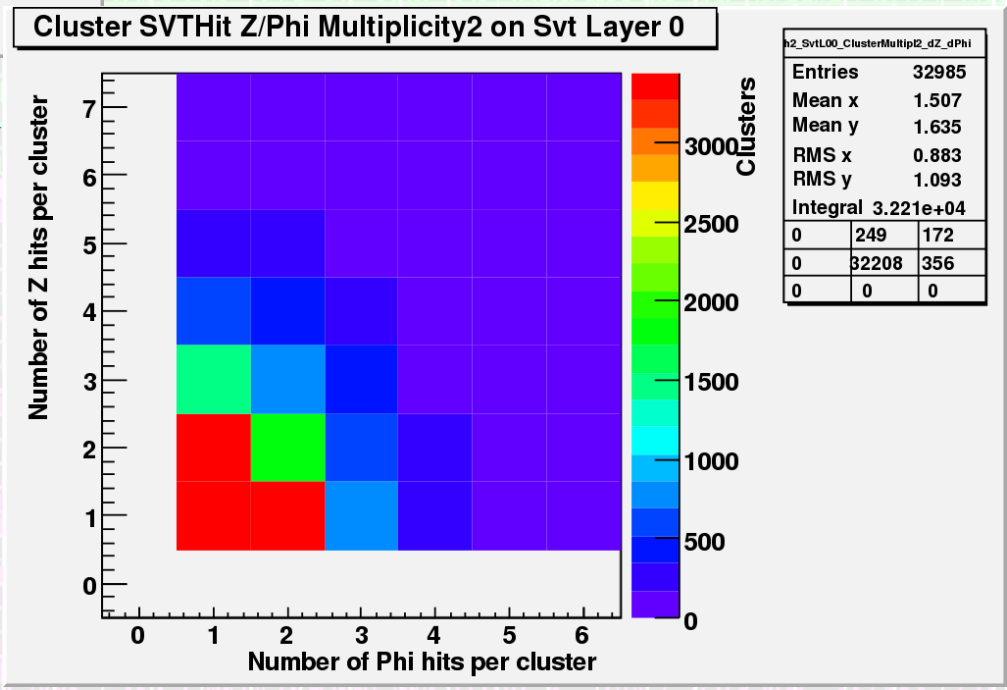
Cluster Pattern Extraction

Implemented cluster spread distribution zeta/phi from physics simulations (by R.Cenci)

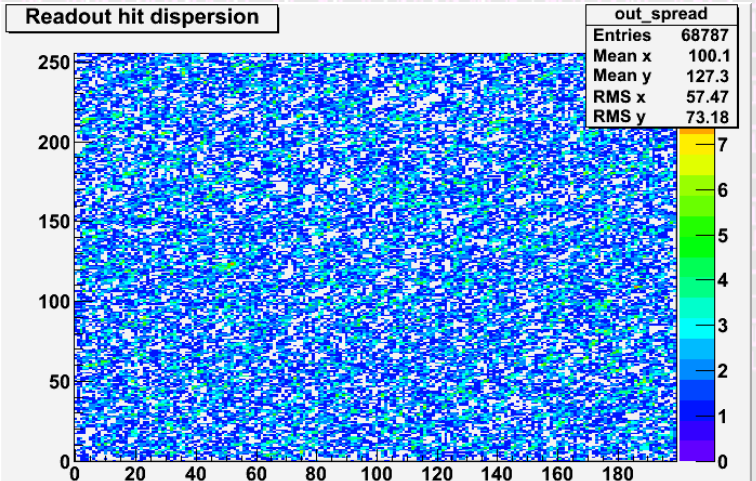


%	1	2	3	4	phi
1	47,27520	12,65198	2,46868	0,70666	…
2	10,62458	5,80757	1,76511	0,55545	
3	4,31710	2,30513	1,06770	0,40116	
4	2,00580	1,15102	0,57397	0,26538	
zeta	…				

Zoom/Equalize



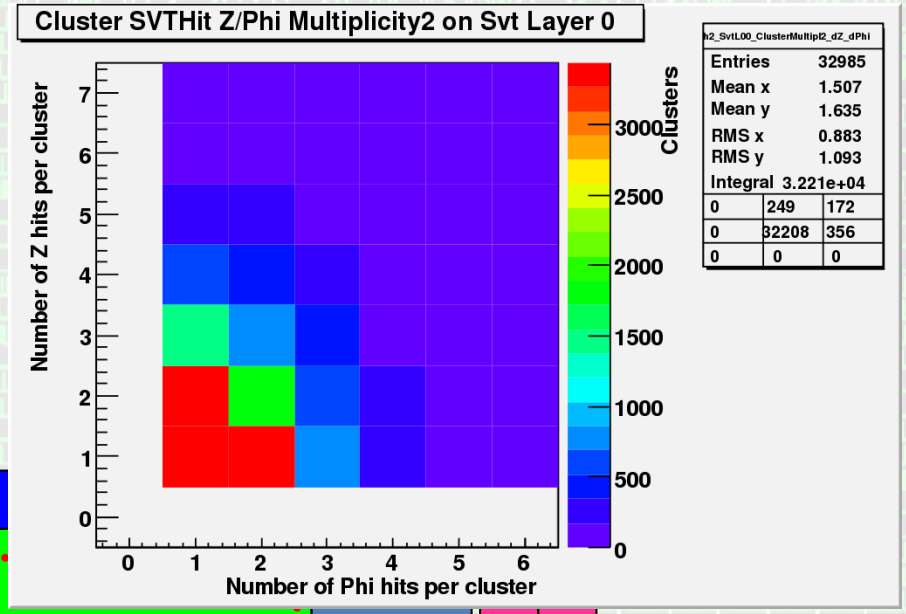
Implemented and simulated



About optimization: 69k hits → ~58k words

Zone compression factor ~ 15%

Matrix Orientation



Z axis

256x200 pixel matrix

Submatrix 4

Submatrix 3

Submatrix 2

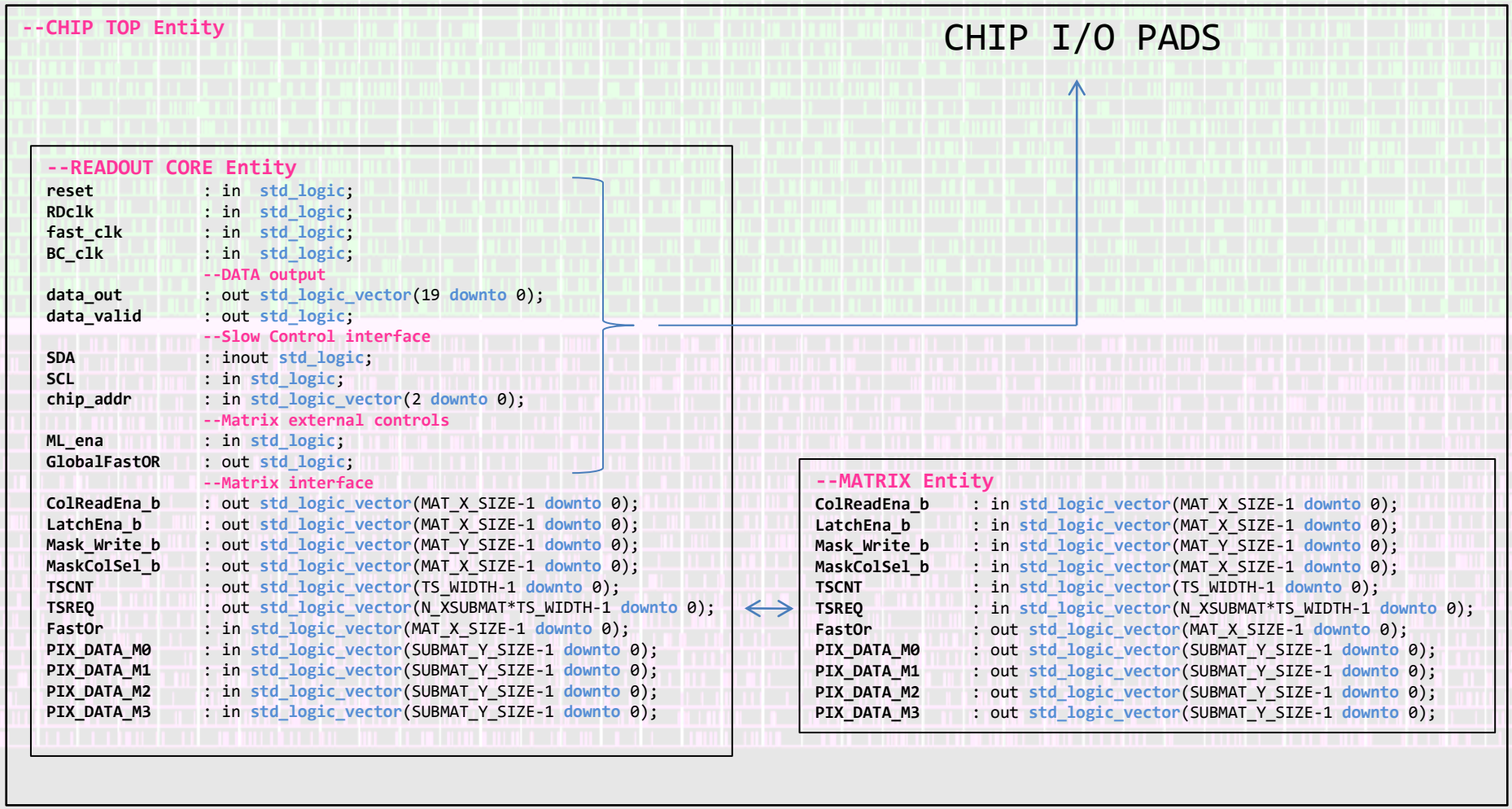
Zones

Submatrix 1

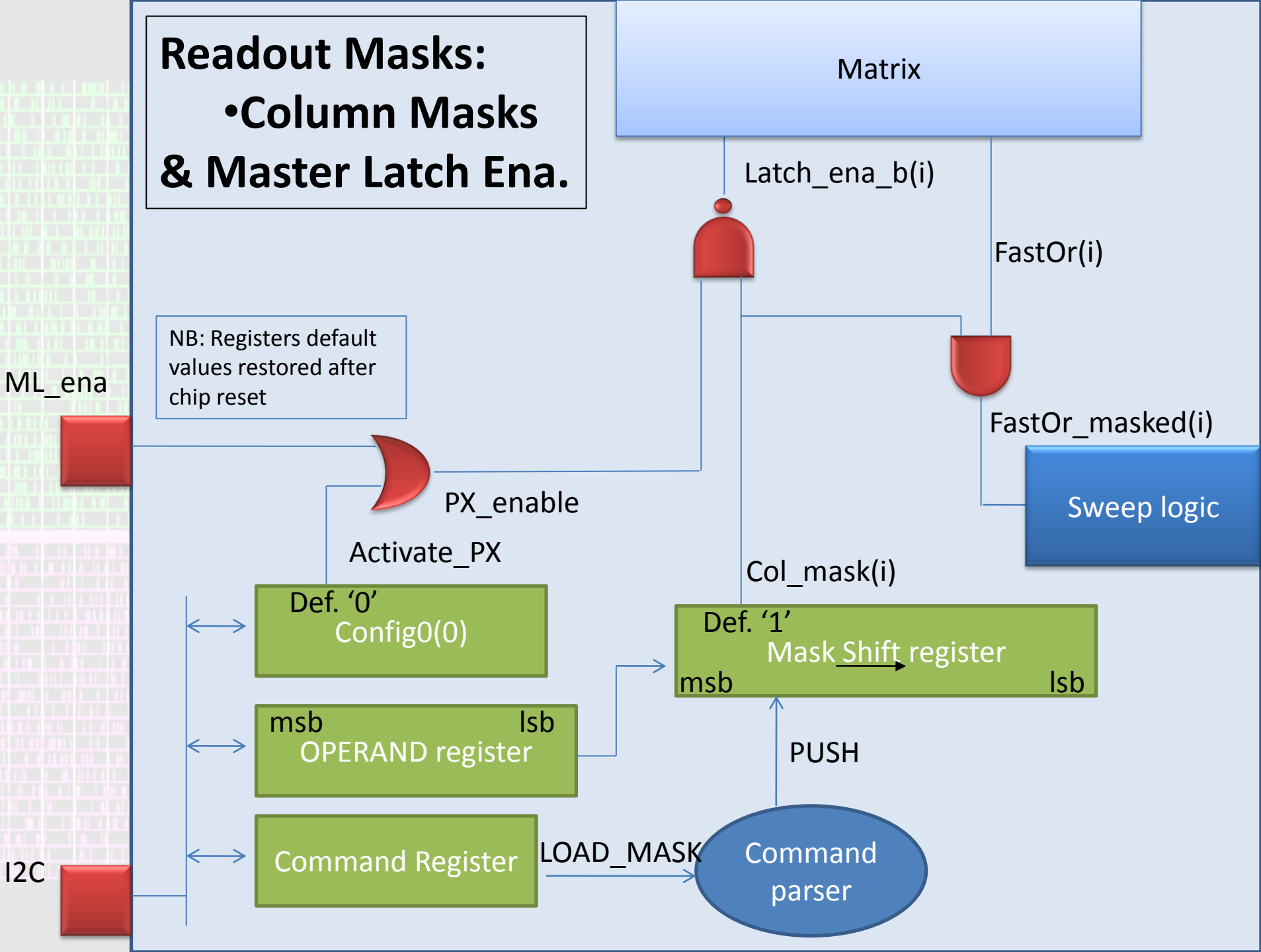
Readout

Phi axis

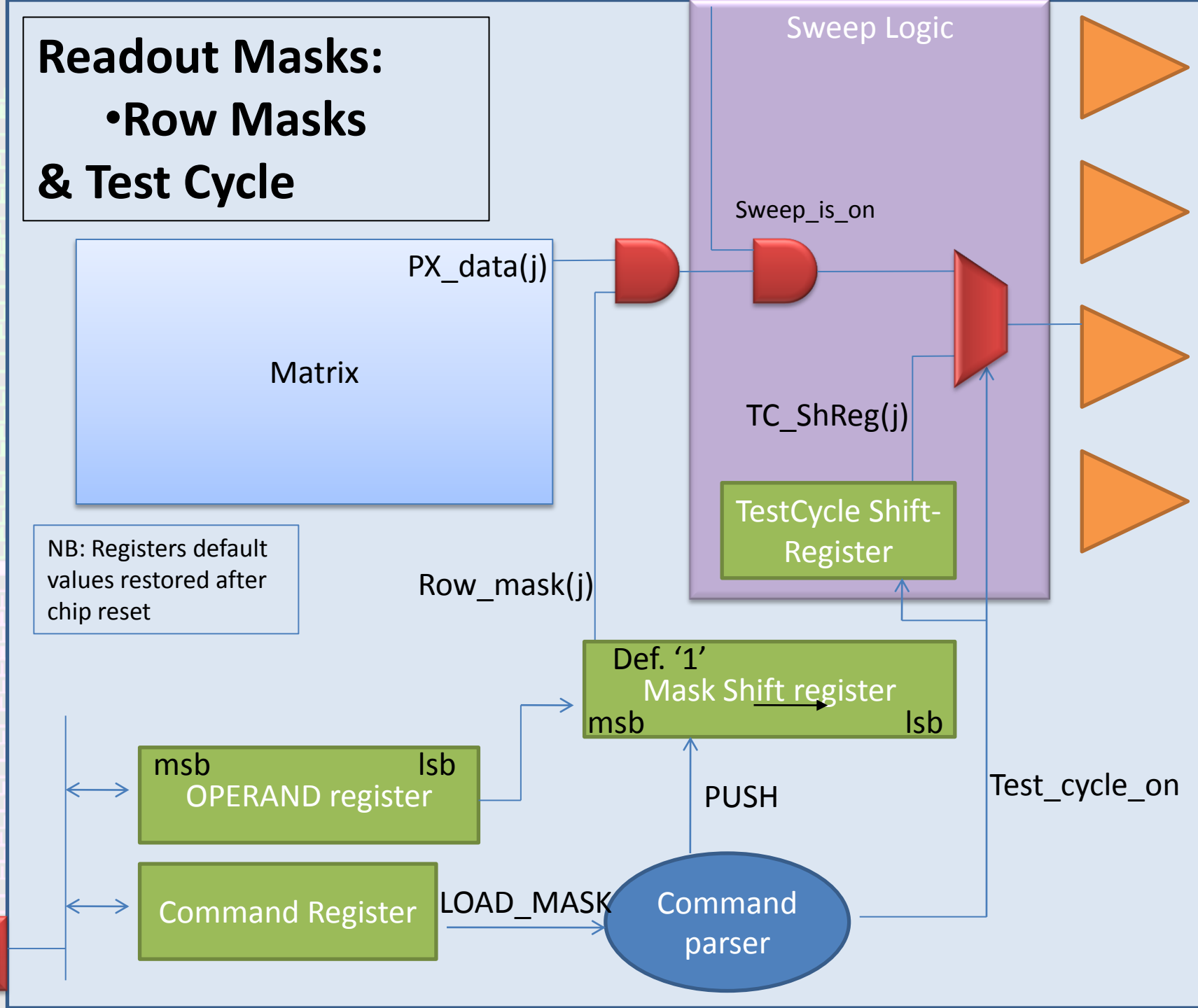
Matrix Interface



Readout Masks:
•Column Masks
& Master Latch Ena.



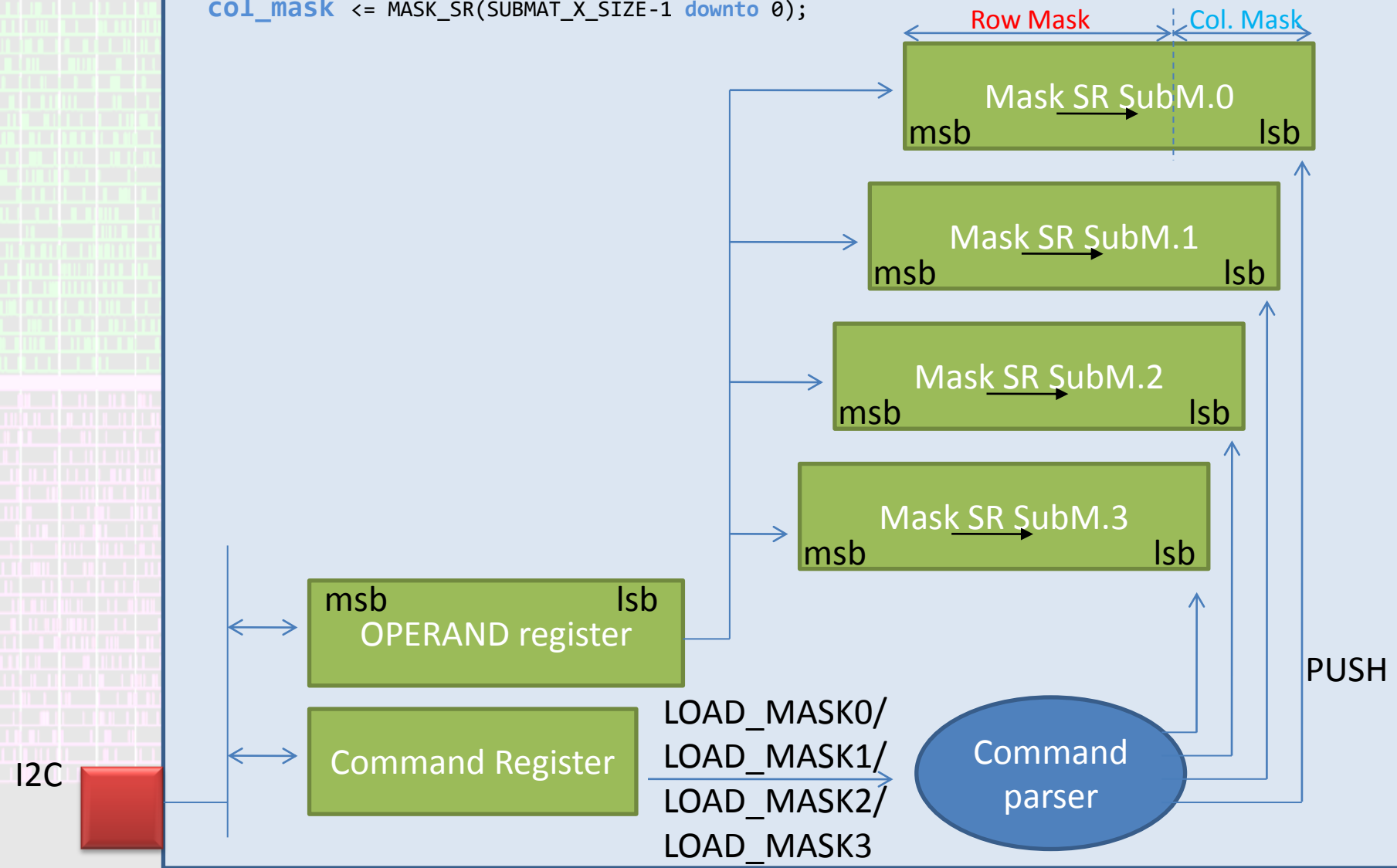
Readout Masks:
•Row Masks
& Test Cycle



Readout Masks:

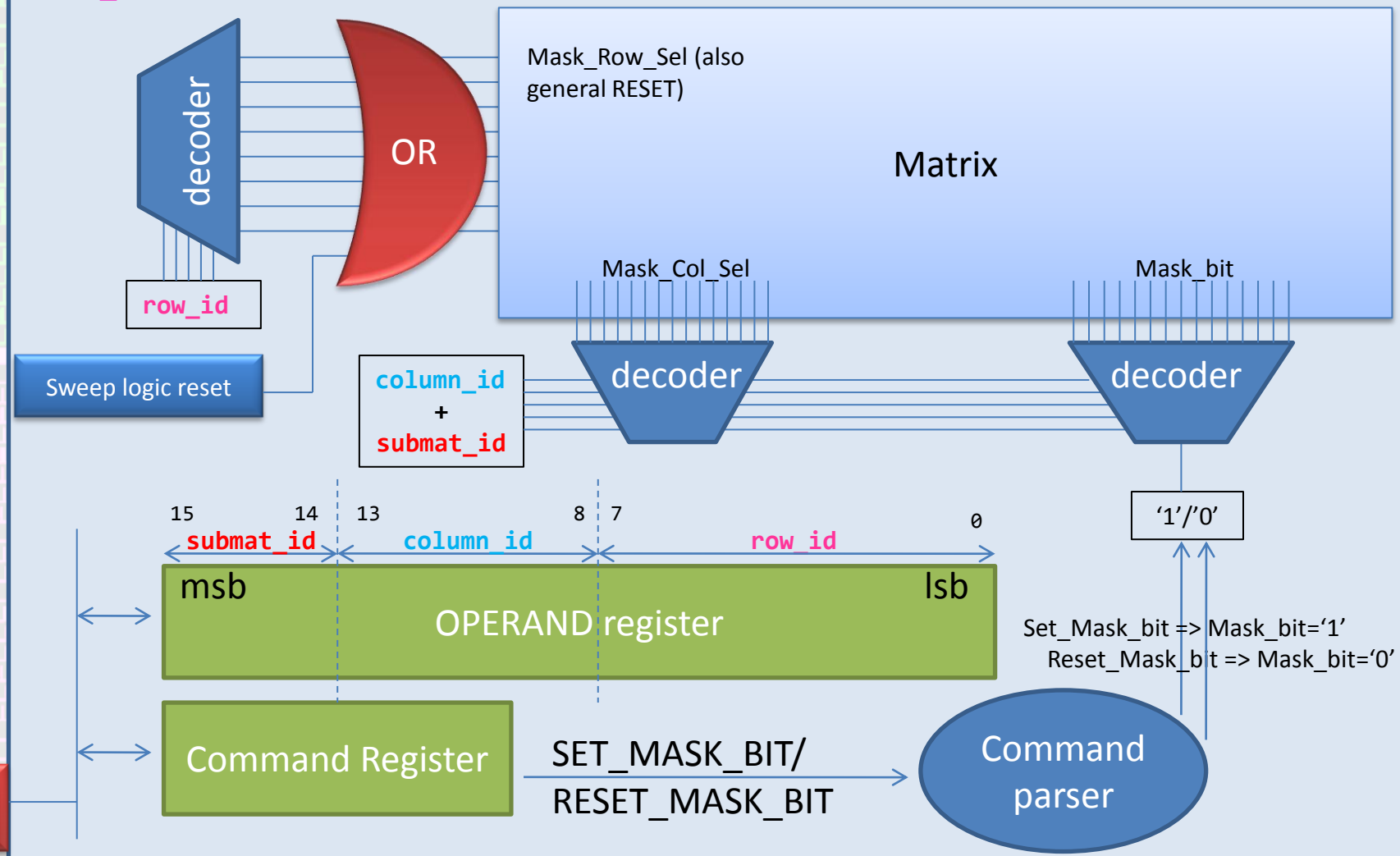
•Details of Mask Shift Registers

```
row_mask <= MASK_SR(SUBMAT_X_SIZE+SUBMAT_Y_SIZE-1 downto SUBMAT_X_SIZE);
col_mask <= MASK_SR(SUBMAT_X_SIZE-1 downto 0);
```



Matrix Masks & Matrix resets

```
submat_id  <= OPERAND(15 downto 14);
column_id  <= OPERAND(13 downto 8);
row_id     <= OPERAND(7 downto 0);
```



Matrix Masks & Matrix resets

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column_id <= OPERAND(13 downto 8);
row_id    <= OPERAND(7 downto 0);
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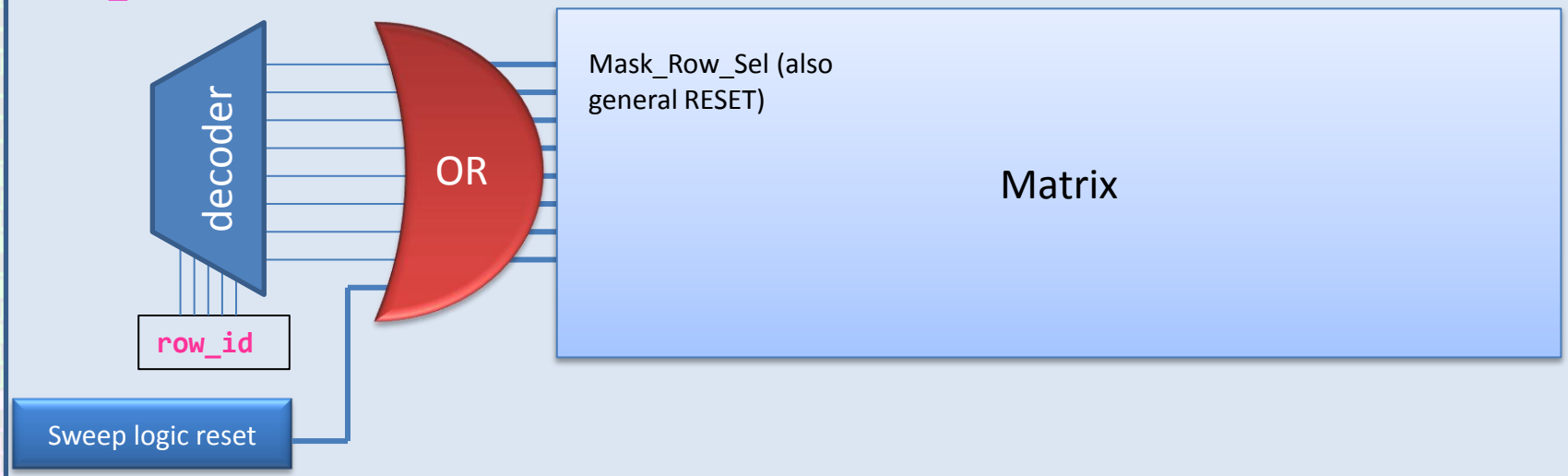

When reset goes low, the general matrix reset is kept active for a certain amount of time.
How long?

Readout Registers

16-bit registers, 16 RO & 16 R/W registers

```
-- READ ONLY REGISTERS
1. MSK_COUNTER1_0
2. MSK_COUNTER3_2
3. ERROR_FLAGS
4. HIT_RATE
5. BCLOST_COUNT0
6. BCLOST_COUNT1
7. BCLOST_COUNT2
8. BCLOST_COUNT3
9. B1_FILL_LEVEL0
10.B1_FILL_LEVEL1
11.B1_FILL_LEVEL2
12.B1_FILL_LEVEL3
13.B1_MEAN_FILL0
14.B1_MEAN_FILL1
15.B1_MEAN_FILL2
16.B1_MEAN_FILL3

-- READ/WRITE REGISTERS
1. COMMAND_REGISTER
2. OPERAND
3. CONFIG_0
4. CONFIG_1
5. FLUSH_TIMEOUT
6. TRIG LATENCY*
7. …
8. …
9. …
10.…
11.…
12.…
13.…
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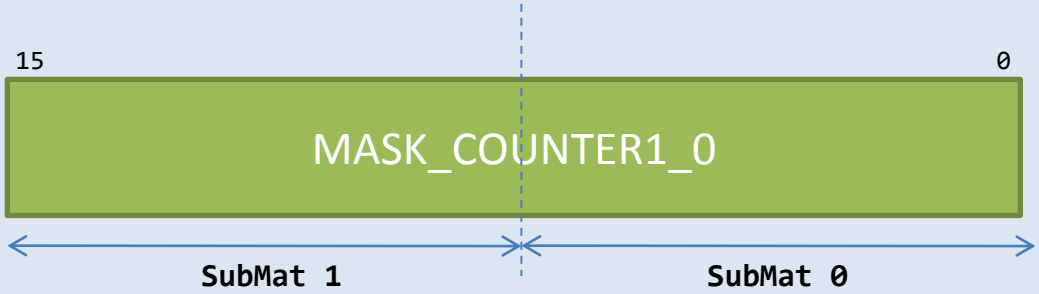
15.…
16.…
```



Readout Masks SR Pointers

Increment +1 on each LOAD_MASK operation

Readout Registers

16-bit registers, 16 RO & 16 R/W registers

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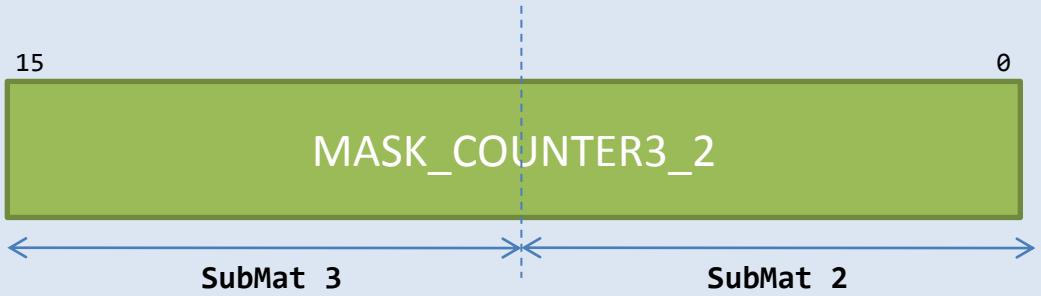
```



Readout Masks SR Pointers

Increment +1 on each LOAD_MASK operation

Readout Registers

16-bit registers, 16 RO & 16 R/W registers

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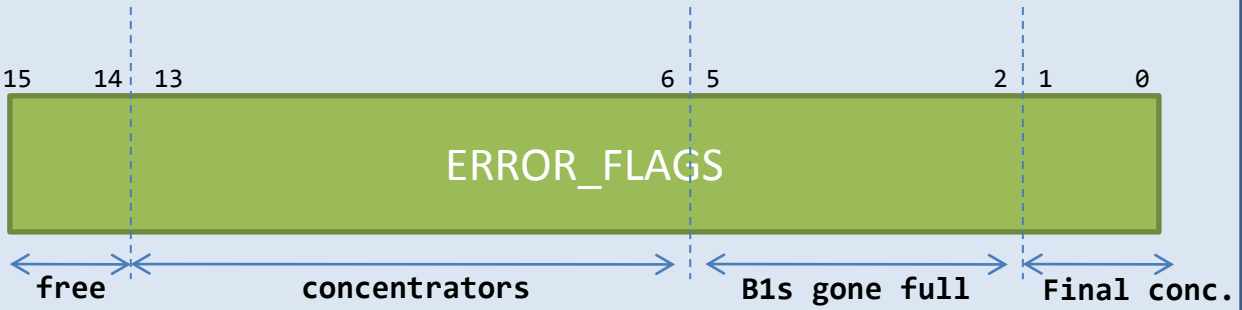
```

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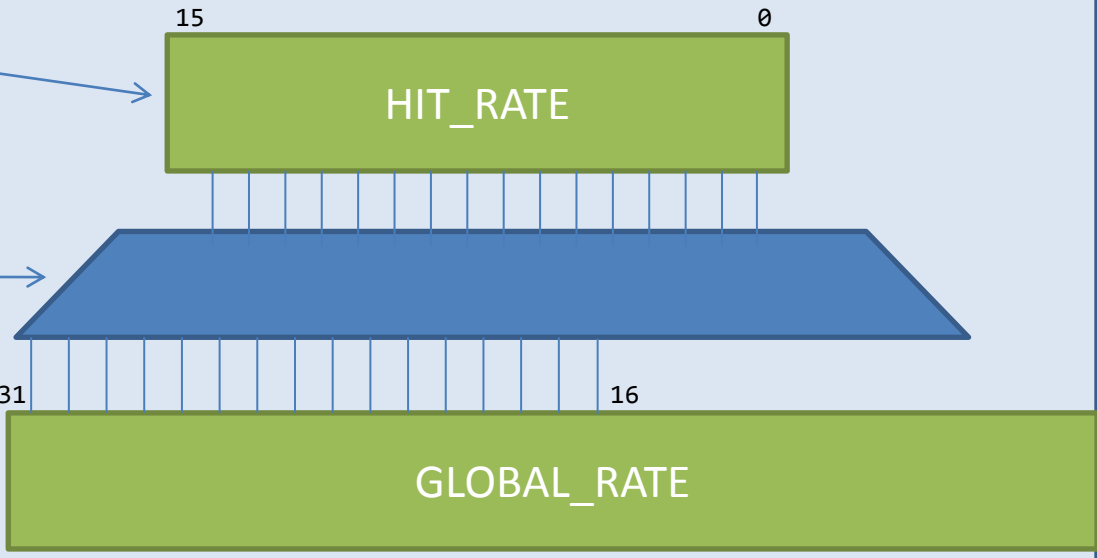
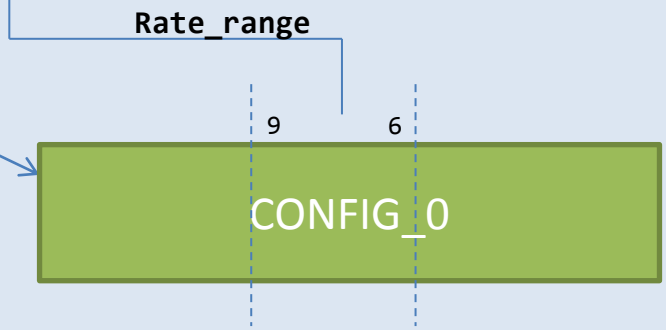


Private 32-bit register



Readout Registers

16-bit registers, 16 RO & 16 R/W registers

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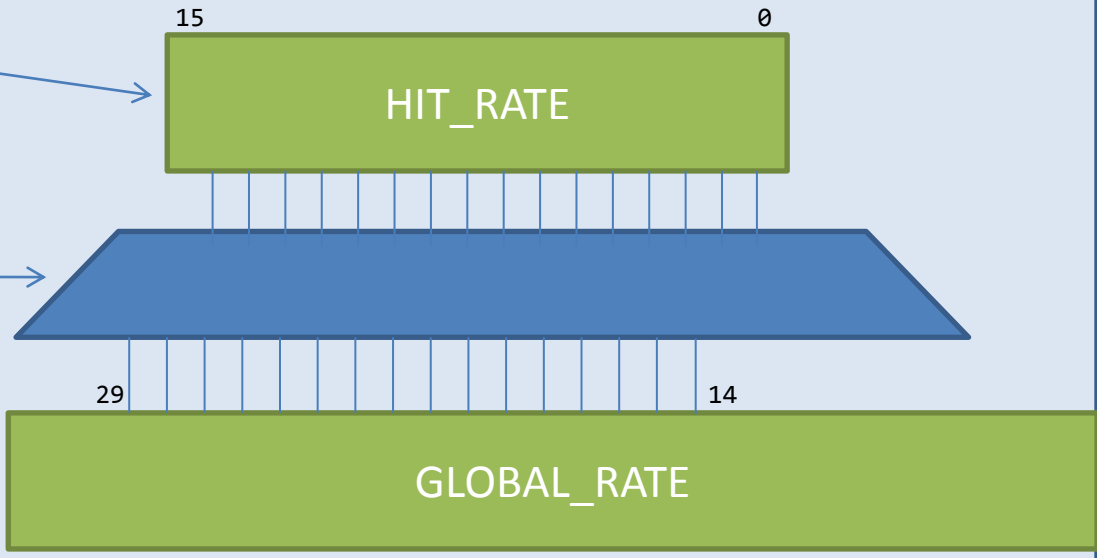
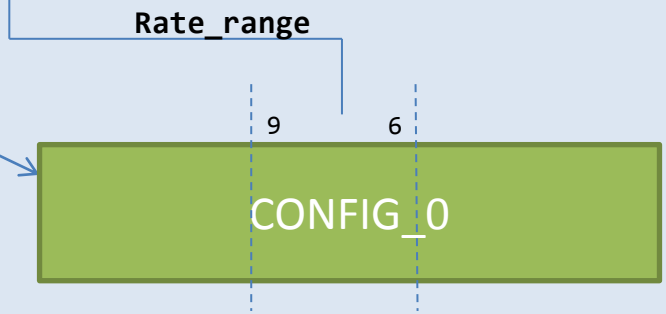


Private 32-bit register



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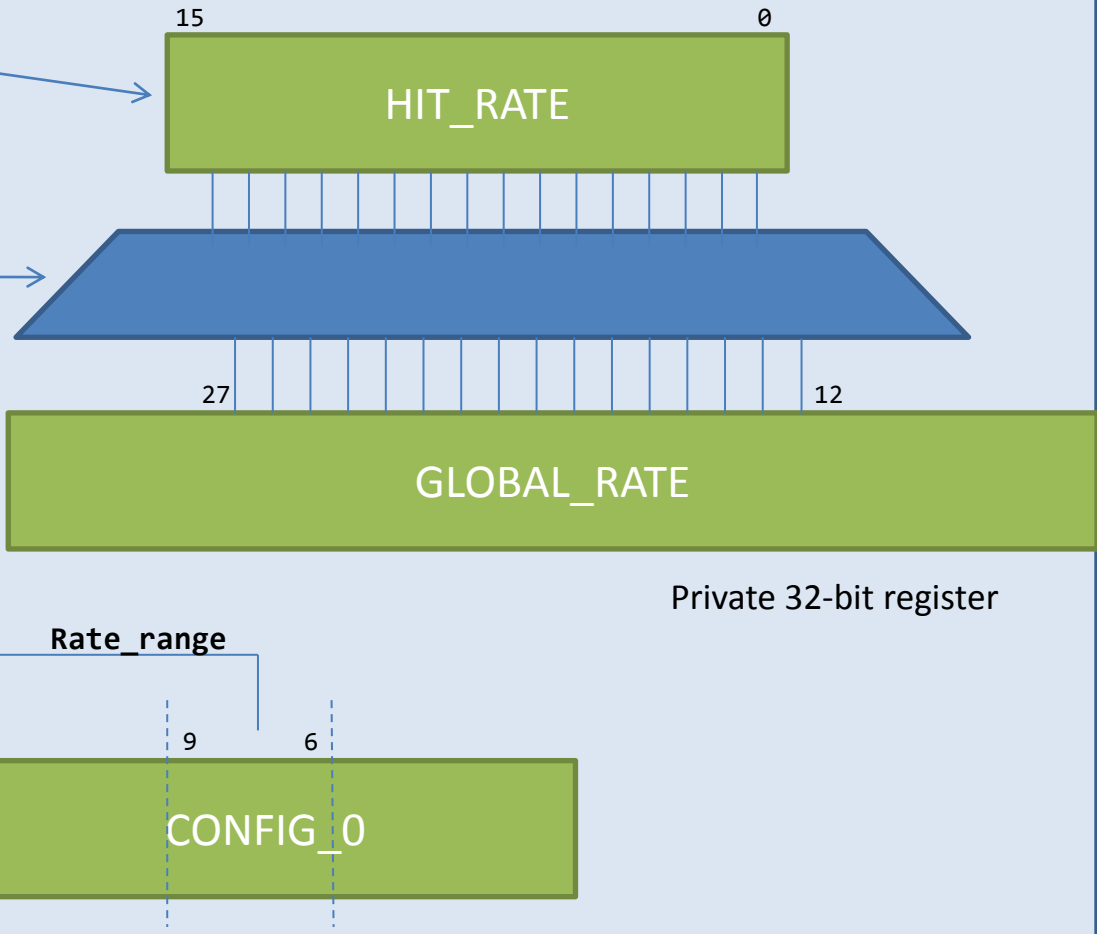

Readout Registers

16-bit registers, 16 RO & 16 R/W registers

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14.…
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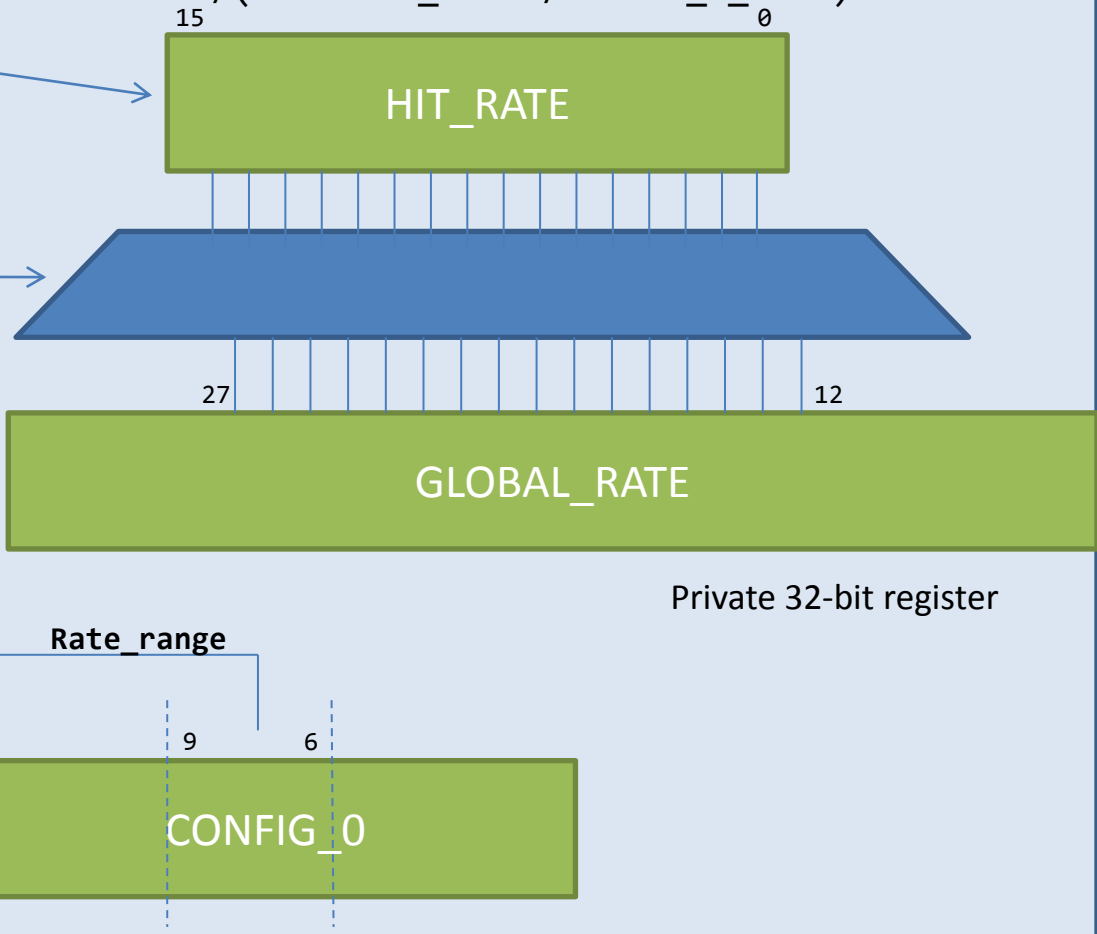
```

Unsigned, expressed in:

counts/(5*2^16*T_RDclk/SUBMAT_Y_SIZE)



Readout Registers

16-bit registers, 16 RO & 16 R/W registers

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6. BCLOST_COUNT1
7. BCLOST_COUNT2
8. BCLOST_COUNT3

Unused in SQUARE Architecture

9. B1_FILL_LEVEL0
10. B1_FILL_LEVEL1
11. B1_FILL_LEVEL2
12. B1_FILL_LEVEL3
13. B1_MEAN_FILL0
14. B1_MEAN_FILL1
15. B1_MEAN_FILL2
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-- READ/WRITE REGISTERS

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Readout Registers

16-bit registers, 16 RO & 16 R/W registers

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```

Unsigned, represents the current used memory in B1n


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Readout Registers

16-bit registers, 16 RO & 16 R/W registers

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10.B1_FILL_LEVEL1
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12.B1_FILL_LEVEL3
13.B1_MEAN_FILL0
14.B1_MEAN_FILL1
15.B1_MEAN_FILL2
16.B1_MEAN_FILL3
```

Unsigned, represents the average used memory in B1n


```
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6. TRIG LATENCY*
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Readout Registers

16-bit registers, 16 RO & 16 R/W registers

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11.…
12.…
13.…
14.…
15.…
16.…
```


```
--COMMAND LIST
NO_CMD(default)        := x"0000";
LOAD_MASK0             := x"0002";
LOAD_MASK1             := x"1002";
LOAD_MASK2             := x"2002";
LOAD_MASK3             := x"3002";
RESET_TIME_COUNTER     := x"0003";
CYCLE_TEST             := x"0004";
SET_MASK_BIT           := x"0005";
RESET_MASK_BIT         := x"0006";
```

Readout Registers

16-bit registers, 16 RO & 16 R/W registers

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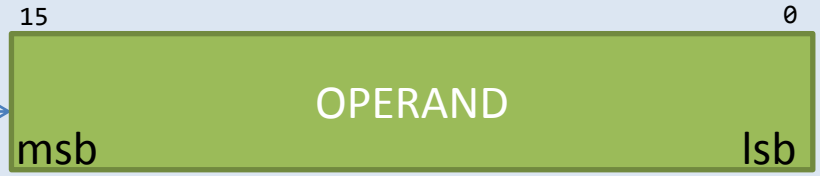
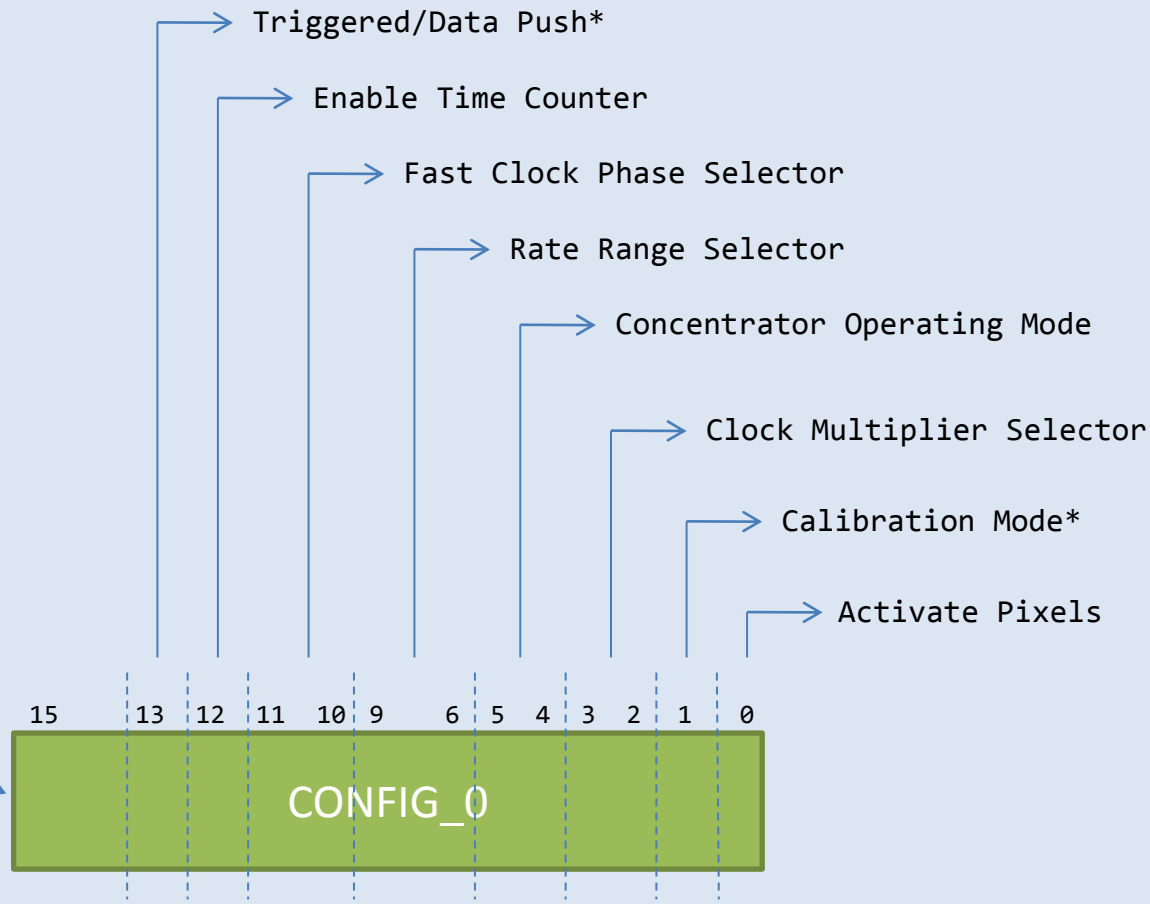


Readout Registers

16-bit registers, 16 RO & 16 R/W registers

-- READ ONLY REGISTERS
1. MSK_COUNTER1_0
2. MSK_COUNTER3_2
3. ERROR_FLAGS
4. HIT_RATE
5. BCLOST_COUNT0
6. BCLOST_COUNT1
7. BCLOST_COUNT2
8. BCLOST_COUNT3
9. B1_FILL_LEVEL0
10. B1_FILL_LEVEL1
11. B1_FILL_LEVEL2
12. B1_FILL_LEVEL3
13. B1_MEAN_FILL0
14. B1_MEAN_FILL1
15. B1_MEAN_FILL2
16. B1_MEAN_FILL3

-- READ/WRITE REGISTERS
1. COMMAND_REGISTER
2. OPERAND
3. CONFIG_0
4. CONFIG_1
5. FLUSH_TIMEOUT
6. TRIG LATENCY*
7. …
8. …
9. …
10. …
11. …
12. …
13. …
14. …
15. …
16. …



Readout Registers

16-bit registers, 16 RO & 16 R/W registers

-- READ ONLY REGISTERS
1. MSK_COUNTER1_0
2. MSK_COUNTER3_2
3. ERROR_FLAGS
4. HIT_RATE
5. BCLOST_COUNT0
6. BCLOST_COUNT1
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9. B1_FILL_LEVEL0
10. B1_FILL_LEVEL1
11. B1_FILL_LEVEL2
12. B1_FILL_LEVEL3
13. B1_MEAN_FILL0
14. B1_MEAN_FILL1
15. B1_MEAN_FILL2
16. B1_MEAN_FILL3

-- READ/WRITE REGISTERS
1. COMMAND_REGISTER
2. OPERAND
3. CONFIG_0
4. CONFIG_1 → Unused in SQUARE Architecture
5. FLUSH_TIMEOUT
6. TRIG LATENCY*
7. …
8. …
9. …
10. …
11. …
12. …
13. …
14. …
15. …
16. …

Readout Registers

16-bit registers, 16 RO & 16 R/W registers

```
-- READ ONLY REGISTERS
1. MSK_COUNTER1_0
2. MSK_COUNTER3_2
3. ERROR_FLAGS
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5. BCLOST_COUNT0
6. BCLOST_COUNT1
7. BCLOST_COUNT2
8. BCLOST_COUNT3
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10.B1_FILL_LEVEL1
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12.B1_FILL_LEVEL3
13.B1_MEAN_FILL0
14.B1_MEAN_FILL1
15.B1_MEAN_FILL2
16.B1_MEAN_FILL3

-- READ/WRITE REGISTERS
1. COMMAND_REGISTER
2. OPERAND
3. CONFIG_0
4. CONFIG_1
5. FLUSH_TIMEOUT
6. TRIG LATENCY*
7. …
8. …
9. …
10.…
11.…
12.…
13.…
14.…
15.…
16.…
```

Concentrator Time Out before Flush Data
Def. 256 (x”0100”)
Expressed in fast clock periods

Readout Registers

16-bit registers, 16 RO & 16 R/W registers

-- READ ONLY REGISTERS
1. MSK_COUNTER1_0
2. MSK_COUNTER3_2
3. ERROR_FLAGS
4. HIT_RATE
5. BCLOST_COUNT0
6. BCLOST_COUNT1
7. BCLOST_COUNT2
8. BCLOST_COUNT3
9. B1_FILL_LEVEL0
10. B1_FILL_LEVEL1
11. B1_FILL_LEVEL2
12. B1_FILL_LEVEL3
13. B1_MEAN_FILL0
14. B1_MEAN_FILL1
15. B1_MEAN_FILL2
16. B1_MEAN_FILL3

-- READ/WRITE REGISTERS
1. COMMAND_REGISTER
2. OPERAND
3. CONFIG_0
4. CONFIG_1
5. FLUSH_TIMEOUT
6. TRIG LATENCY*
7. …
8. …
9. …
10. …
11. …
12. …
13. …
14. …
15. …
16. …

Unused in SQUARE Architecture

TO DO:

verify that EACH required/requested/desiderata operation on chip is affordable with the presented logic.

- Calibrations..
- tests, (ML_ena, resets, mask…)
- …