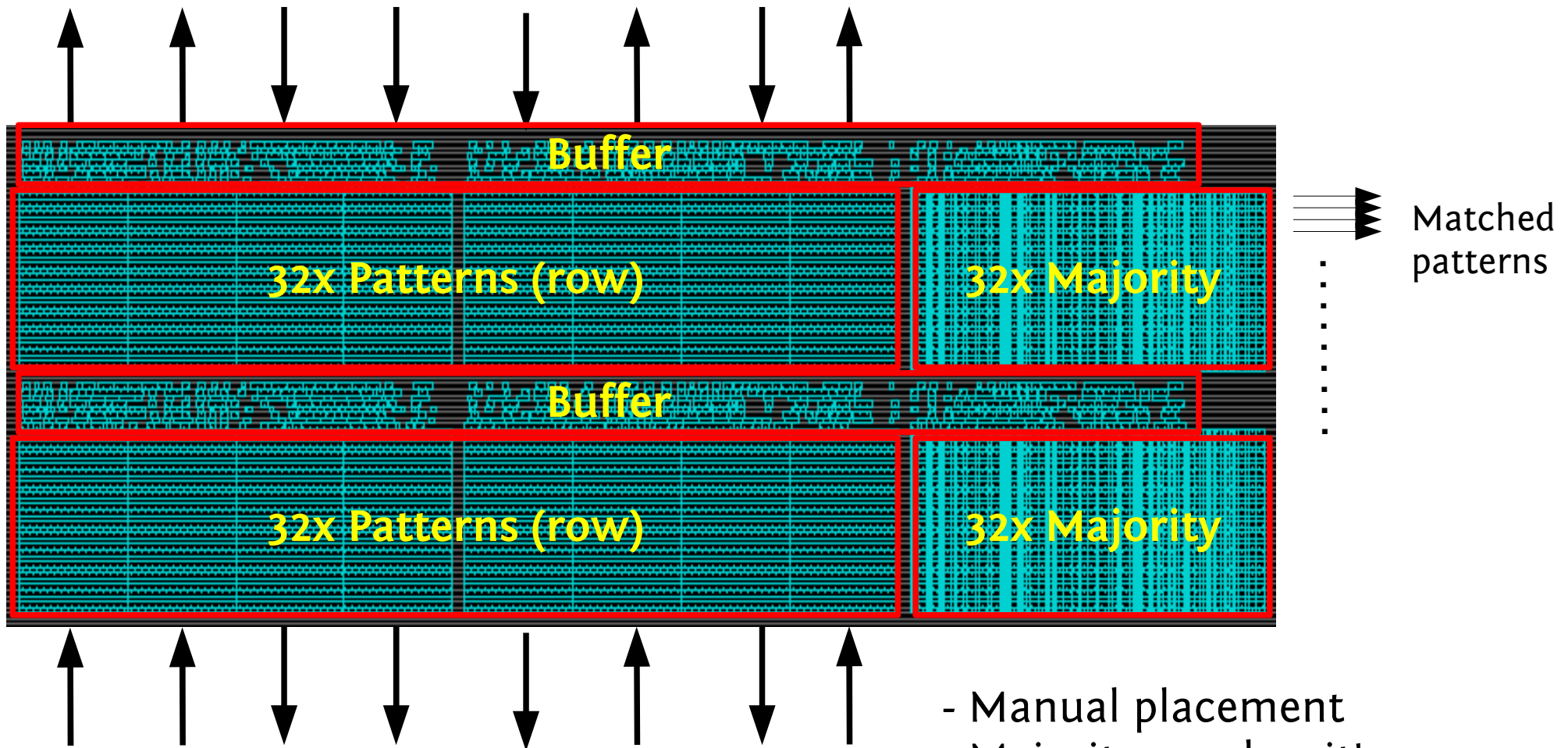


AMCHIP04 WITH UMC90 STD CELLS

- UMC90 FSD0A_A standard cells library
- Our custom standard cells:
 - single_layer
 - search_line
- Tools used
 - Synopsis DC D-2010.03-SP1-1 (synthesis)
 - Cadence SoC Encounter v07.10-s219_1 (placement, routing)
 - Synopsis PT D-2010.03-SP1-1 (timing analysis)
 - Custom scripts (manual place)

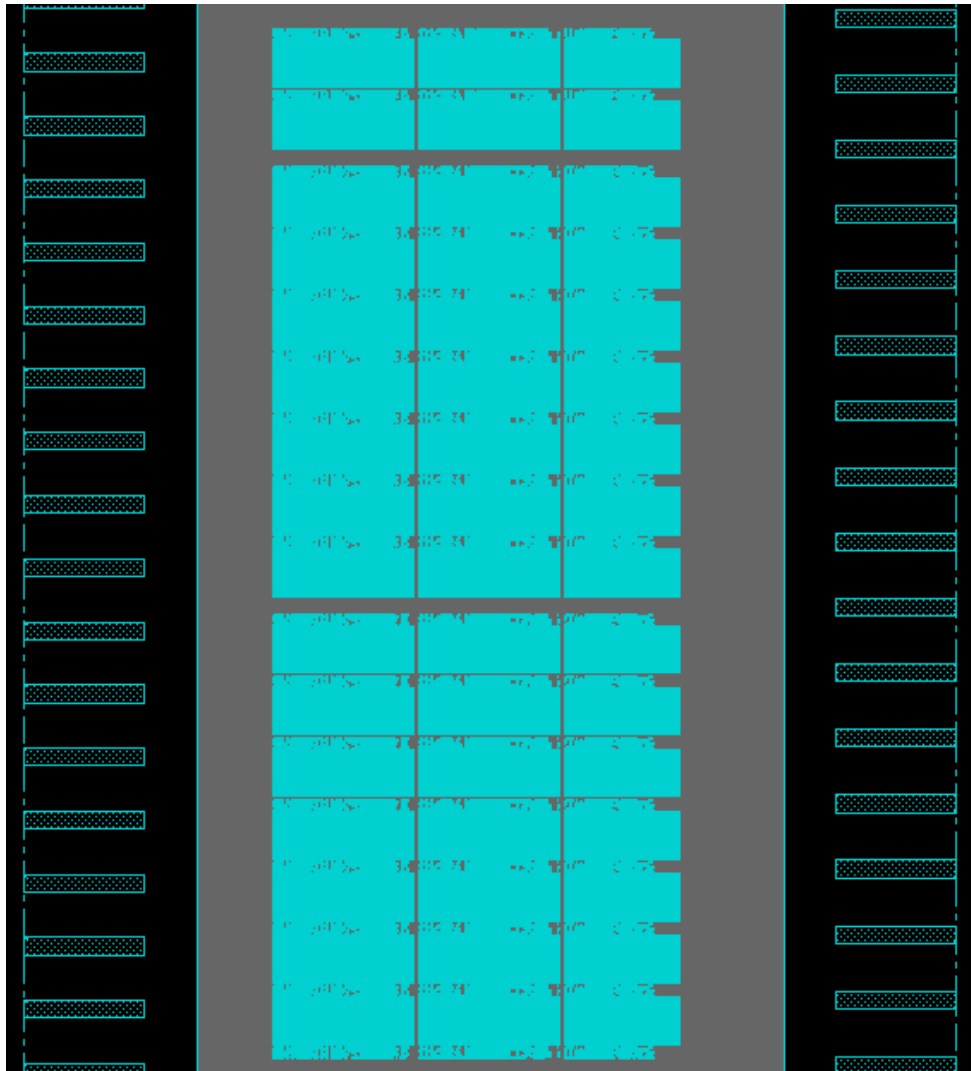
Basic bank structure

8x Input Bus



- Manual placement
- Majority row has it's own clock tree

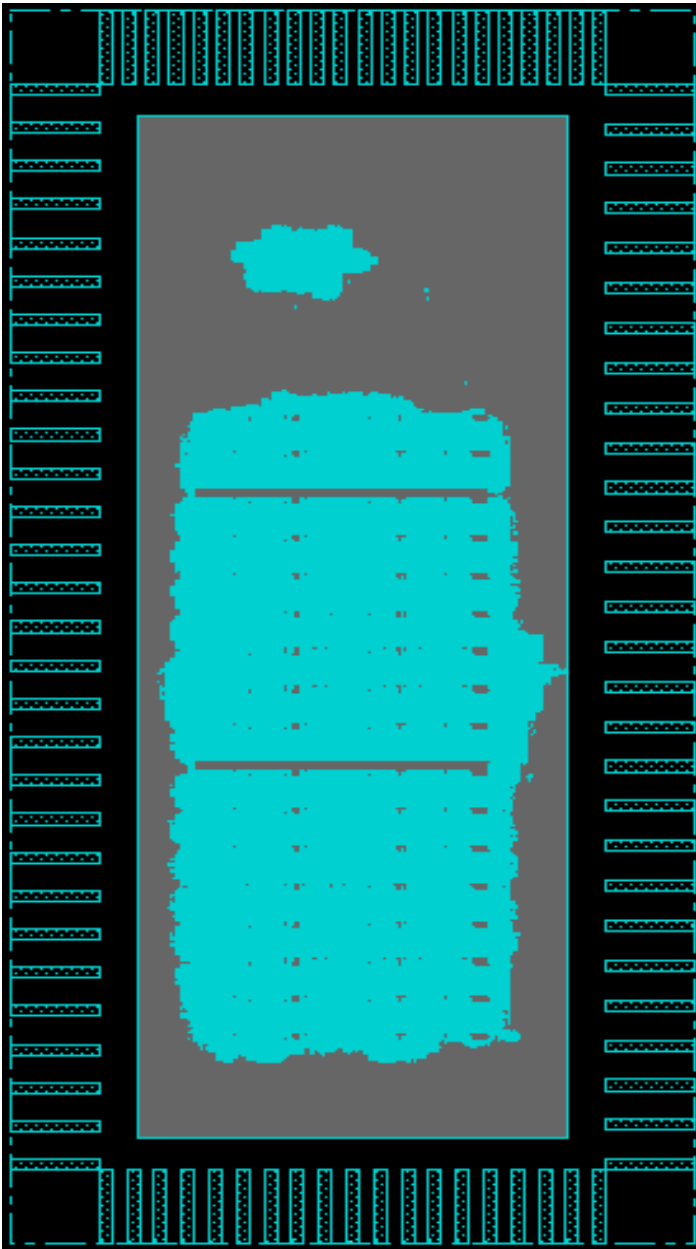
512 patterns bank



16 x 32 pattern blocks are manually placed to build a 512 patterns bank.

Horizontal and vertical gaps are left for power grid.

All logic placed

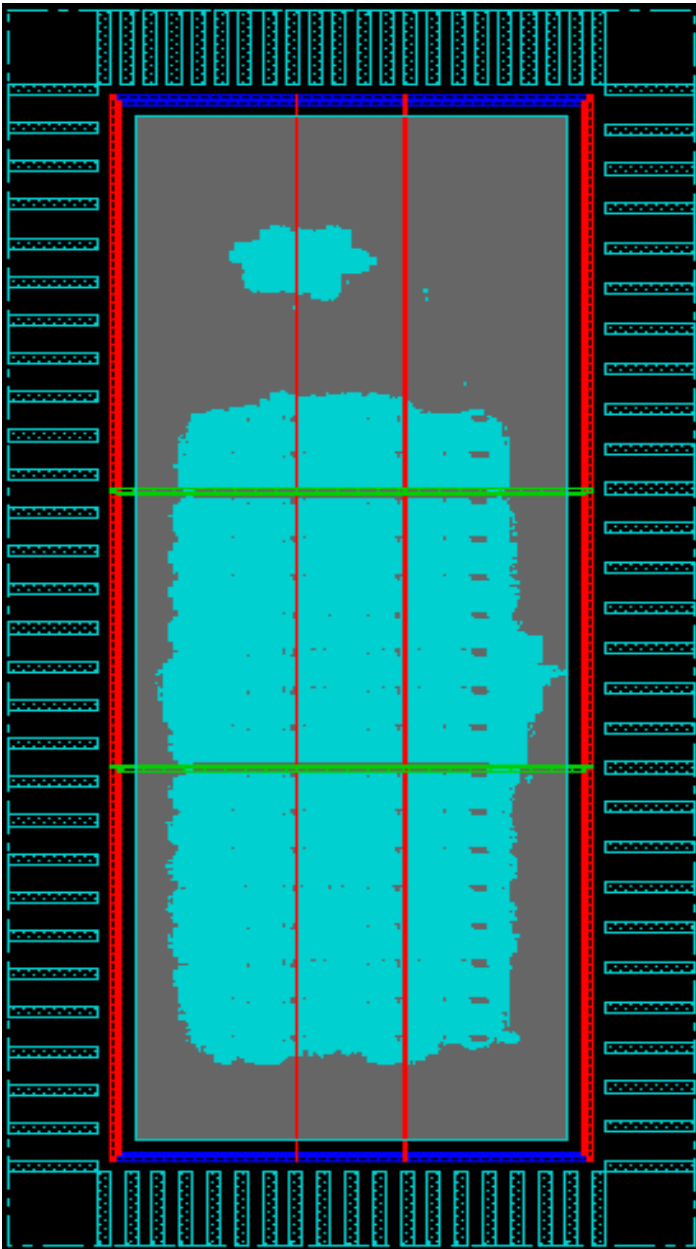


The pattern bank occupies most of the area.

All the other control logic scale very weakly with the number of patterns.

We could try to fill the chip with a bigger column of patterns (~800), but is not critical for this [mini@sic](#) prototype to have a bigger bank.

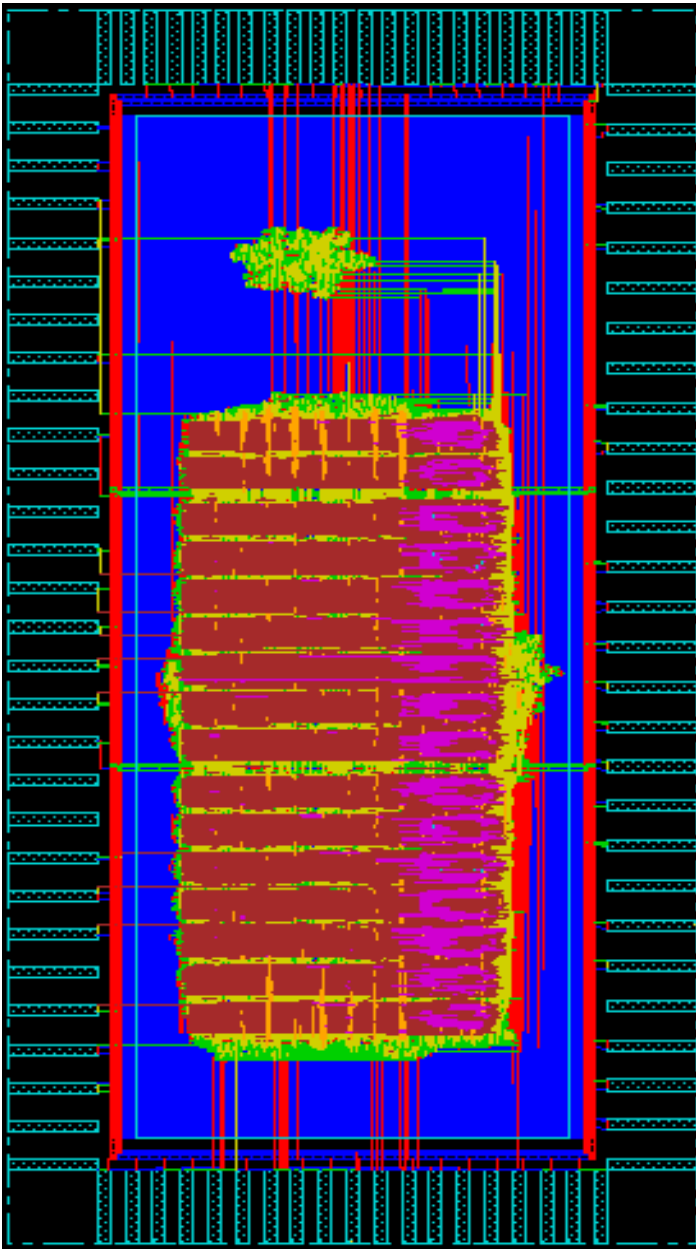
Power grid



Power distribution is done by two big horizontal stripes and two thinner vertical stripes.

We are waiting a feedback from IMEC about this power grid design.

512 patt AMCHIP04 routed



First results of routing (wroute, clock tree routed first, no post-routing optimization) are reasonable:

- routing is simple and consistent with our plans in the bank area (vertical buses, horizontal output)
- no critical congestions in other areas

Timing Analysis

- We have working skeleton scripts for static timing analysis
- A first look at the timing with PrimeTime showed some various setup and hold violations
 - No post-route optimization was done, buffer optimization in this step might remove most of the violations
 - Global signals running through all the patterns column have setup violation
 - Force a better routing of the column area
 - Manually optimize buffer usage
 - Split the column in two shorted columns
- Some optimization and re-routing is needed, but no critical flaws are detected