HASPIDE WP2: Electronics and DAQ

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HASPIDE WP2 Target and Tasks

Two targets:

- Clinical dosimetry and radiation flux measurement
  - Current signal from the detector, to be converted in frequency, then digitized (counting pulses) and acquired by an FPGA-based DAQ board
- Single particles and neutron detection
  - Single charge pulse read-out solution (based on a previosly designed chip); data acquisition by an FPGA-based board

Tasks:

T2.1: Design of the front-end chip for clinical dosimetry

T2.2: Design and test of the data acquisition board for neutron detection

T2.3: Design and test of the data acquisition board for clinical dosimetry

HASPIDE WP2 People

Participant institutions and people (as listed in the proposal):

- **Milano**:
  - Valentino Liberali (WP2 Responsible)
  - Alberto Stabile
  - Luca Frontini
- **Torino**:
  - Gianni Mazza
  - Edoardo Bianco
  - Richard Wheadon
- **Perugia**:
  - Pisana Placidi
- **LNS**:
  - Pietro Paolo Falciglia

+ 1 AdR (Torino)

Milestones

First year (2022) milestones:

M2.1: Design of the first miniAsic (M8)

M2.2: Test board for the first miniAsic (M12)

Second year (2023) milestones:

M2.3: Characterization of the first miniAsic (M15)

M2.4: Design of the second miniAsic (M18)

M2.5: Test board for the second miniAsic (M22)

M2.8: Design and fabrication of the data acquisition board for neutron detection (M24)

The miniAsic for clinical dosimetry will be designed in 28 nm CMOS.
Two versions: a first prototype, and a final chip.
All the features (including the interfaces with the DAQ board) must be included in the first design.

The chip for neutron detection has been previously designed in a different technology.

The miniAsic (1)

Technology: TSMC CMOS 28 nm HPC+

- mature technology
- available through Europractice
- excellent radiation hardness
- already used in previous designs (TimeSPOT, HTT)

Drawbacks:

- performance limited by parasitics; complete layout design and parasitic extraction required for meaningful simulation results
- dedicated NDA required before exchanging design information between different teams

Other drawbacks:

- "Chip crisis": Several TSMC shuttles are extremely loaded; possible delays in MPW fabrication
- Limited number of miniAsic submissions; advance reservation required (3 months before submission)

The miniAsic (2)

Deadlines and costs for **mini@sic** submissions:

- Submissions: Feb. 2, May 25, ...
- Min area: 1 mm^2
- Cost (discounted, w/o VAT): 7833 € (min area) + 681 € / 0.1 mm^2

The run schedule for the second half of 2022 will be published in late March. Design registration must be done at least 3 months in advance (the sooner the better).

Actions

- Update WP2 participant list (+ mailing list)
- Regular WP2 meetings in 2022
- Define the complete architecture (detector + read-out chip + acquisition board) of the two deliverables as soon as possible
- Book miniAsic submissions (in advance!)
- Joint meetings with WP1 on detector / read-out interfacing (for clinical dosimetry)

ASIC developments in Torino

Gianni Mazza

HASPIDE collaboration - Torino group

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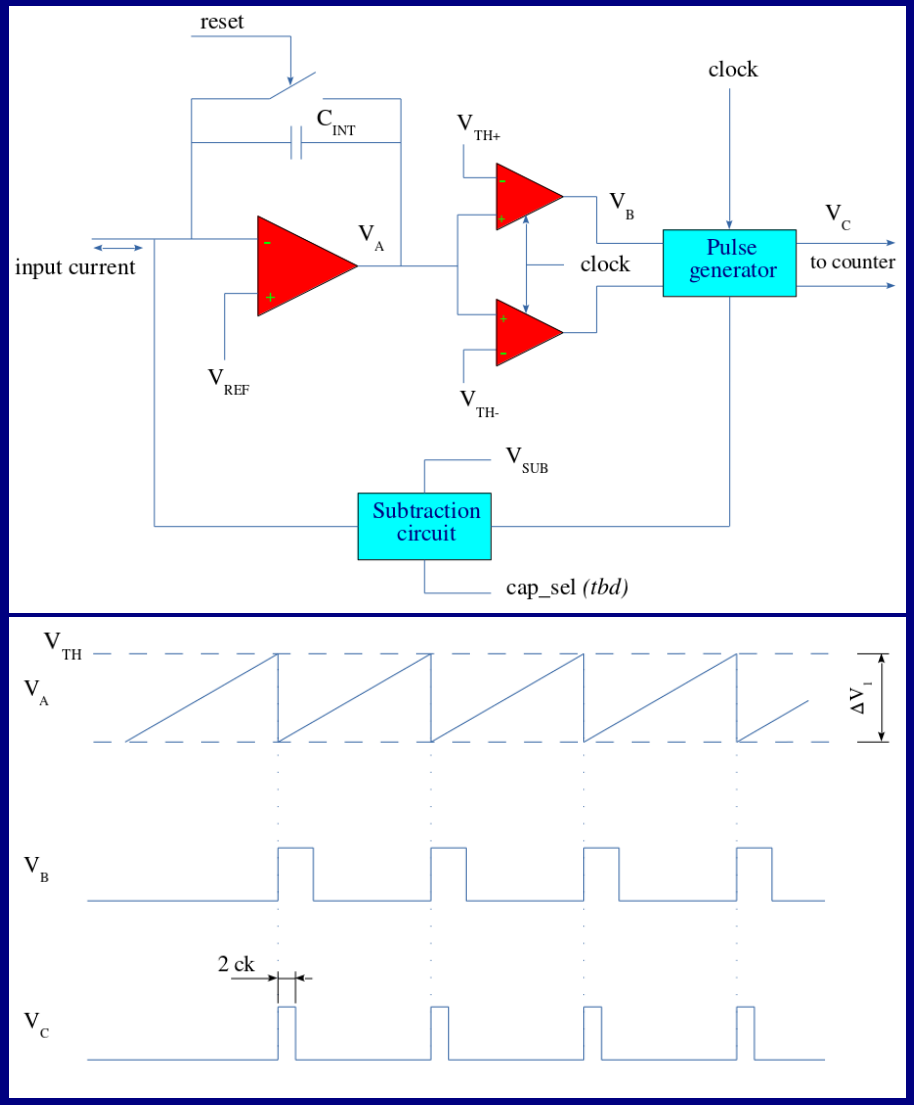
January 18^{th} 2022

Torino tasks

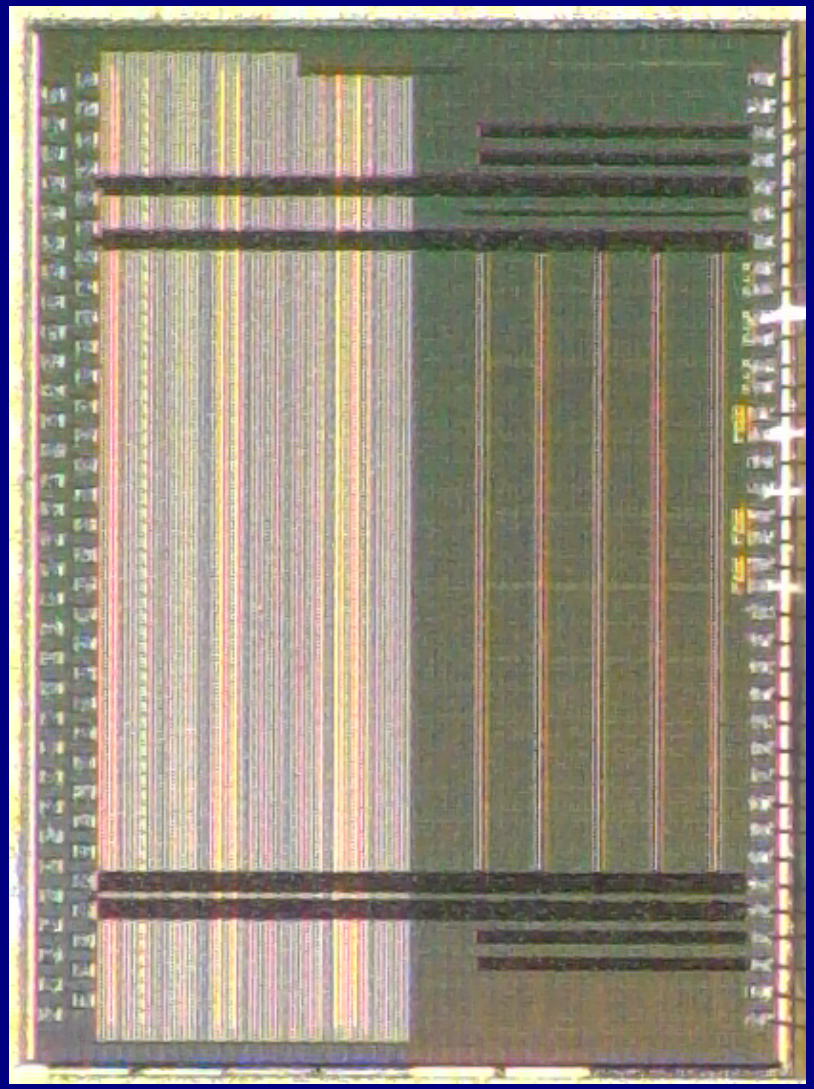
- Tasks in the framework of the WP2 (FE electronics and DAQ)
- Task 1 : design of a current mode readout ASIC
  - Based the charge recycling intergrator technique
  - Technology : CMOS 28 nm
  - In collaboration with INFN Milano
- Task 2 : evaluation of the ToASt ASIC for pulse mode readout
- AdR procedure ongoing

Recycling integrator



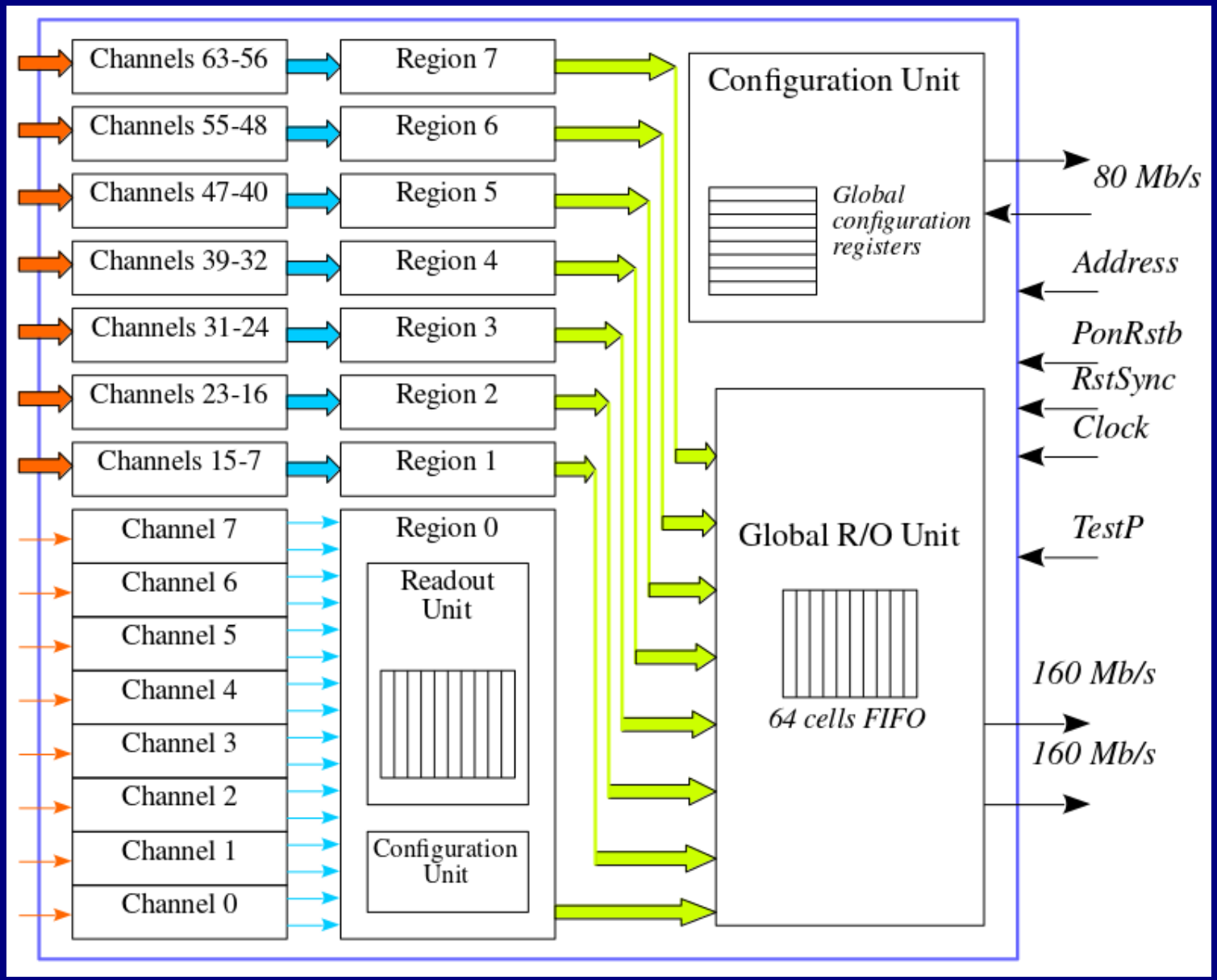
- Well known architecture
  - Used in the Tera ASIC family
  - Beam monitor at CNAO
- To be implemented in 28 nm technology
  - Faster, smaller parasitic
  - Higher radiation tolerance
  - Low voltage supply can be a challenge

ToASt ASIC



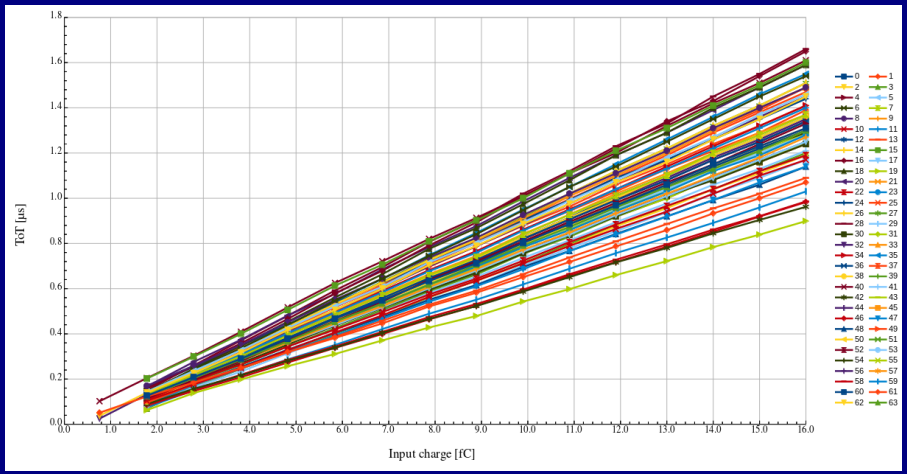
- 64 channels ASIC for strip readout
- Detector capacitance 2÷17 pF
- ToA and ToT measurement
- Input charge up to 50 fC
- Reference clock 160 MHz
- Die size 3.24 $\times$ 4.41 mm^2
- Time resolution (rms) 1.8 ns
- CMOS UMC 0.11 μm technology

ToASt block diagram

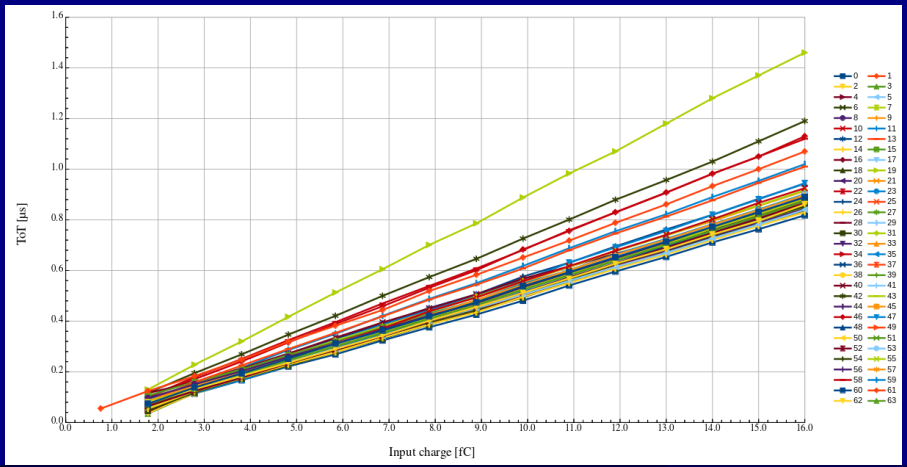


Test results *(Warning : VERY preliminary results)*

Before calibration



After Calibration



- Configuration interface ok
- Data transmission ok
- All 64 channels respond correctly to test pulse
- Fairly large gain spread
  - Expected : depends on a very small current
  - Channel level gain calibration implemented
  - Gain calibration procedure under optimization *(some channels are overcorrected)*
  - Threshold tuning to be done