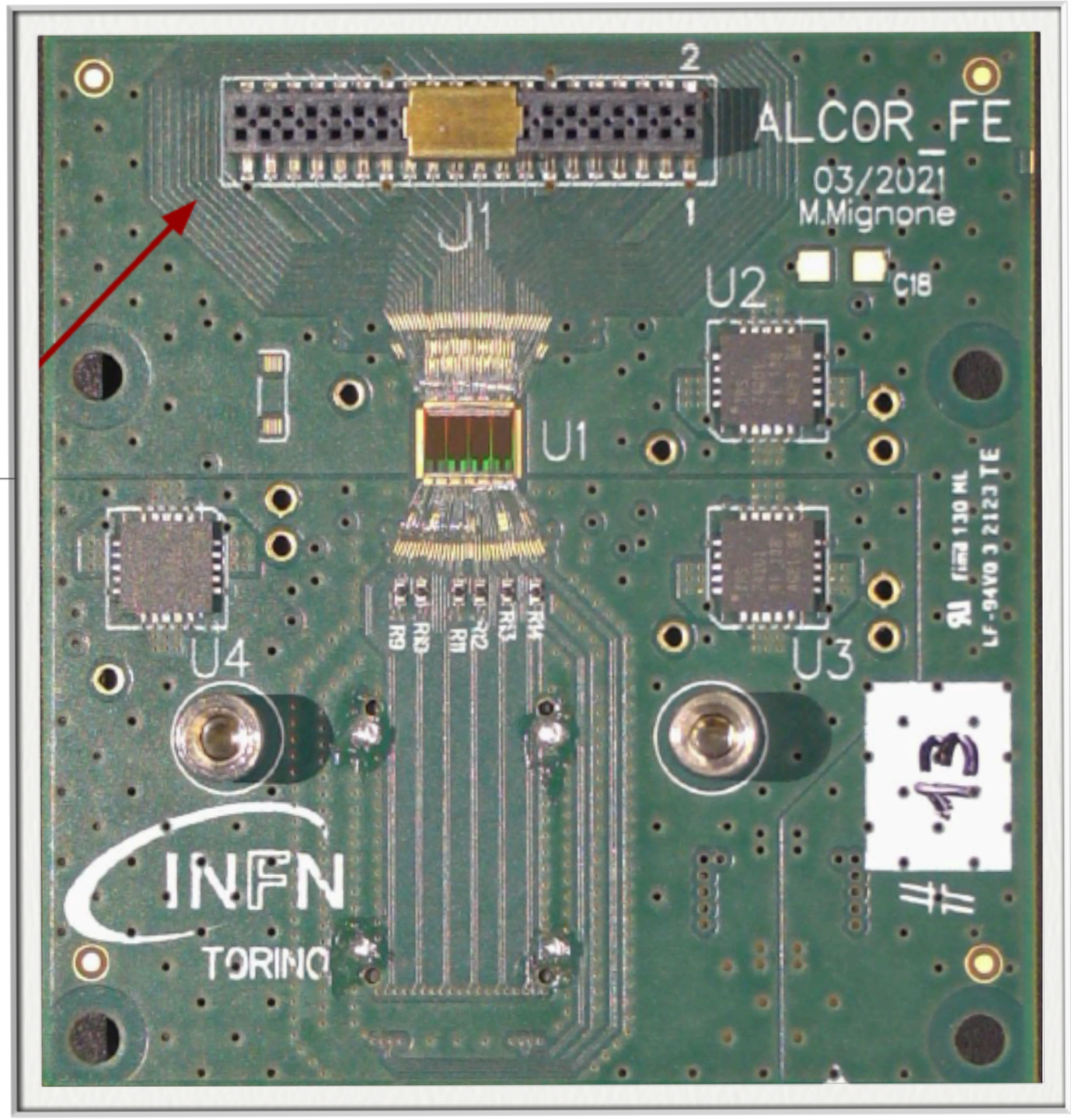
# Plans for ALCOR-v2

dRICH meeting
Monday Jan 31, 2022, 11:30 AM



# ALCOR ASIC for fast-timing with SiPMs

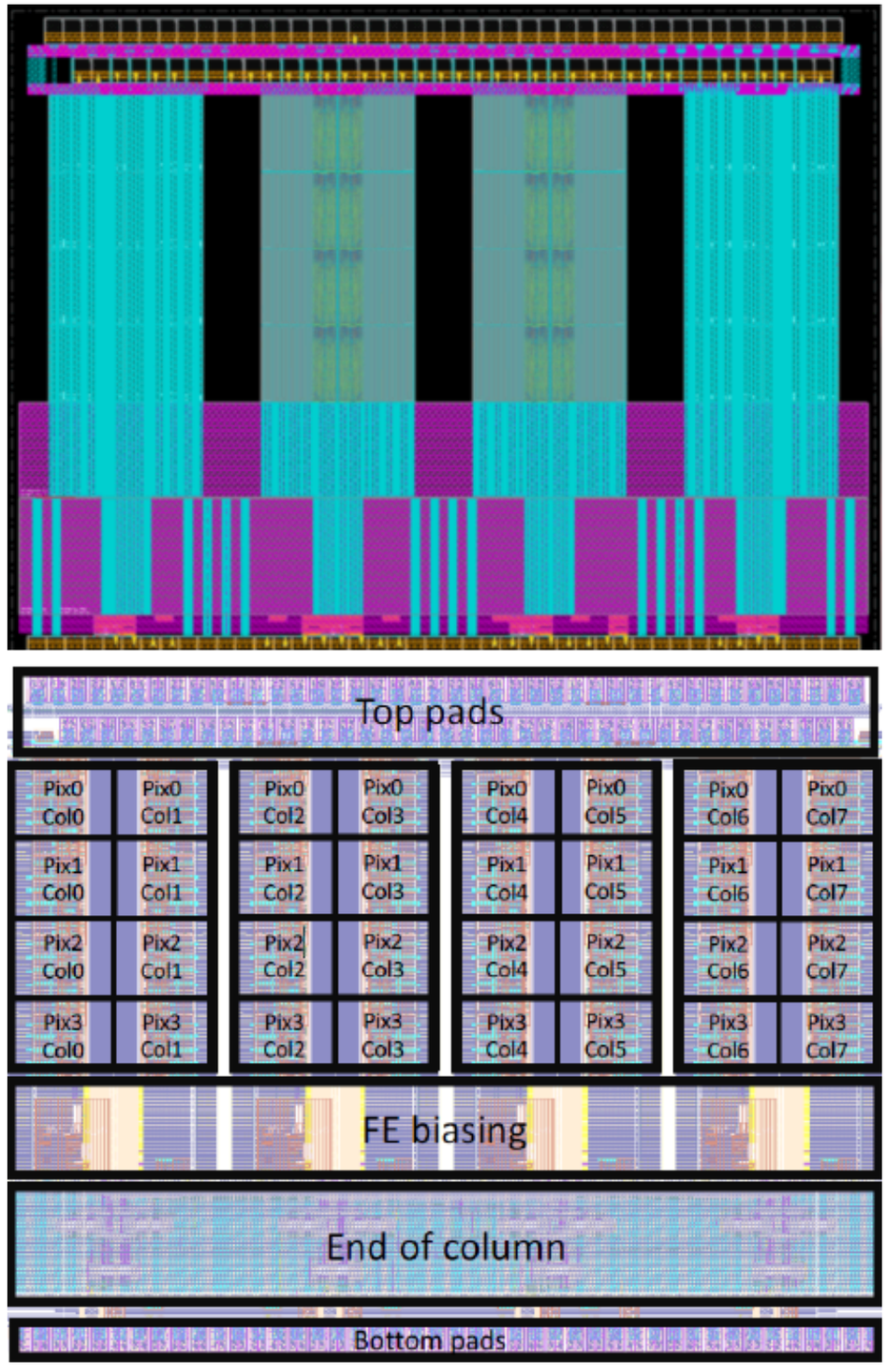
- ALCOR (A Low Power Chip for Optical Sensor Readout) stems from an INFN R&D as a mixed-signal ASIC for the readout of SiPMs in the framework of Darkside. Optimised for cryogenic operation and low power

- pixel matrix mixed signal ASIC the chip performs amplification, signal conditioning and event digitisation, and features fully digital I/O

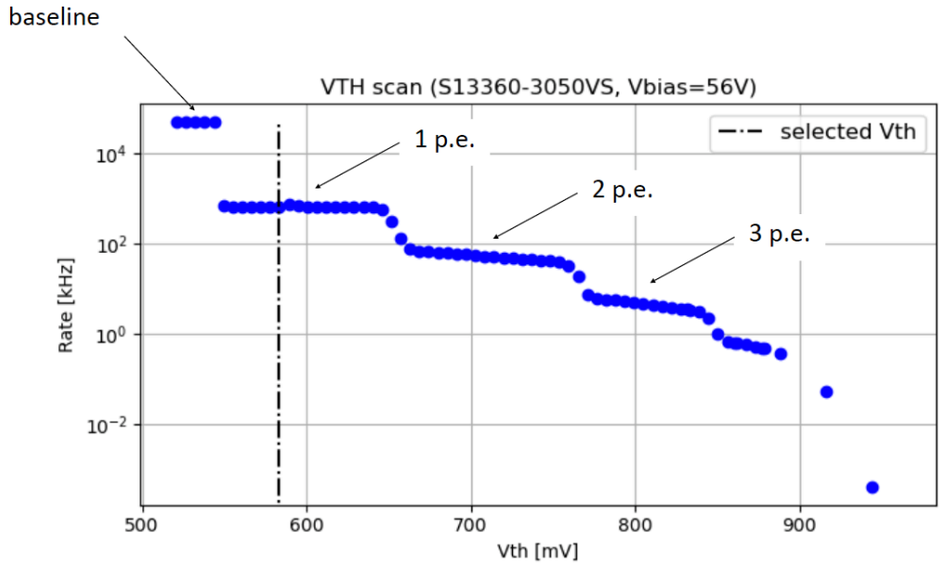
- Single-photon time tagging mode or time and charge measurement

- 4 LVDS TX data links, SPI configuration

- operation up to 320 MHz (TDC binning down to 50 ps)



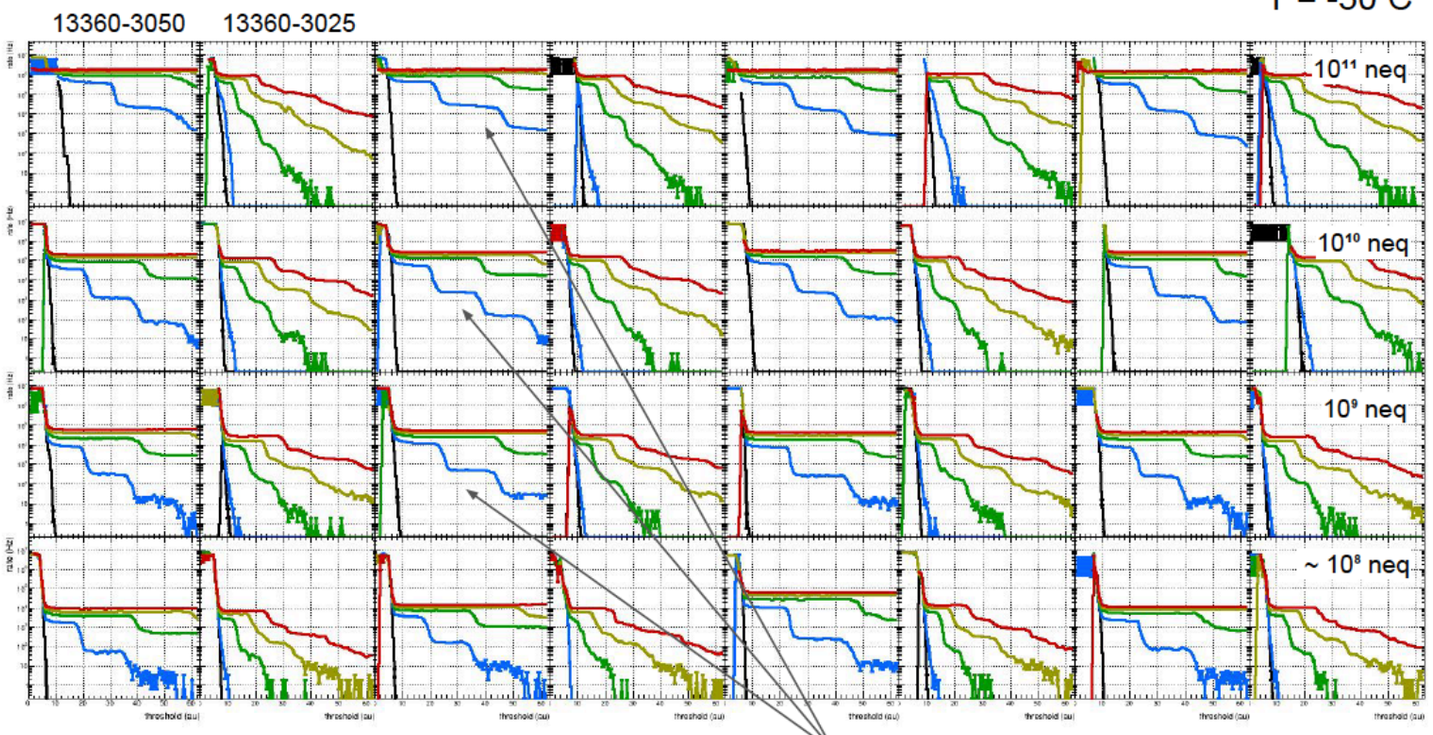
# Threshold scan with SiPMs

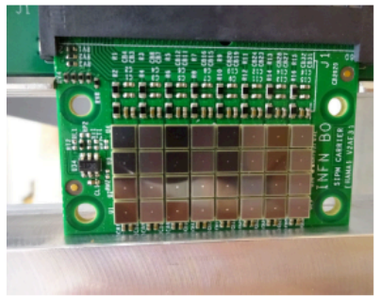



## Hamamatsu (HAMA1 #2) threshold scans

PRELIMINARY

T = -30 C



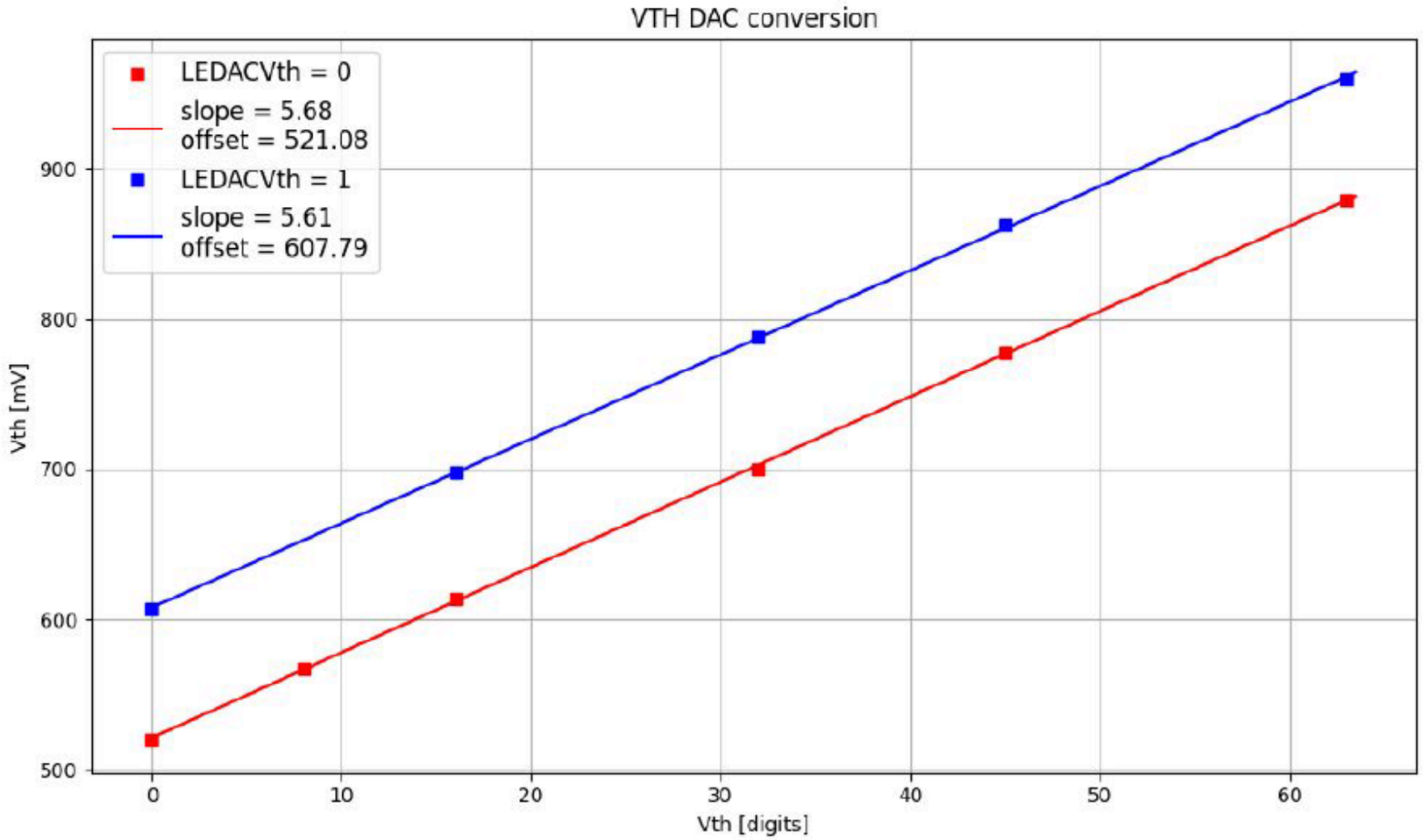



**irradiated board after annealing**

still working!

Preliminary: successfully tested in lab by Roberto up to 1 MHz hit rate / channel, with one single channel

# Threshold scan with SiPMs




Pixel level register LEDACVth allows to shift the DAC threshold range to compensate eventual channel-by-channel offsets

# ALCOR-v2: operation with various SiPM

**nice if ALCOR can be tested with a large range of SiPM**

* different manufacturers, micro-cell size and capacity

- for EIC we might eventually want to have ASIC optimised to chosen SiPM, but we do not know which SiPM is best to be used yet

- best if ALCORv2 can function with large spectrum of SiPM

* SiPM-ASIC coupling: AC or DC

* analog part / amplification stage: gain should be sufficiently high to work also with rad.tolerant SiPM with lower gain ~ 3 $10^5$

# ALCOR-v2: whishlist

1. Bug fixing (TDC control logic)

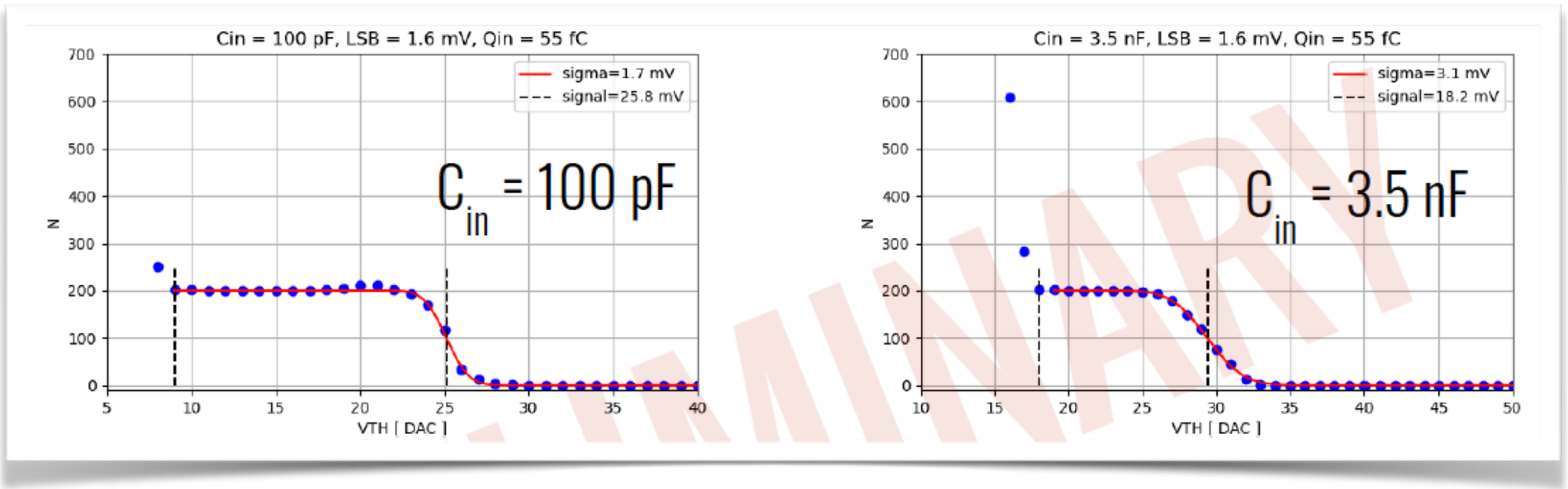
2. high gain

* 2 branches and 4 gain settings already available (≃ 60 - 600 mV/pC) —> increase the gain

* single-photon detector of SiPM with low-gain (3 $10^5$)

3. AC coupling on chip

* not for v2 —> to have more flexibility for test with different SiPM



# ALCOR-v2: schedule and plan

1. Submission mid of April 2022

2. We should receive the new ASICs (∼ 40) by the end of July 2022 (assuming no delay in the production)

3. Until November: tests in LAB (electrical and functional tests; tests with irradiated SiPMs)

4. Possibly test-beam in November at CERN PS: dRich+SIPMs+ALCOR-v2

Test beam in September at CERN SPS: dRich+SIPMs+ALCOR-v1