Spurious Signals on the MSD Strips

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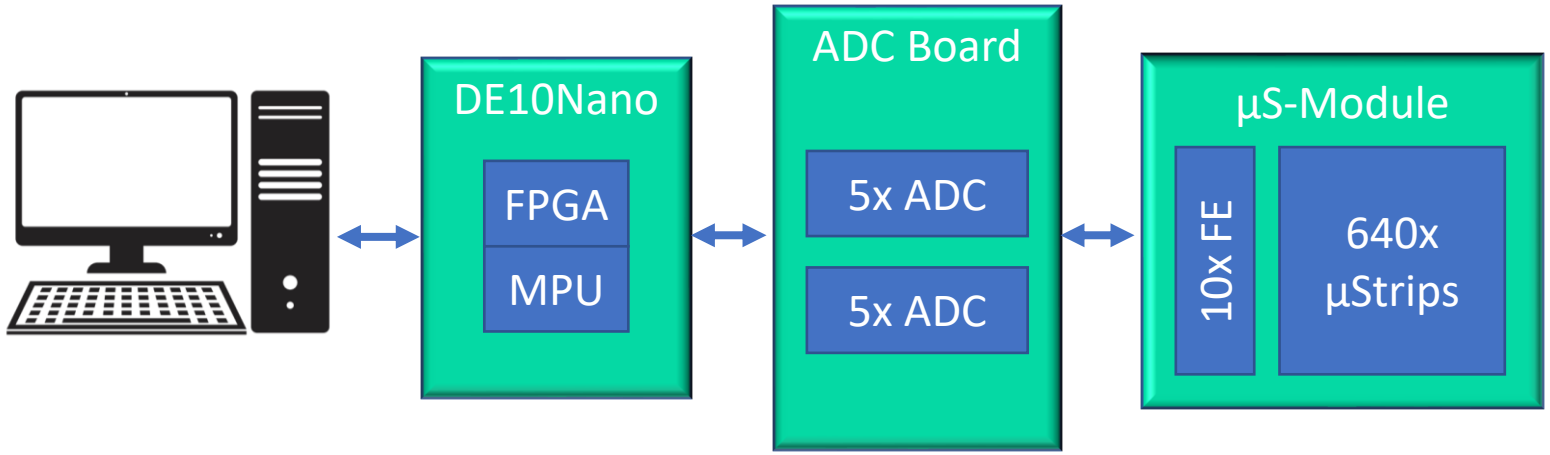
FOOT Physics Meeting – 04-May-2022

Spurious Signals on the MSD Strips - Outline

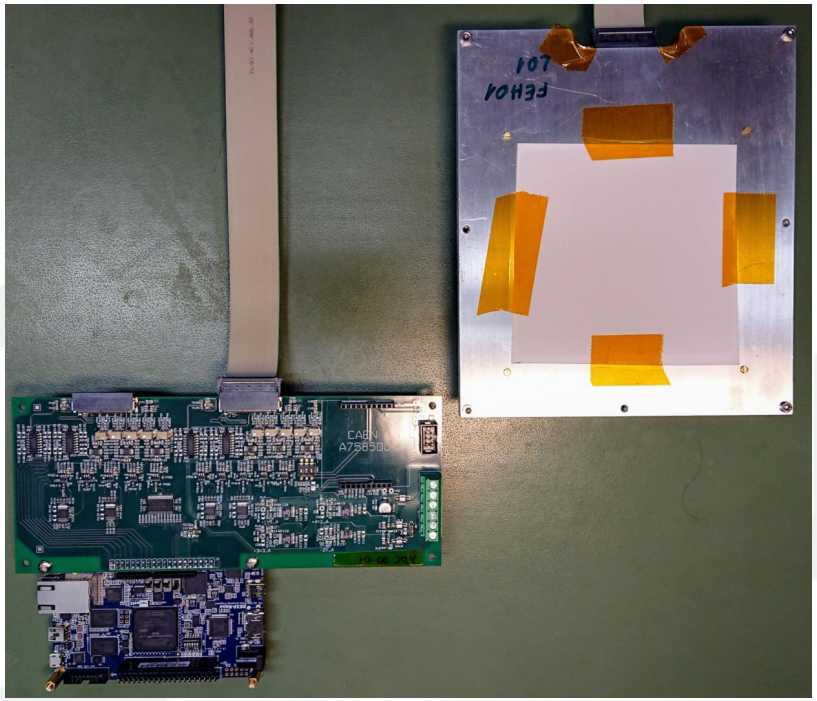
1. Recap on the MSD architecture and setup
2. Problem description
   - Spurious signals in the last VAs channels
3. Addressing of the problem
   - ADC sampling time
   - Reset of the digital circuitry of VAs
4. Verification: Calibration
5. Verification: Laser Setup

Recap on the MSD Architecture

Single µStrip Detector (MSD)

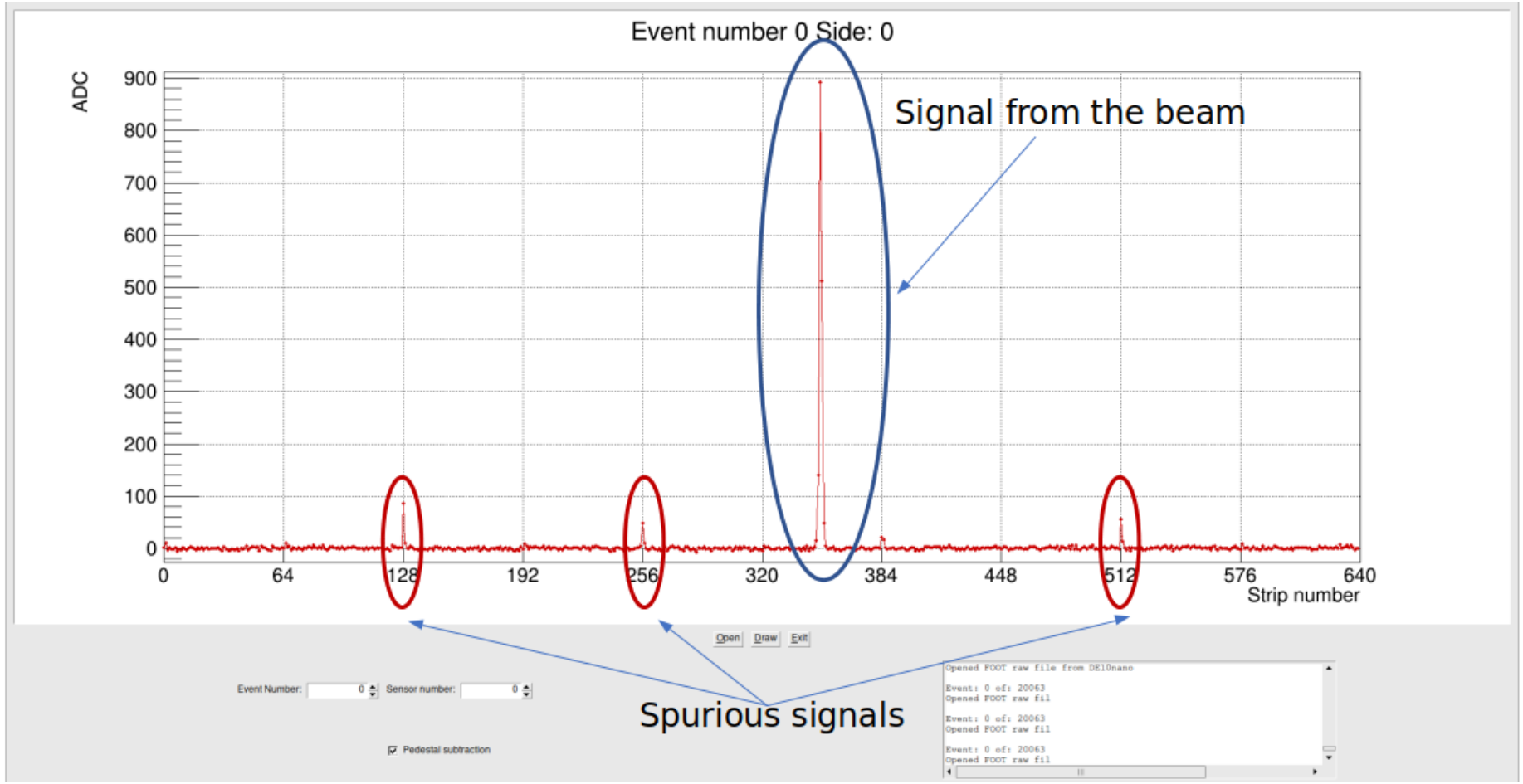


- 1x µStrip Detector (L13):
  - 10x IDE1140 front-ends (VAs)
- 1x ADC Board:
  - 10x AD7276 ADCs
- 1x DE10Nano: data acquisition



Spurious signals in the last VAs channels

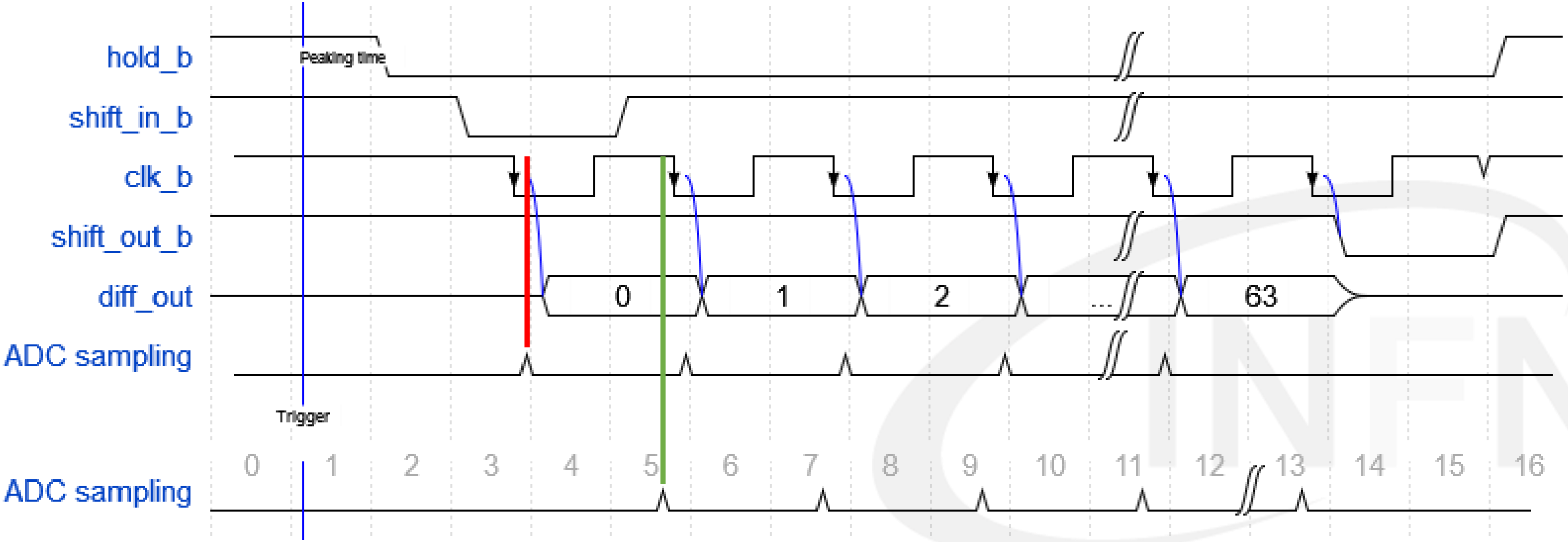
RECAP: From last test beam we spotted these spurious signals in the last channels of the VAs



First possible cause: Sampling time

Sampling the strips analog signals too early

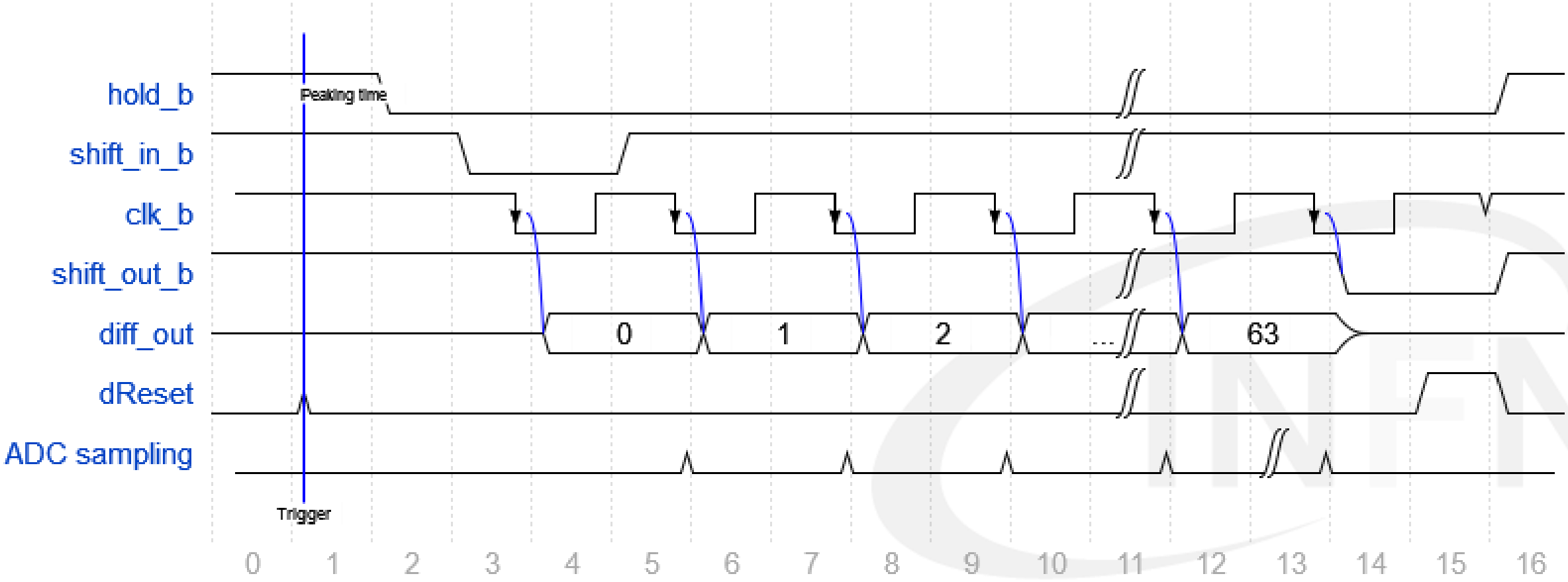
- GOAL: Sample one strip just before the consecutive one
- Delay the sampling time of a parametrizable value



Second possible cause: Reset

Digital circuitry of VAs need 65 clock cycles or reset

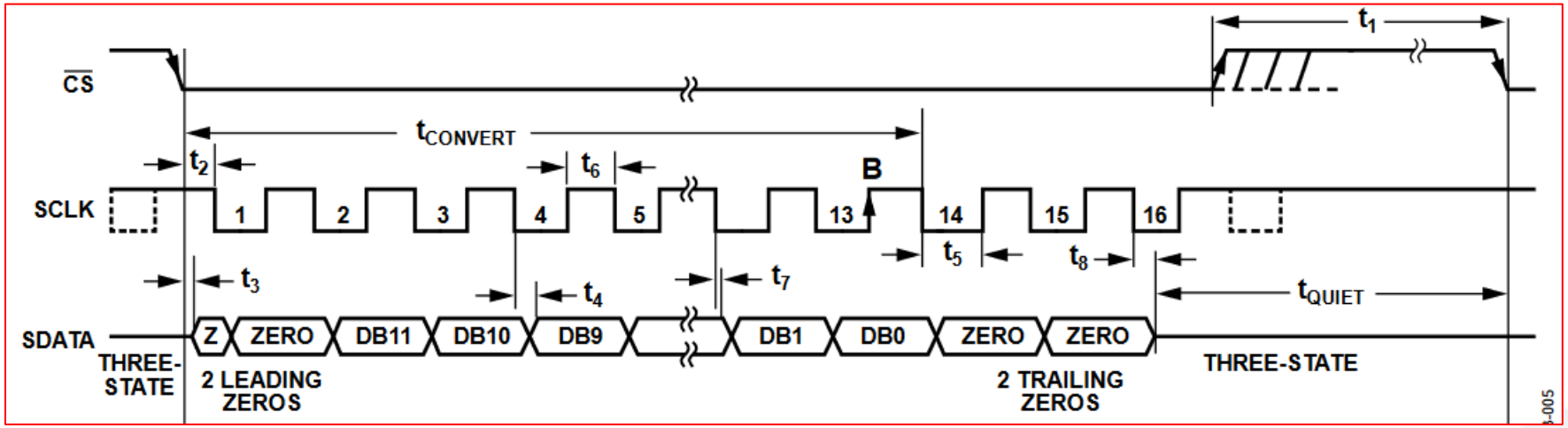
- We were sending 64 clocks per VA -> Added a Reset at beginning and end of a transaction

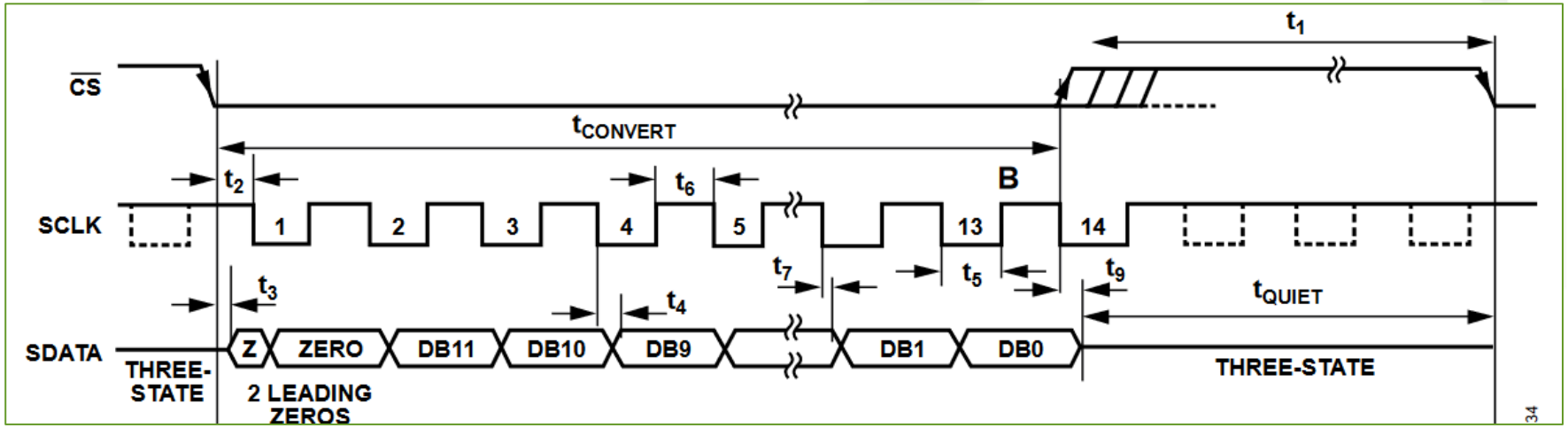


Possible Update: Speed-Up the Readout

Reduce ADC conversion time by using AD7276 ADC *Fast-Mode*

- From 16 to 14 clock cycles -> 12.5% faster





Verification Plan

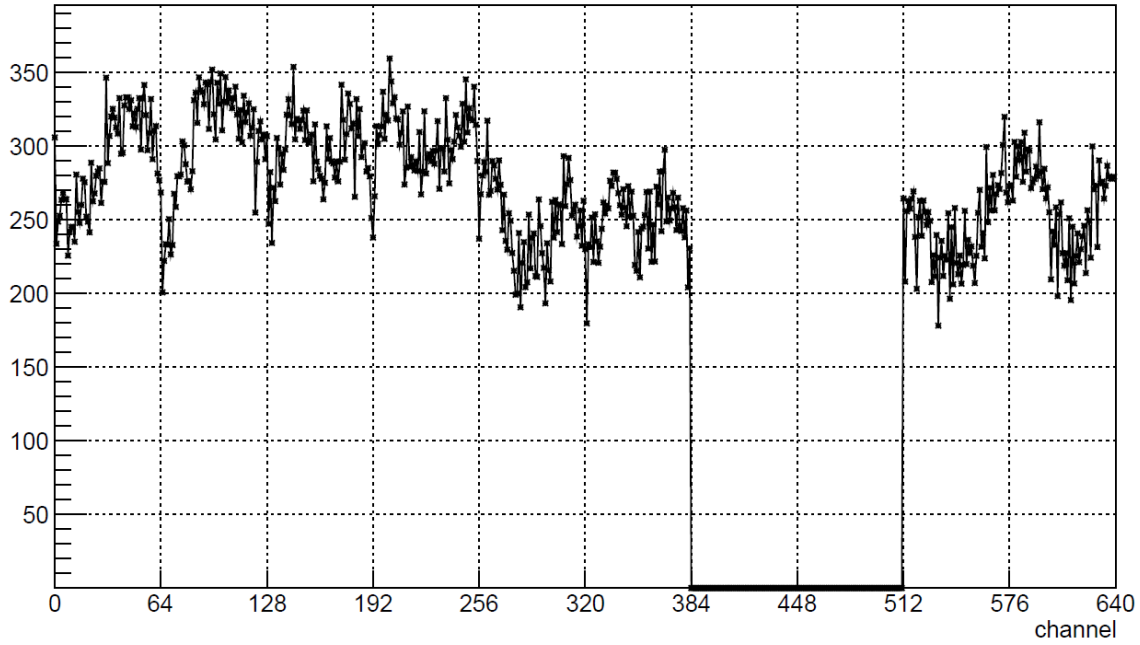
1. Calibration of the system with the old GateWare (GW) as reference
2. Coarse scan to find the optimal ADC sampling delay
   - VA *clk_b* period: 800 ns
   - Delay values: 40, 200, 400, 600, and 700 ns
3. Calibrations with *dReset* assertion at different moments
   - No dReset, end of read-out, beginning and end of read-out
4. Laser beam to see spurious signals

Calibration: 5000 events (without source) to compute
- Average
- Raw-sigma
- Sigma

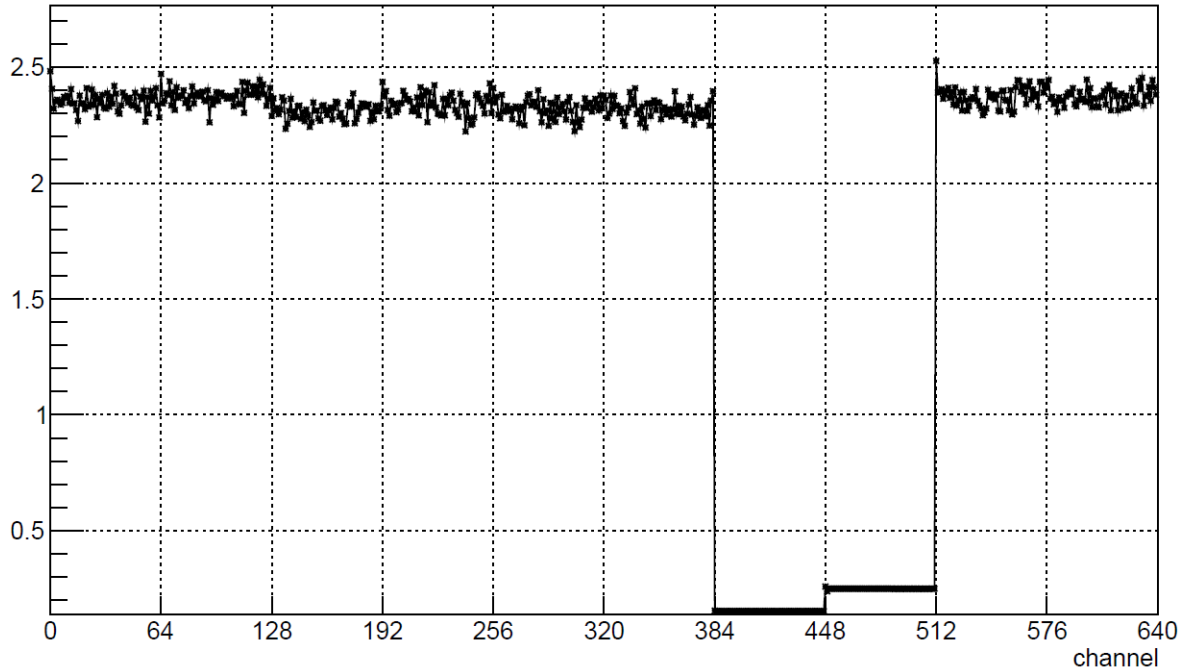
Reference: old GW

N.B.: the hole is a problem of the ADC Board

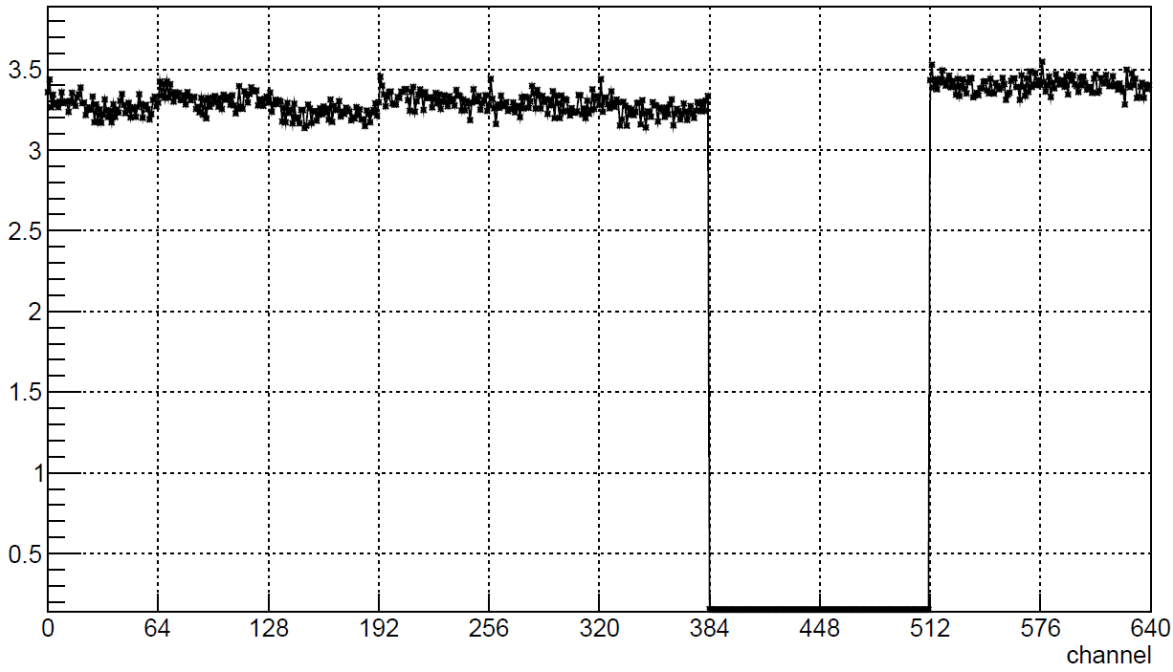
Pedestal



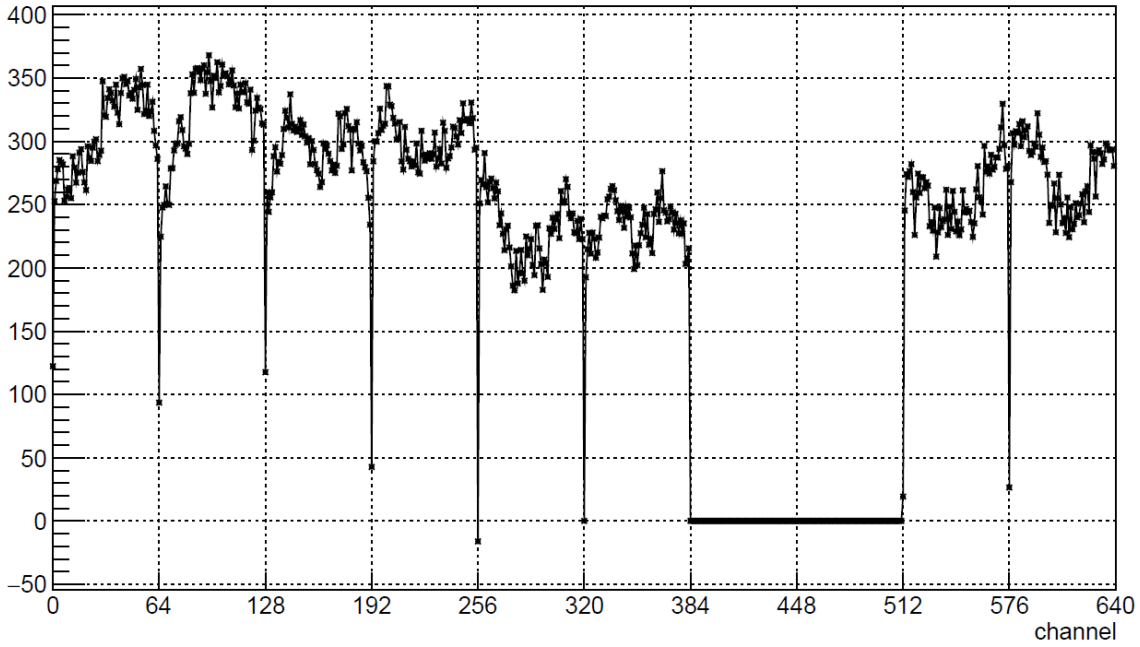
Sigma

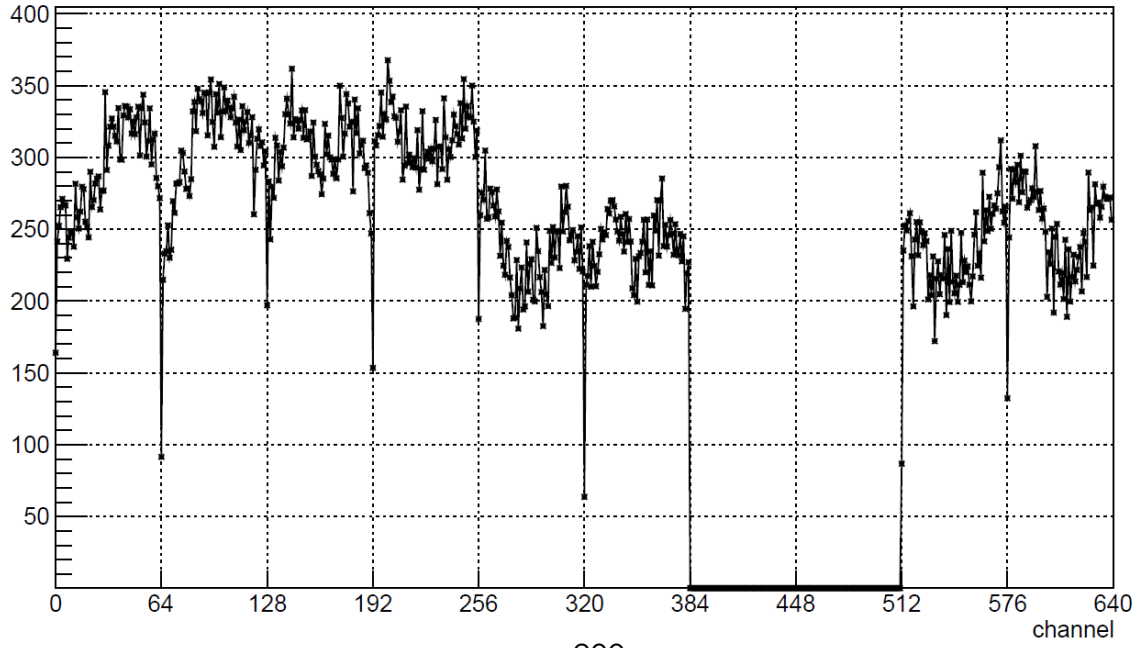


Raw-Sigma



2. ADC delay Coarse Scan: Average

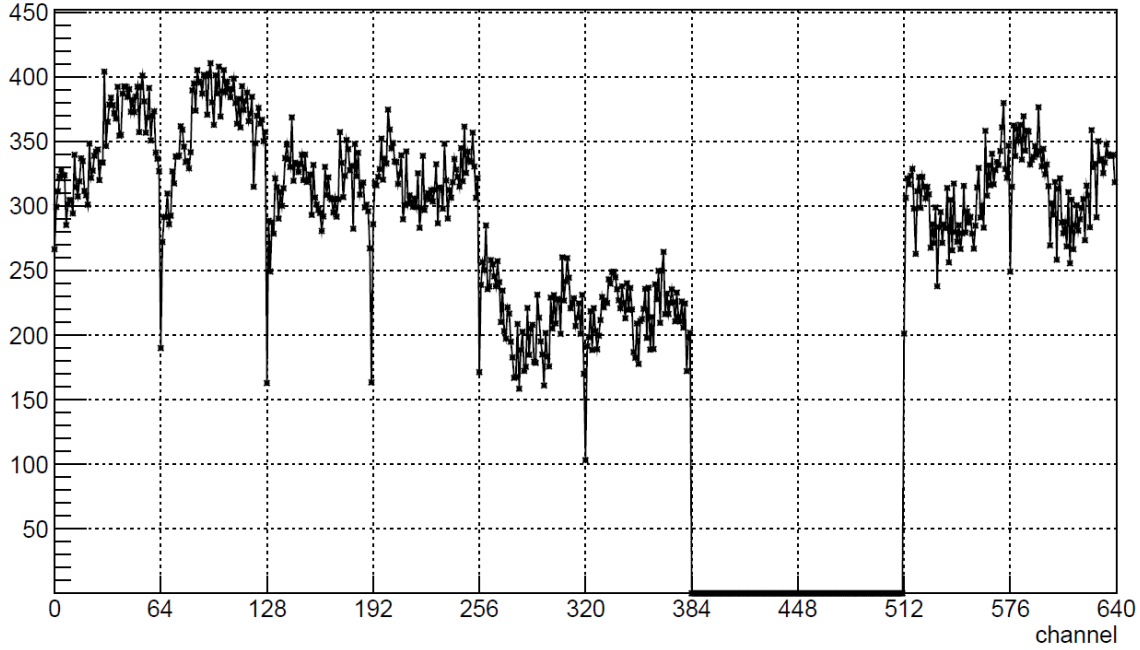


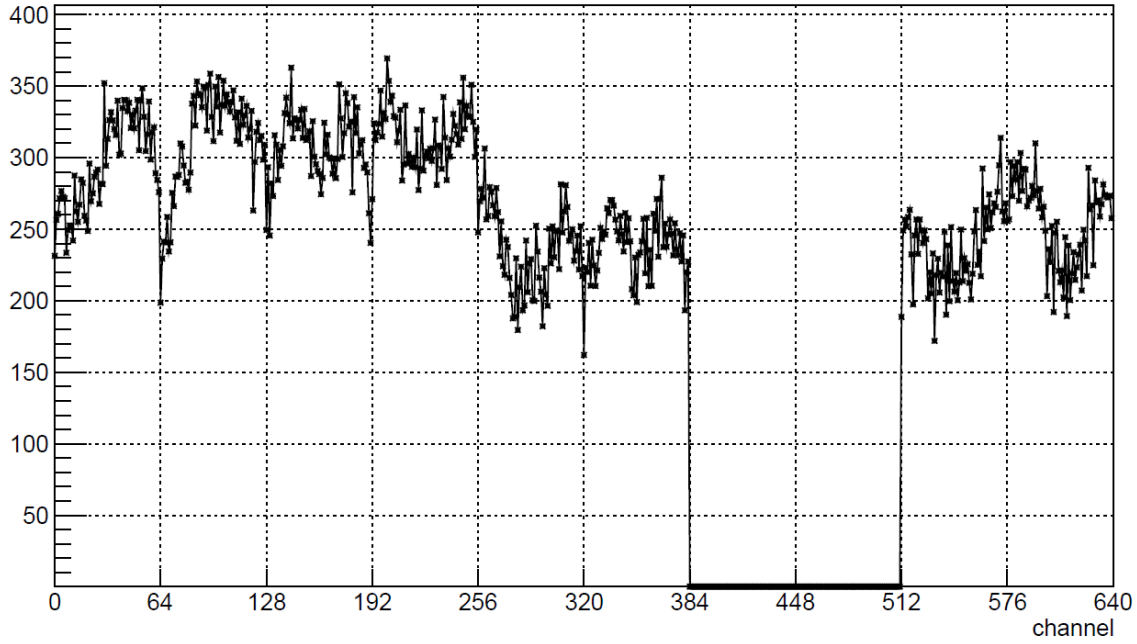


40 ns
400 ns

Pedestal Average

200 ns
600 ns





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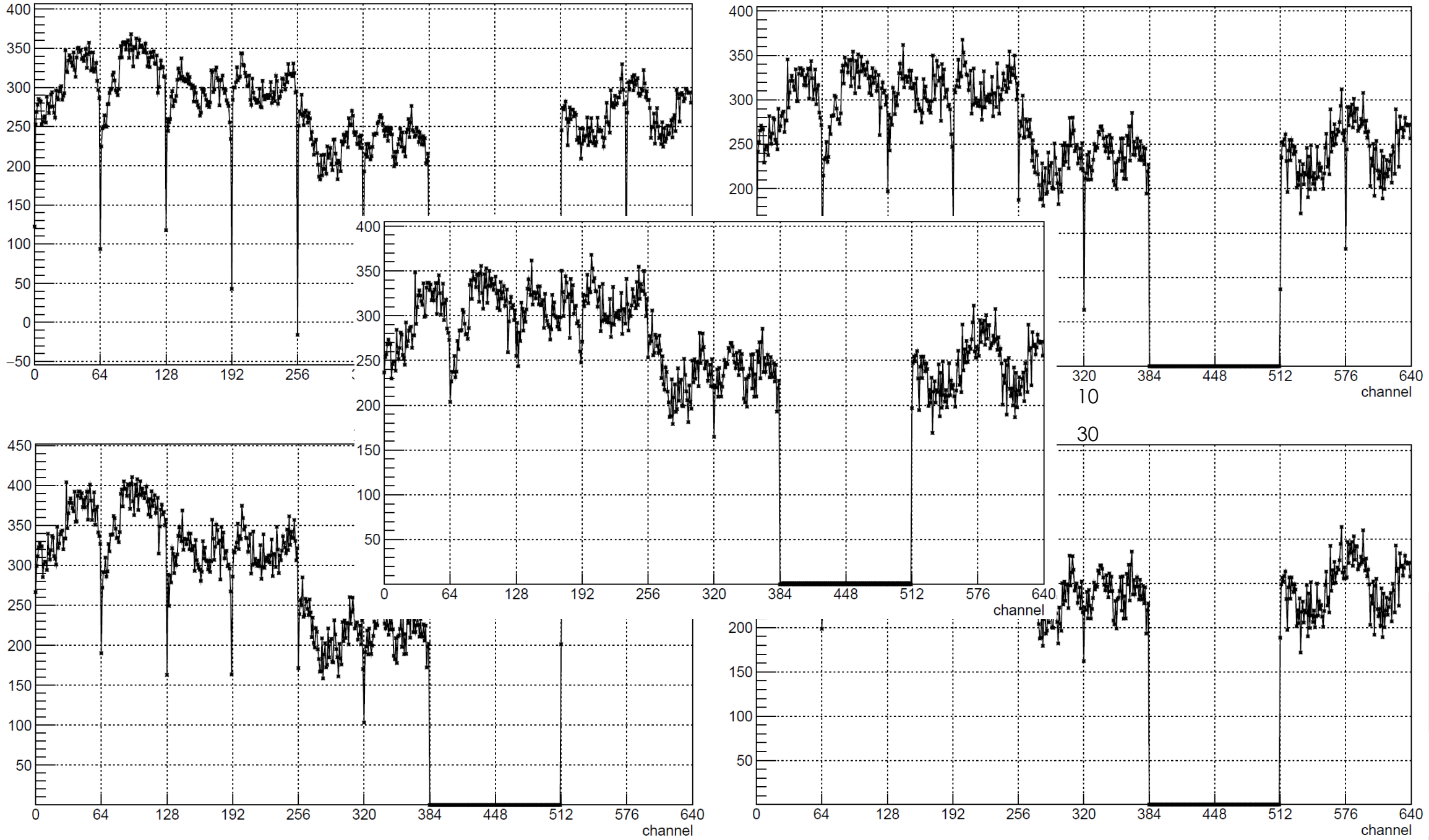
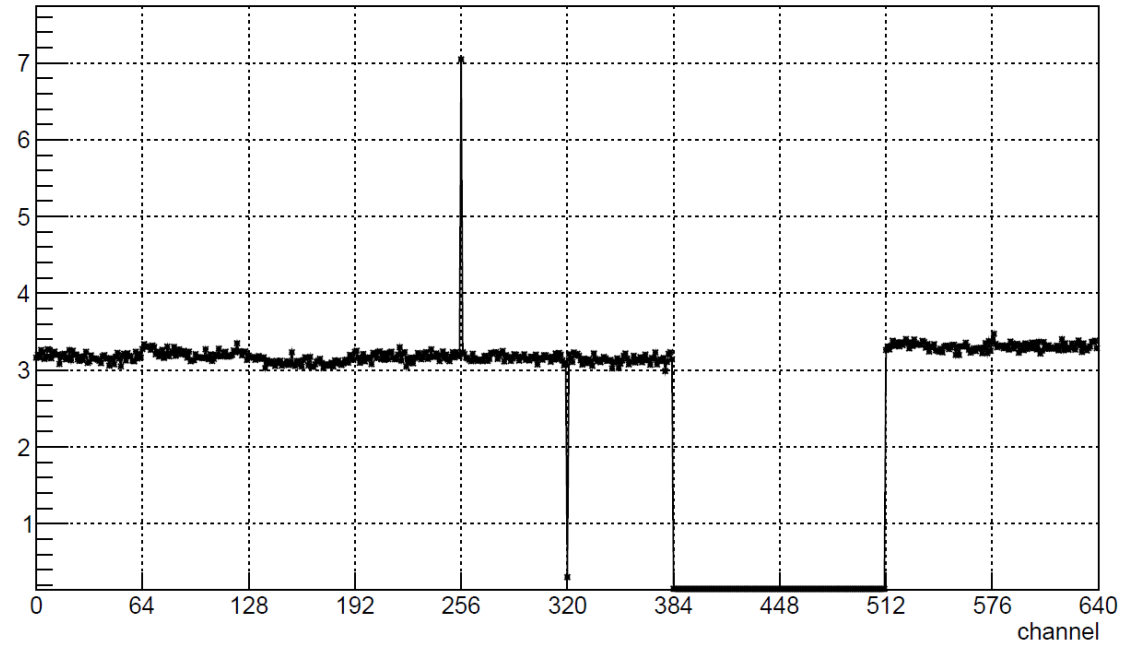
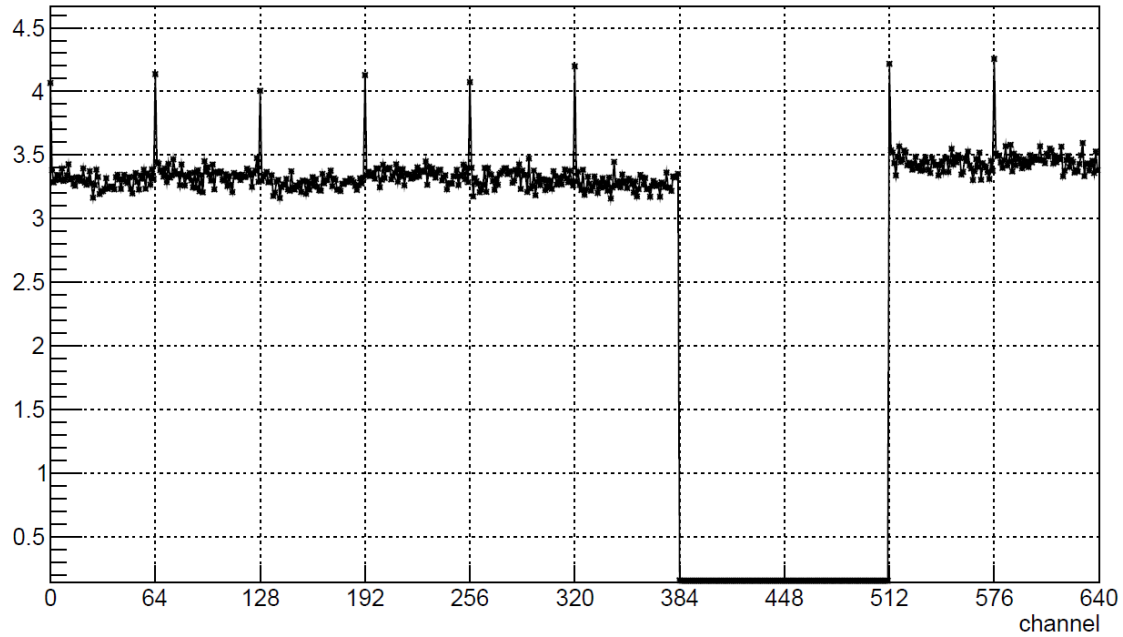


2. ADC Delay Coarse Scan: Raw Sigma

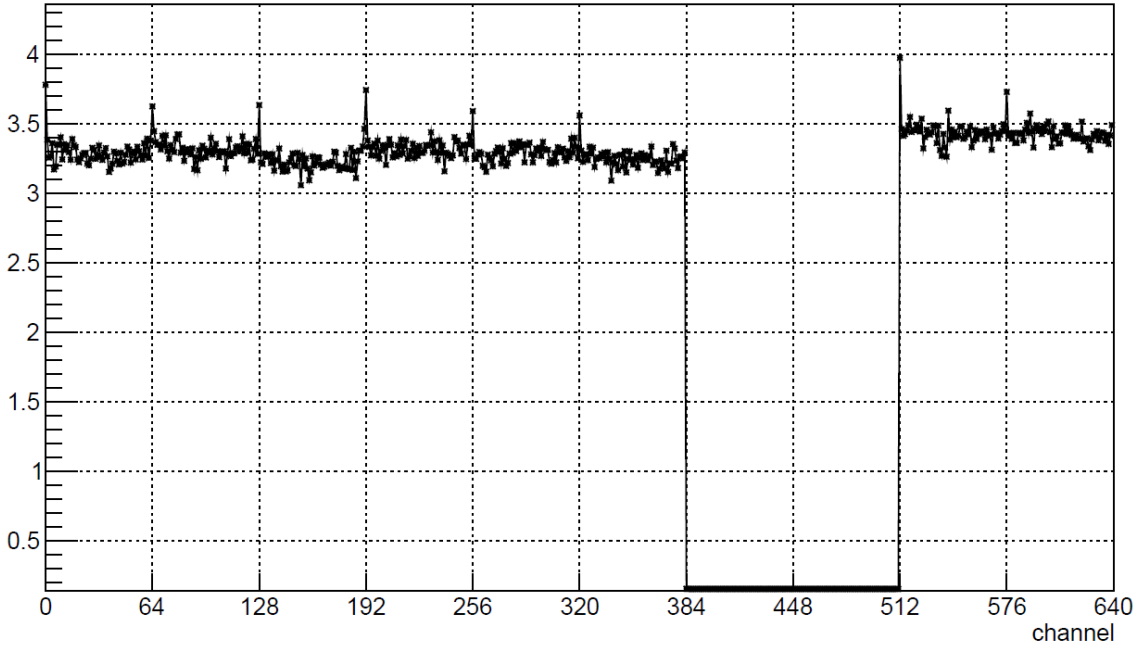


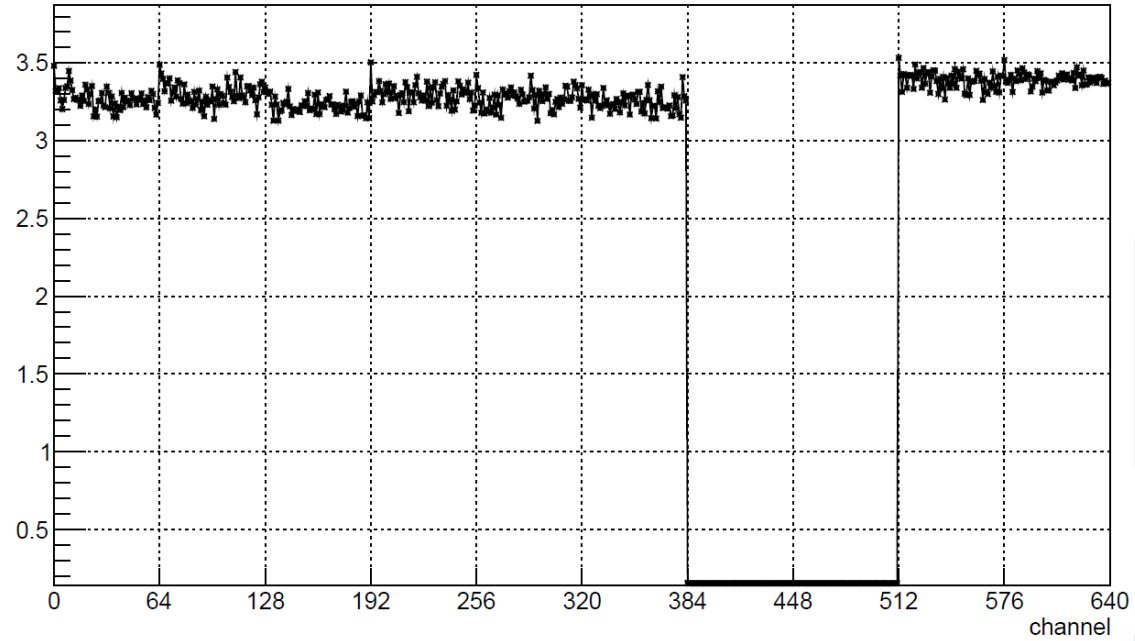


40 ns
400 ns

Pedestal Raw-Sigma

200 ns
600 ns





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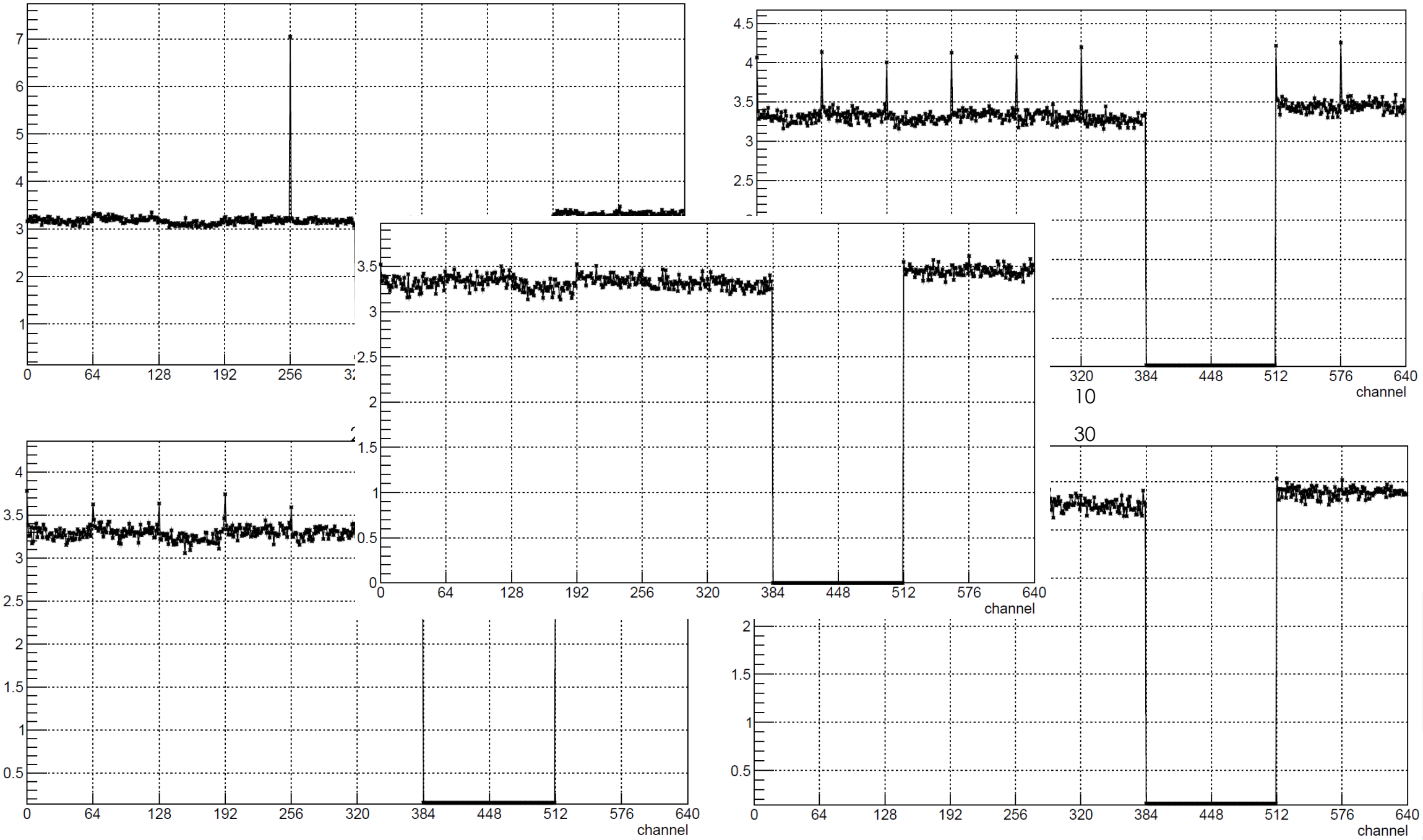
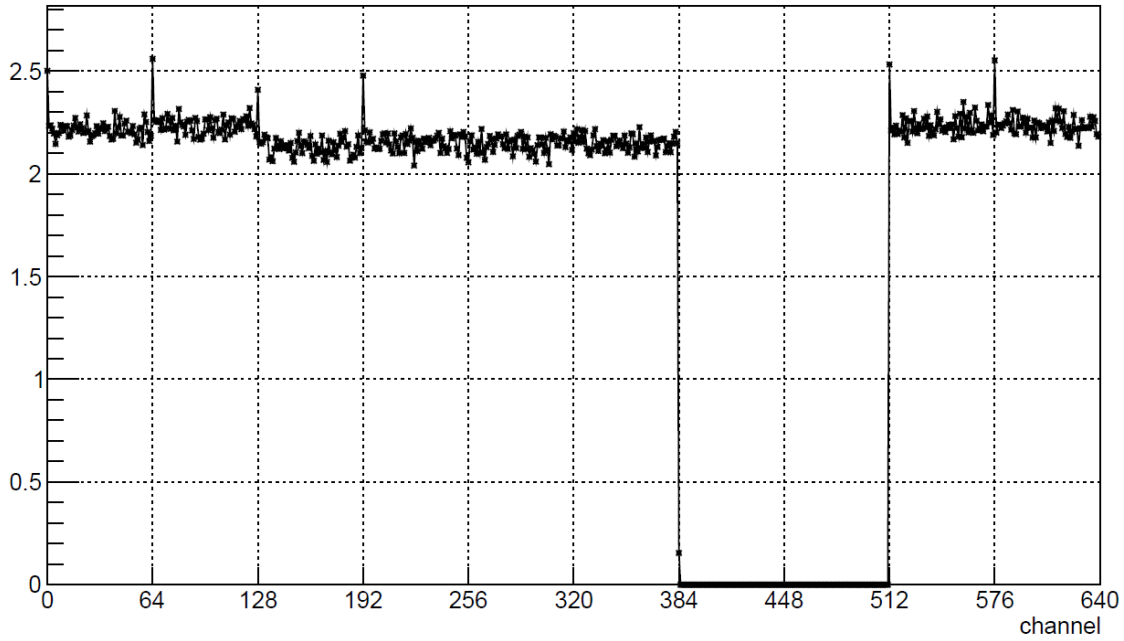
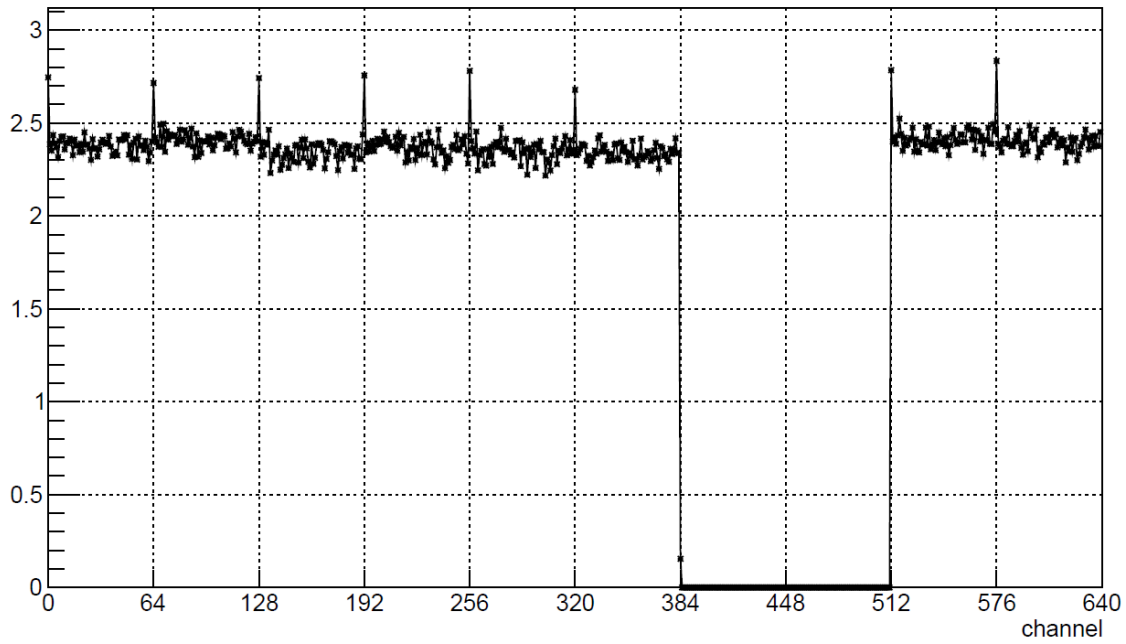


2. ADC Delay Coarse Scan: Sigma

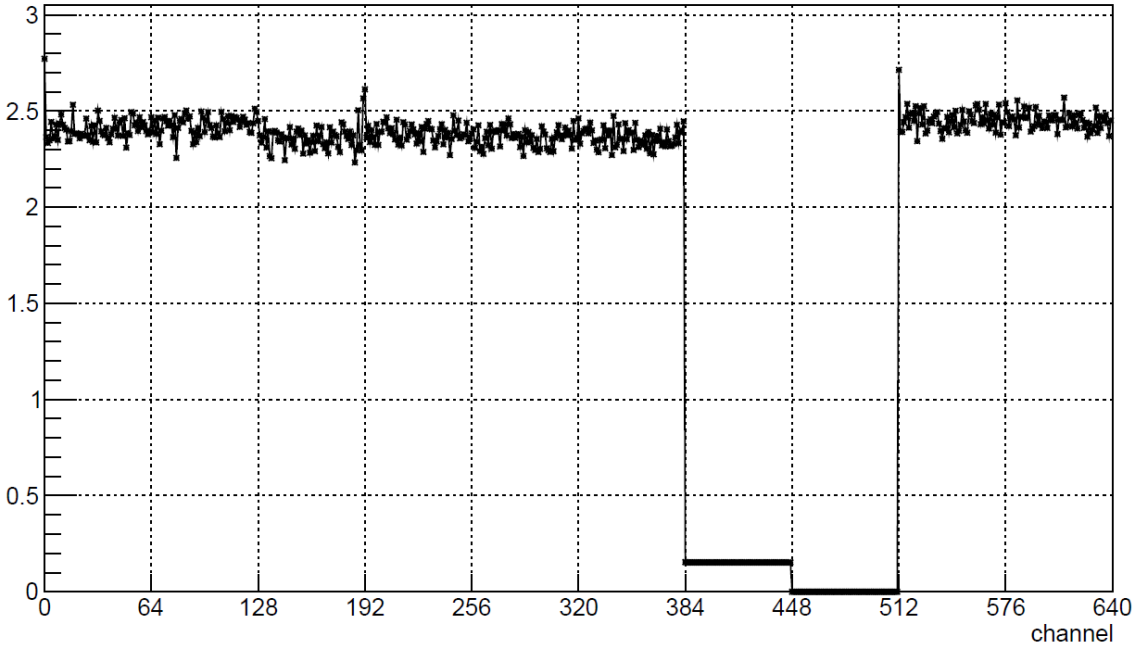


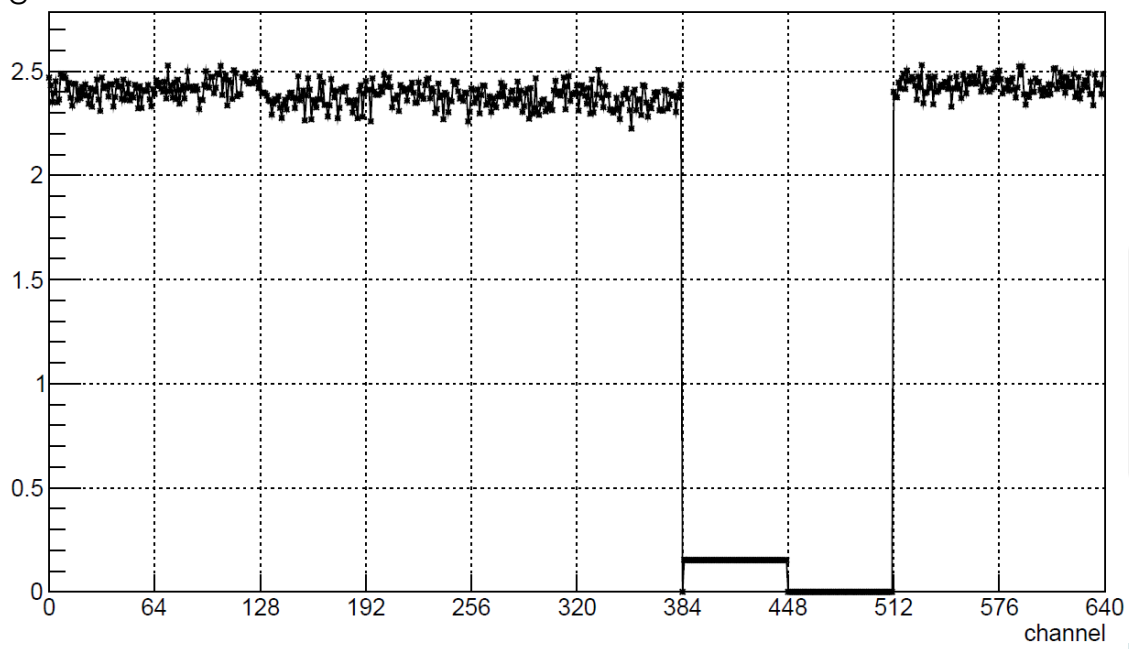


40 ns
400 ns

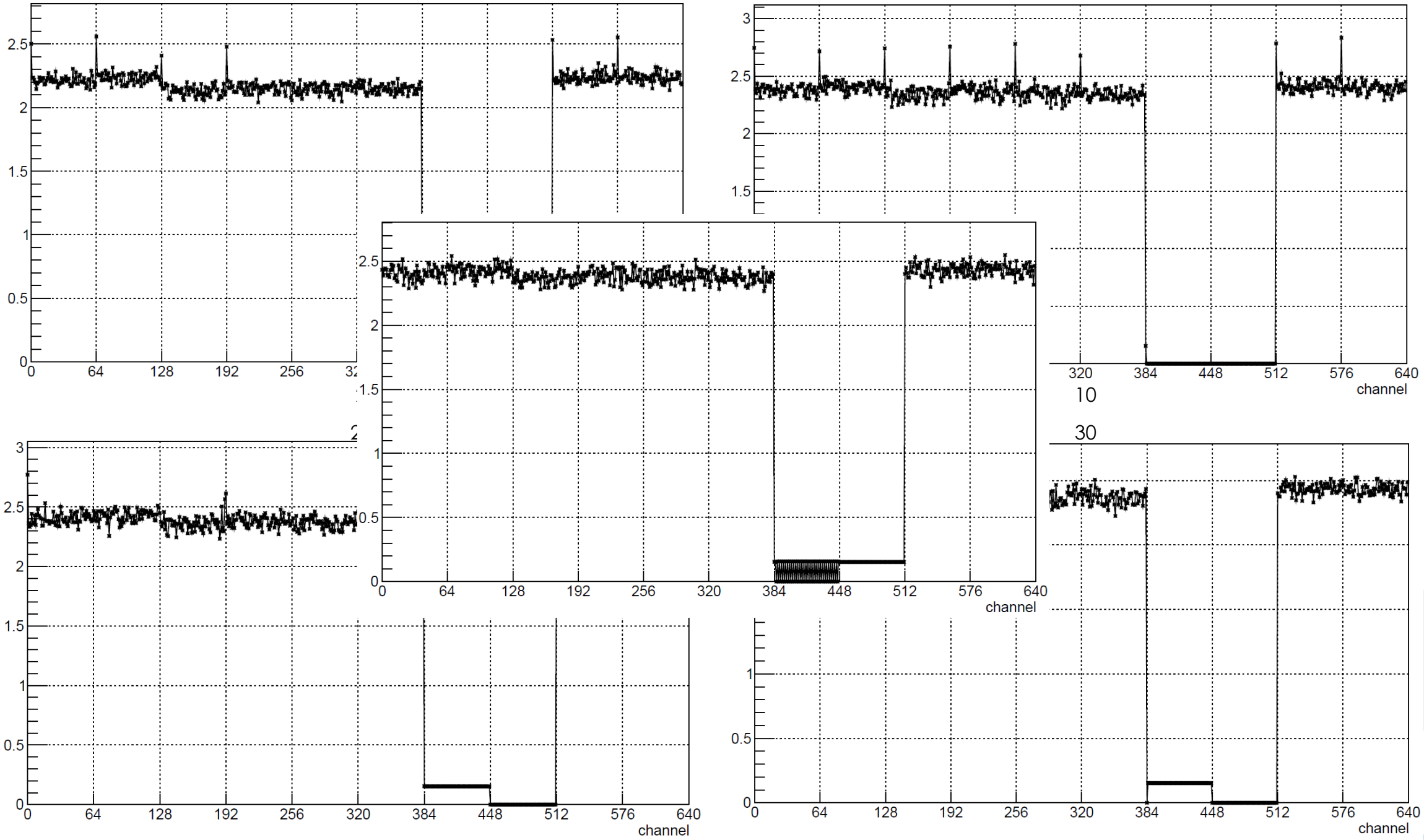
Pedestal Sigma

200 ns
600 ns

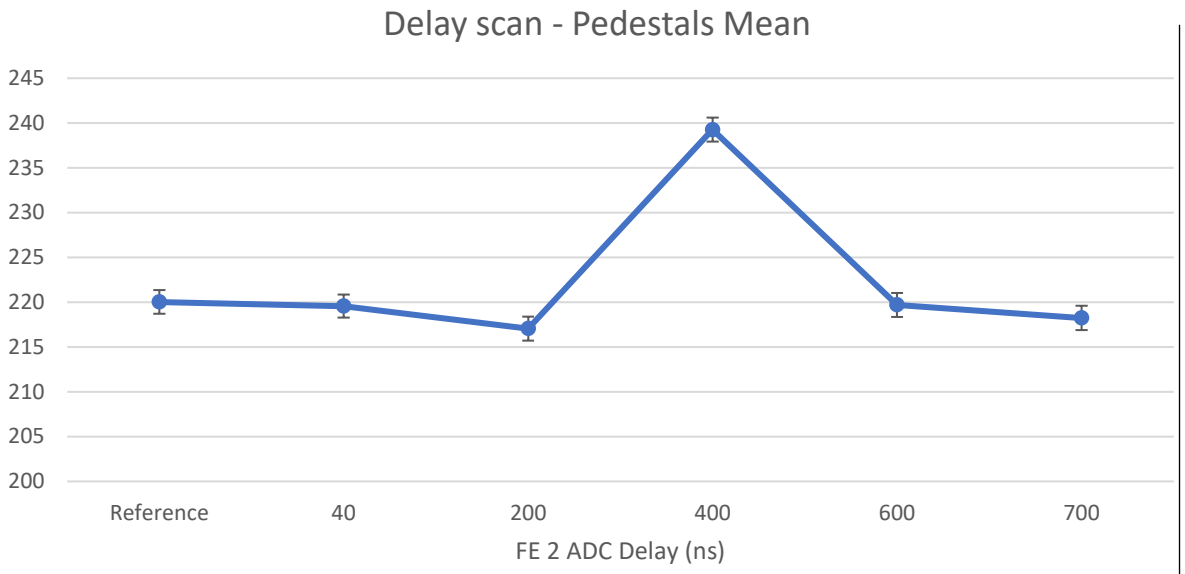


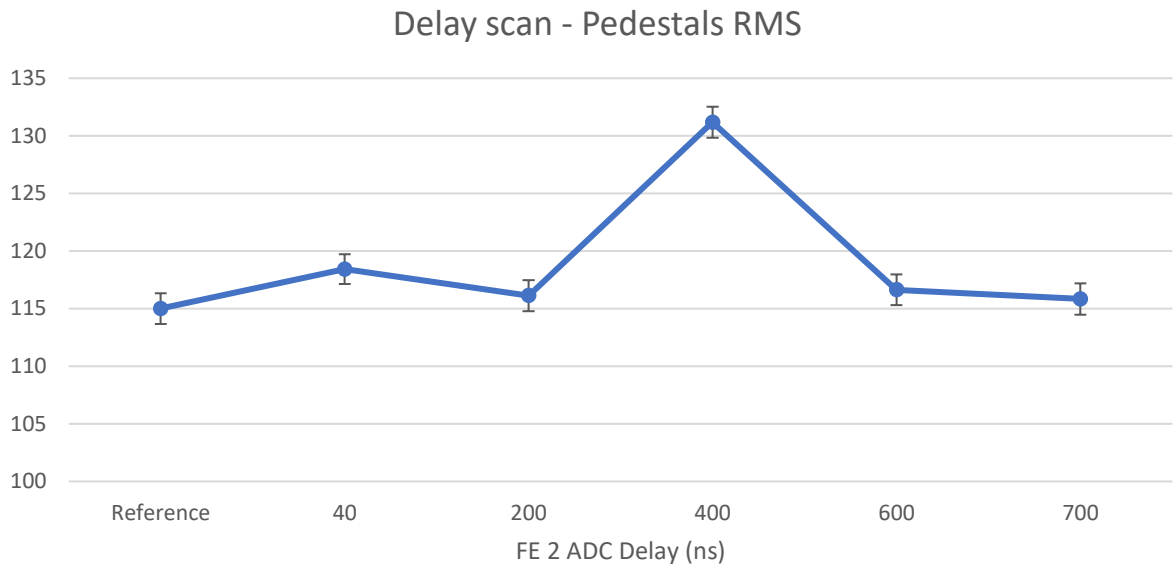


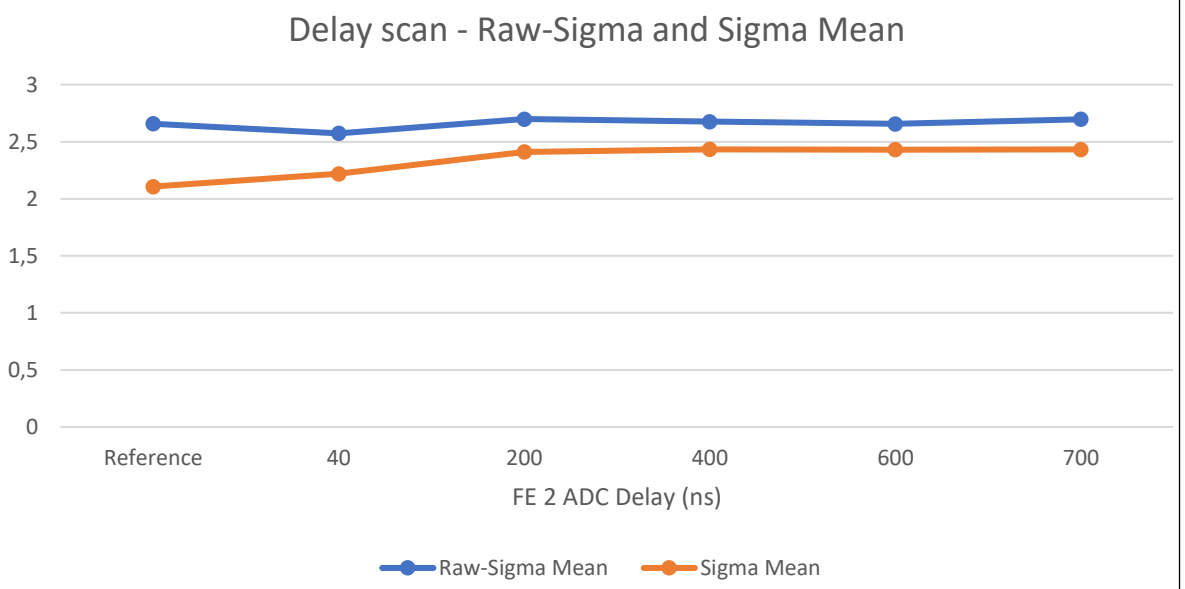
2. ADC Delay Coarse Scan: Sigma

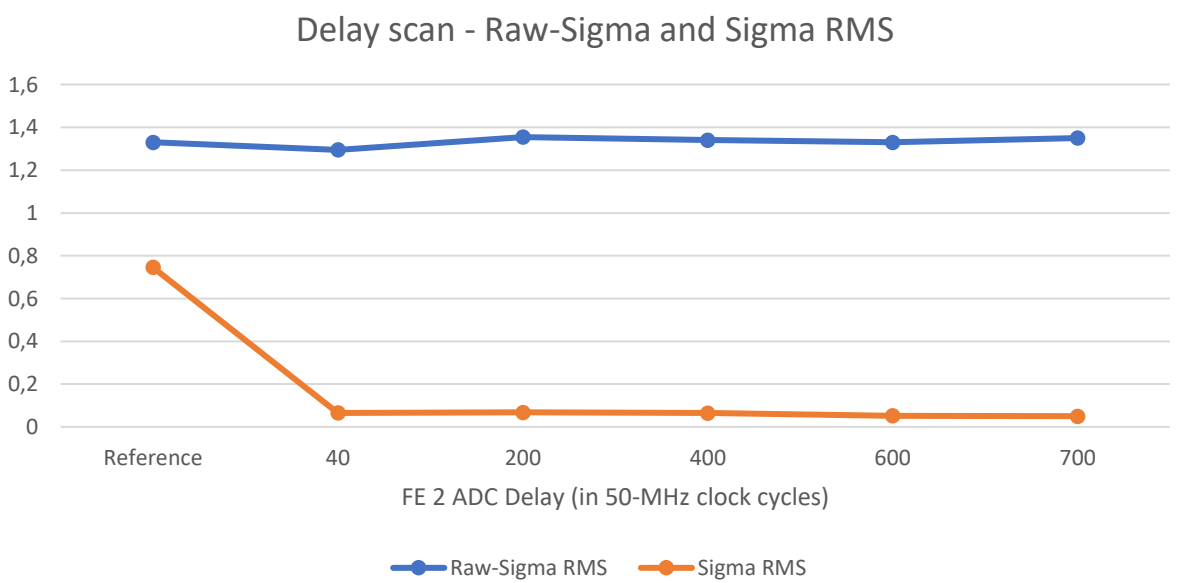


2. ADC Delay Coarse Scan

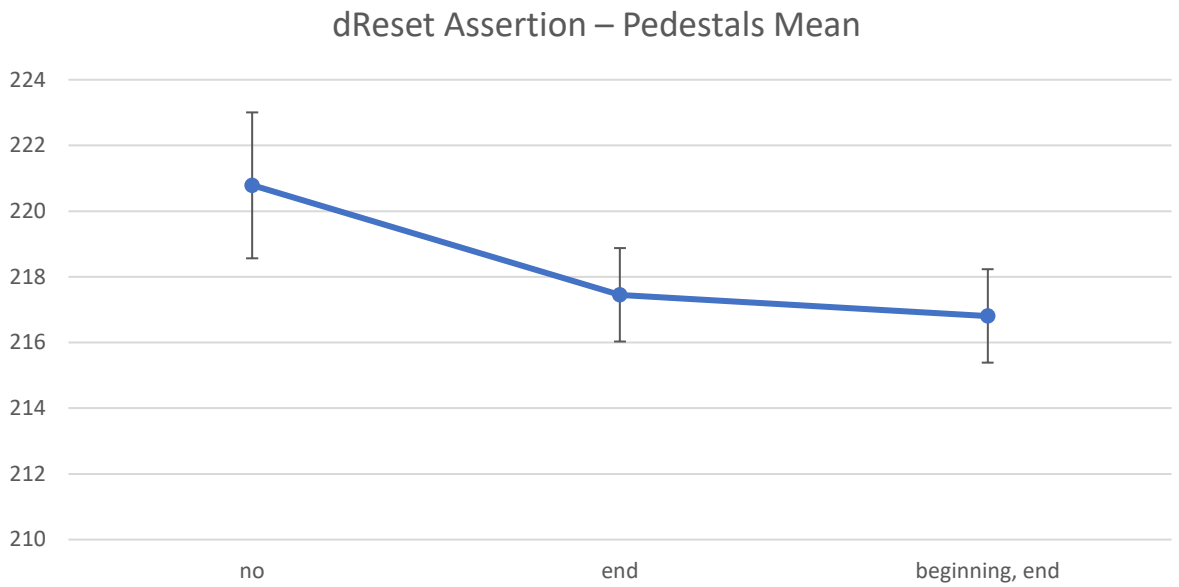


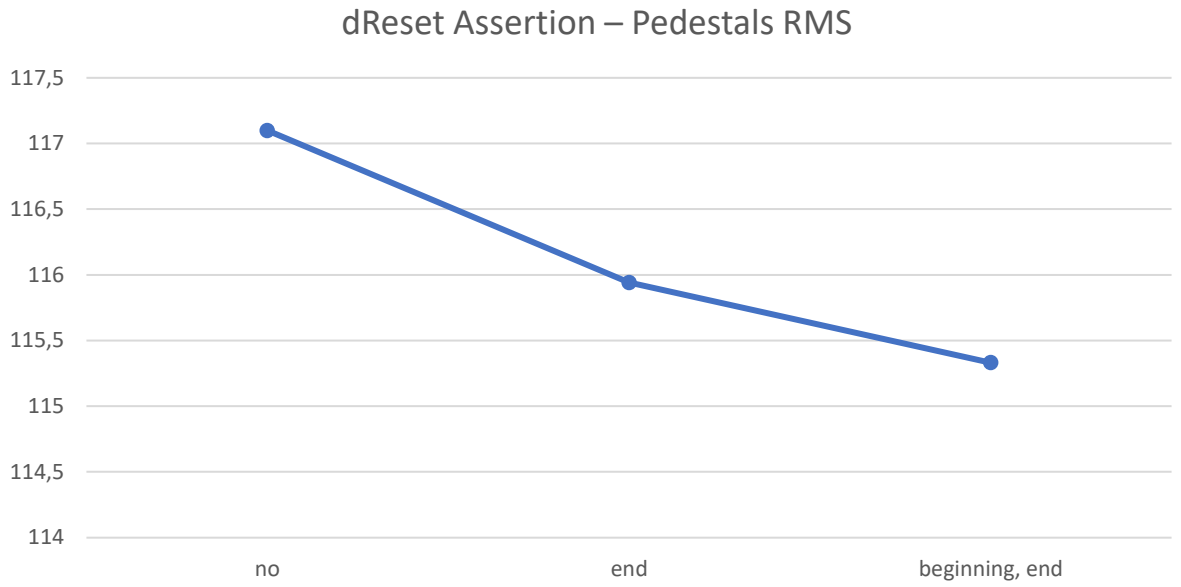


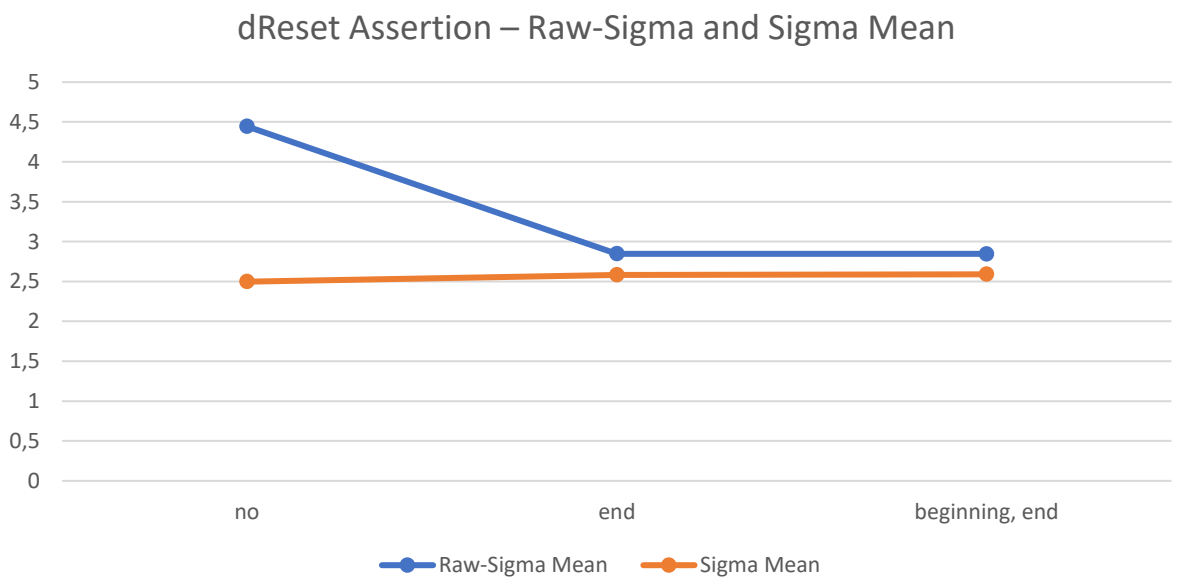


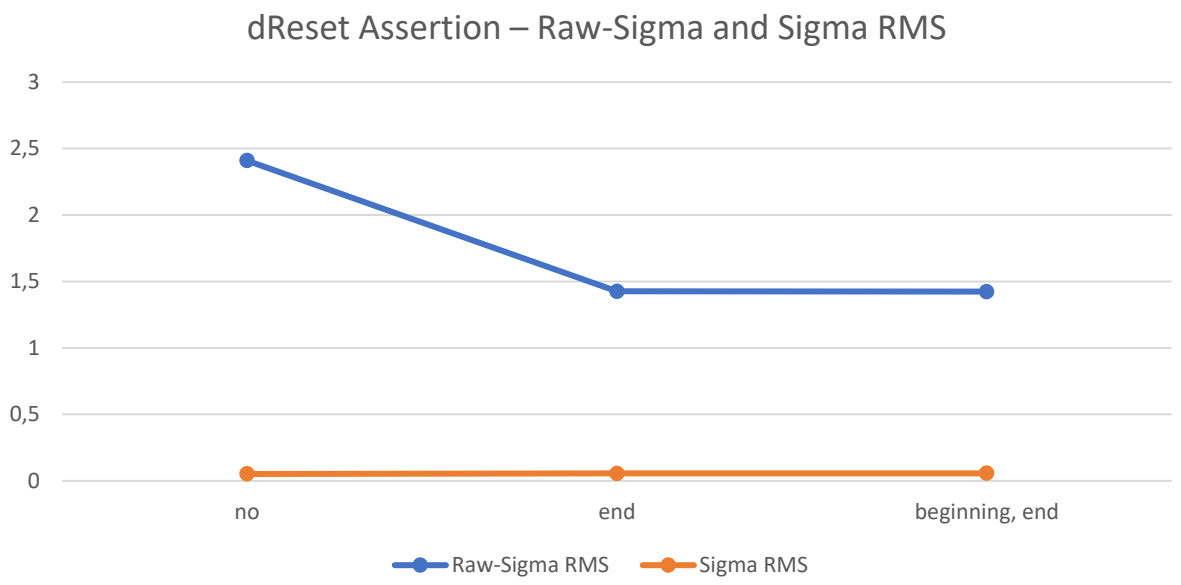


3. dReset Assertion



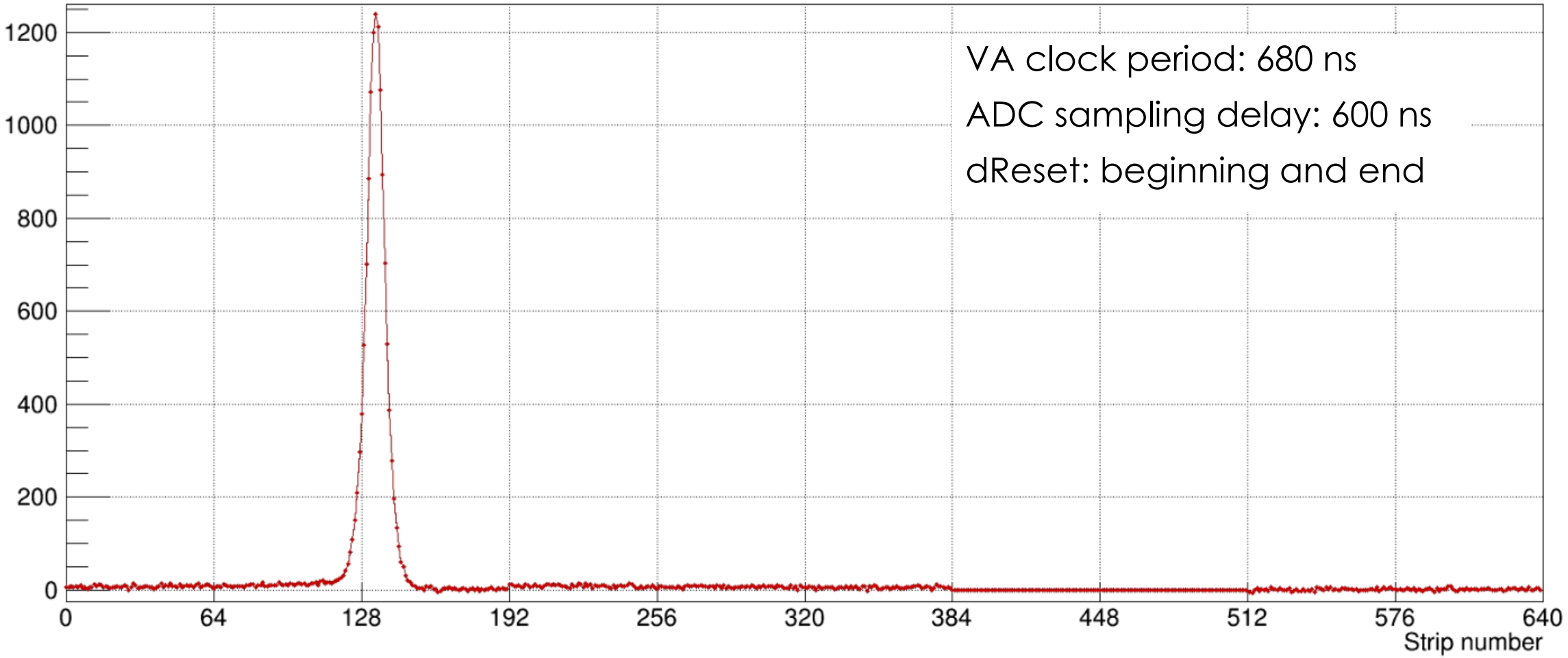






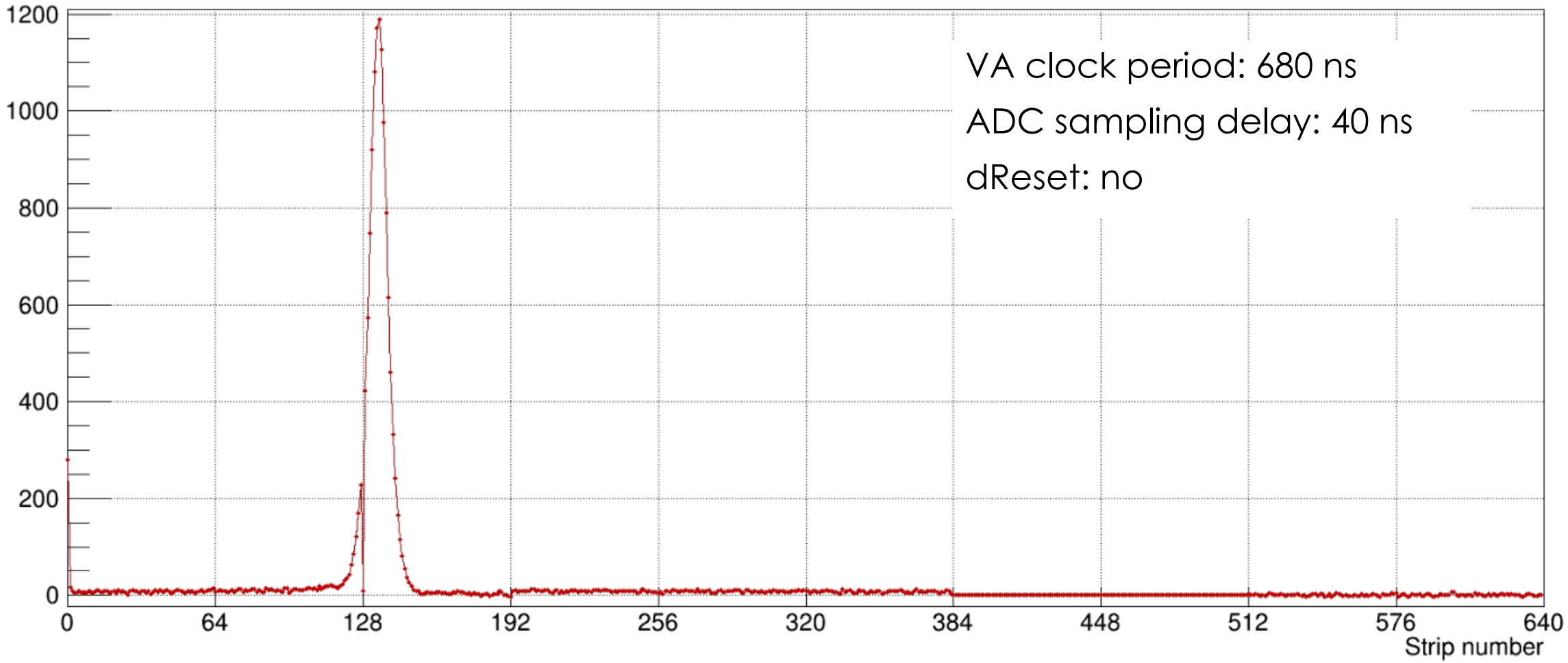
Laser Setup

1058 nm pulsed laser beam to see spurious signals and verify the functionality



Laser Setup: Comparison

Small ADC sampling delay and no dReset (to simulate the old GW)



Conclusions

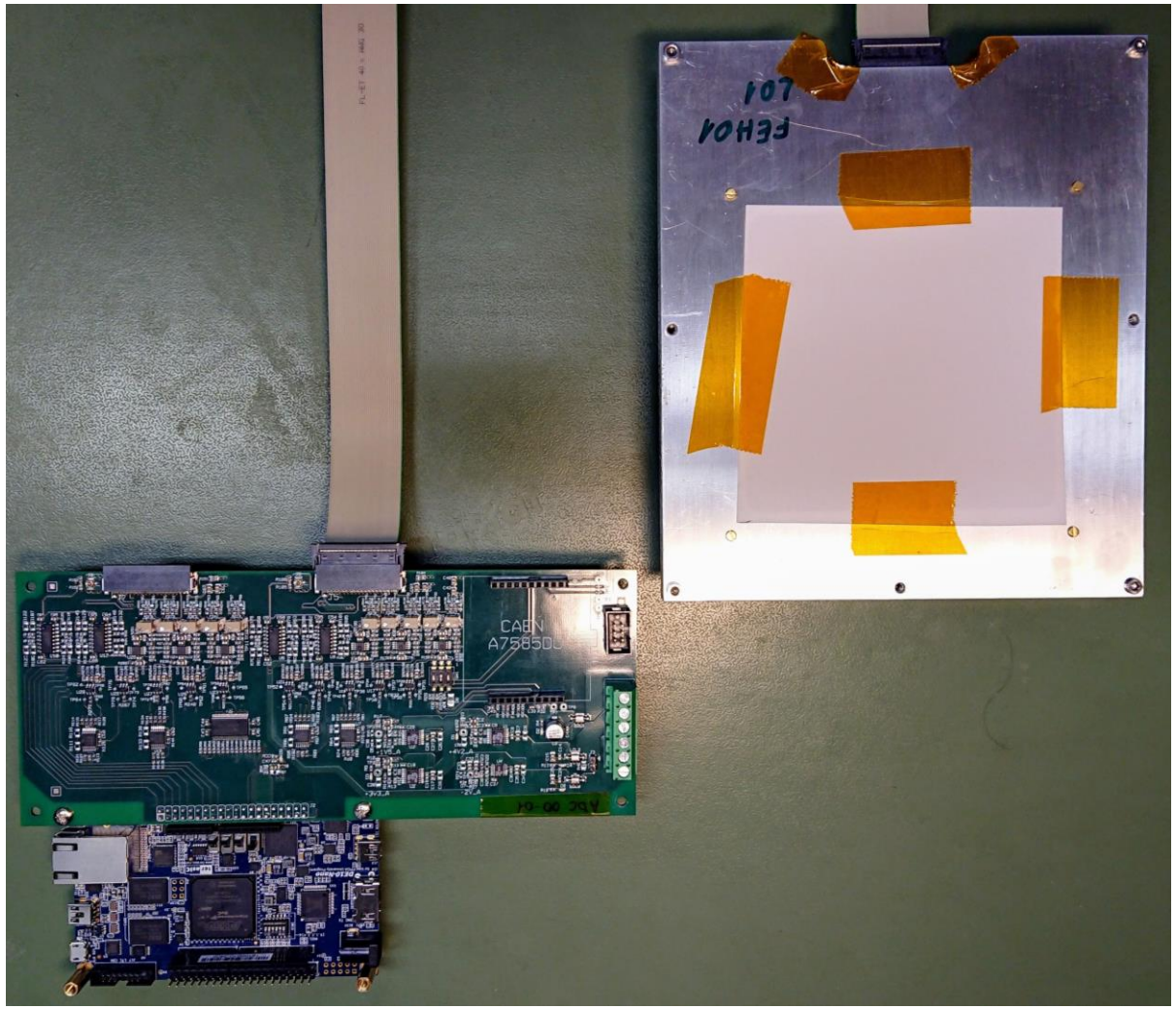
- New features implemented
  - Programmable delay between VA output and ADC sampling
  - dReset at the beginning and end of an event
  - AD7276 *Fast-mode* support

- Performed several scans to find optimal parameters
  - VA Clock: 1.47 MHz, 50% duty cycle
  - ADC Clock: 25 MHz, 50% duty cycle
  - ADC delay: 600 ns
  - 15% decrease in readout time per strip:
    - 800 ns (1.25 Msps) -> 680 ns (1.47 Msps):

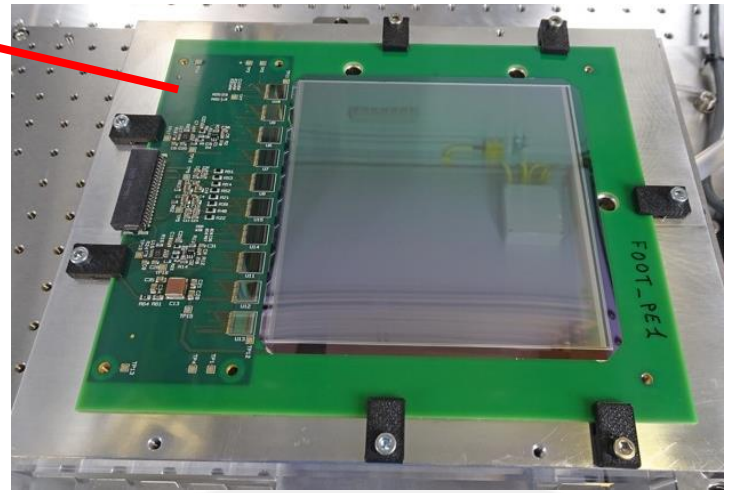
- No more spurious signals with laser setup

Study on last channels spurious signals

Actual setup

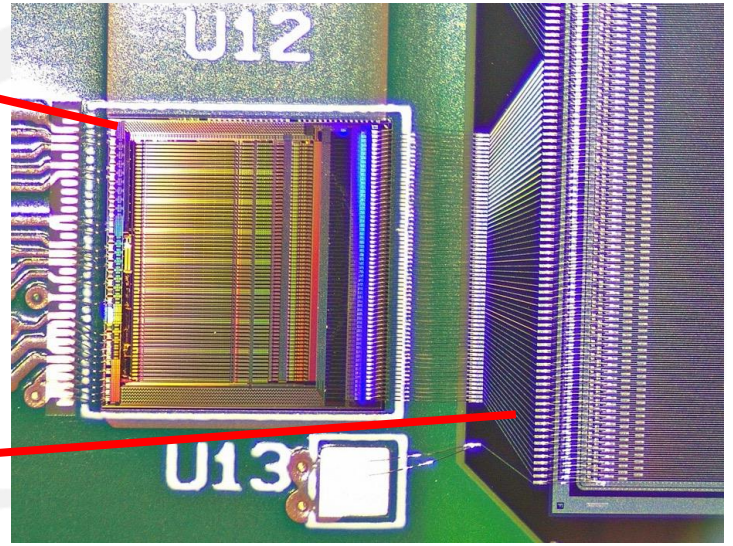


Hybrid Board

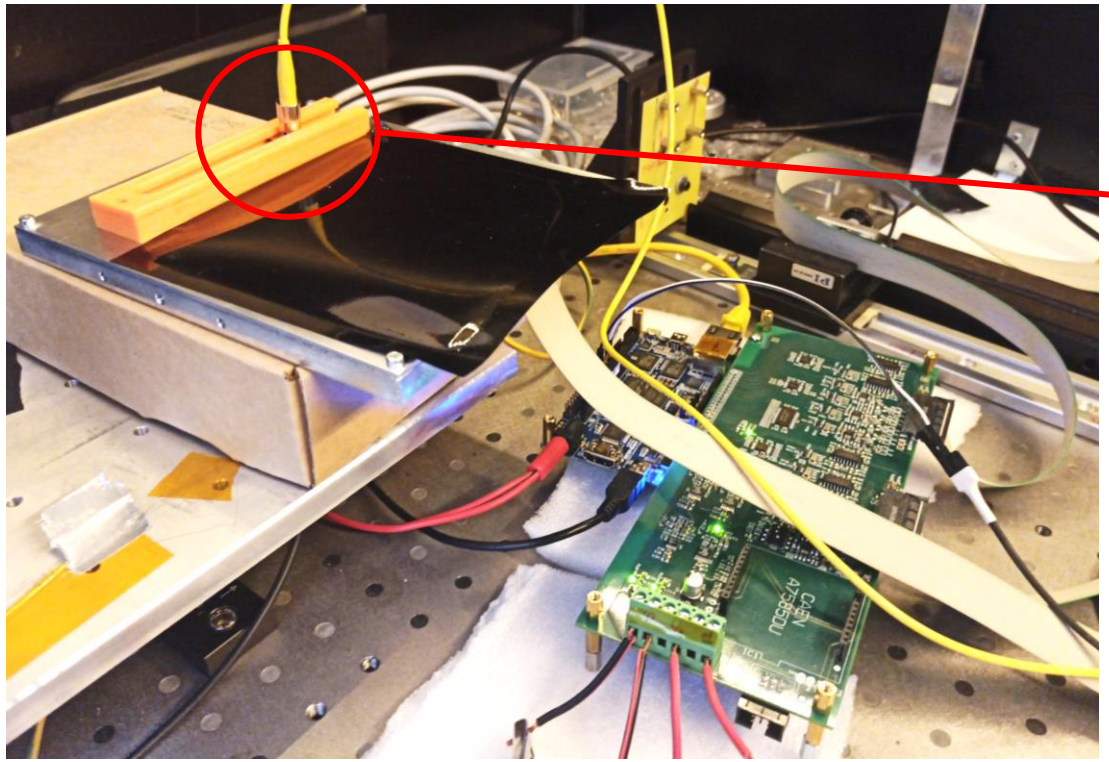


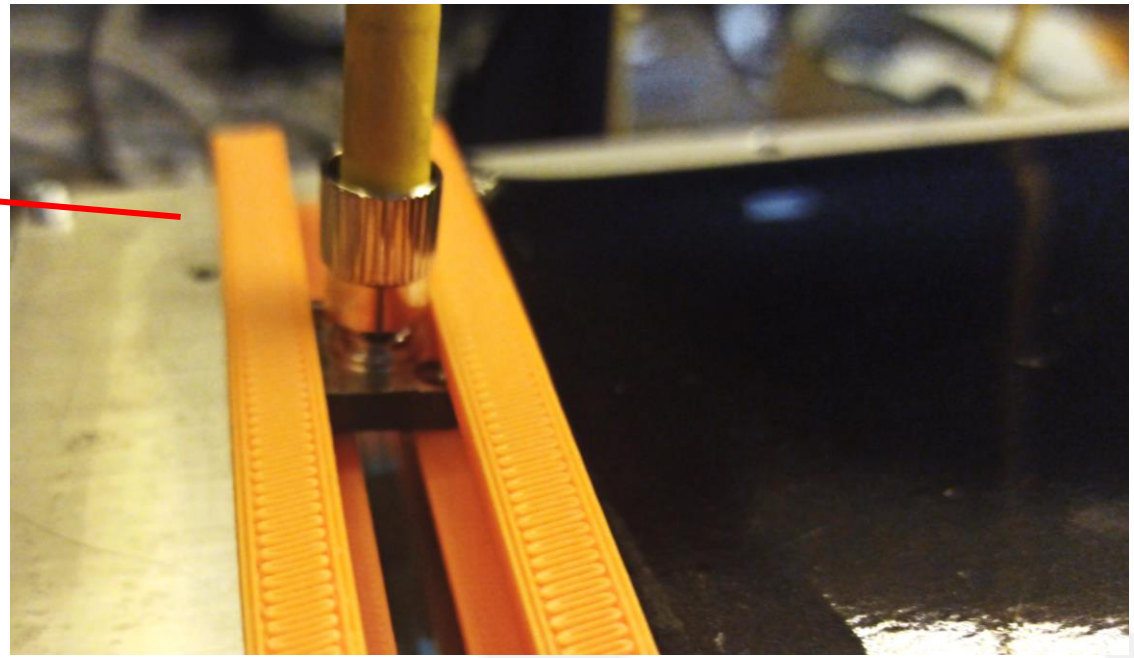
IDE1140 Front End

DET + Pitch Adapter



Laser Setup





- µS-Modules: FOOT L13
- GW settings:
  - ADC clock frequency: 25 MHz
  - ADC clock duty cycle: 50%
  - Artificial busy: 2.5 us

- Laser wavelength: 1058 nm
  - FE clock frequency: 1.47 MHz
  - FE clock duty cycle: 50%

Readout Operations: Daisy-Chain