FALAPHEL: Drivers

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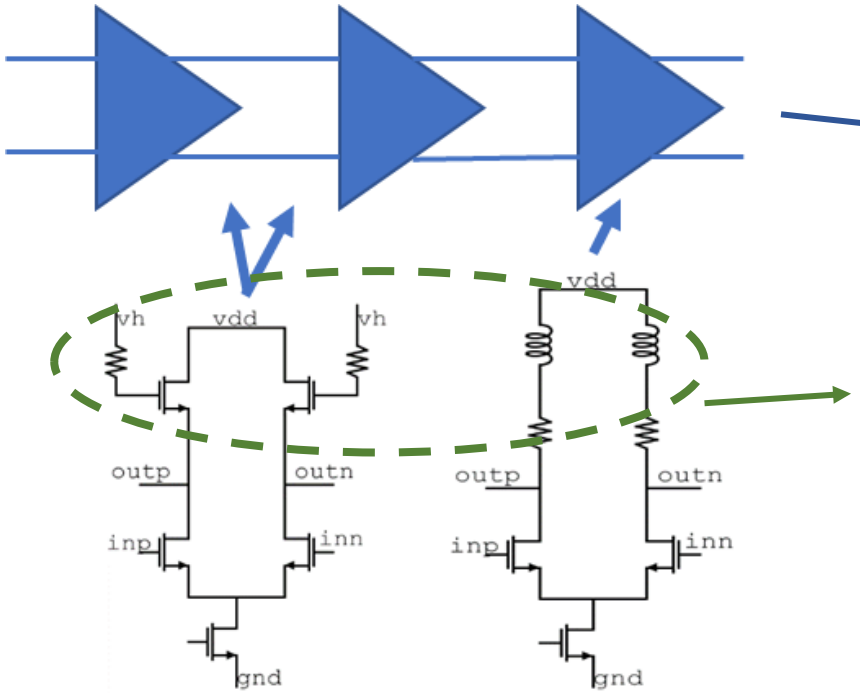
Drivers

- 25 Gb/s driver in 28 nm HPC for SiPh Ring Resonator
- 12.5 Gb/s CML driver in 28 nm HPC+ for SERDES
- 12.5 GHz clock receiver in 28 nm HPC+ for SERDES
- 25 Gb/s driver in 28 nm HPC+ for SiPh Ring Resonator

25 Gb/s Driver for RR in HPC-28 nm

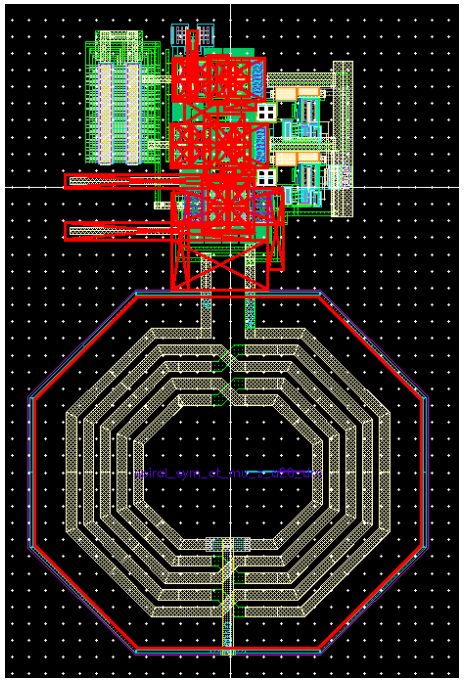
Old design submitted in December 2020, testing board designed in 2021, first tests performed in October 2021.

Driver for SiPh Ring Resonator device able to sustain 25 Gb/s



Three CML stages

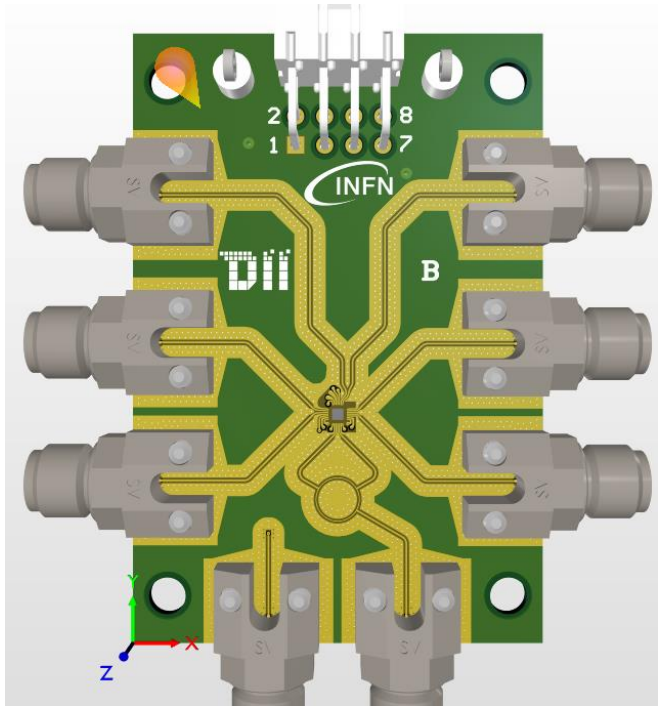
Passive and Active bandwidth enancement



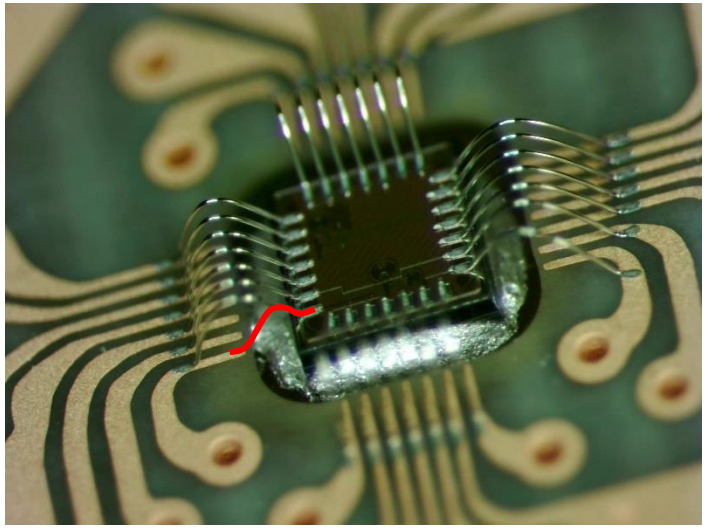
Layout of the 25 Gb/s driver in 28 nm

High-speed Board Design

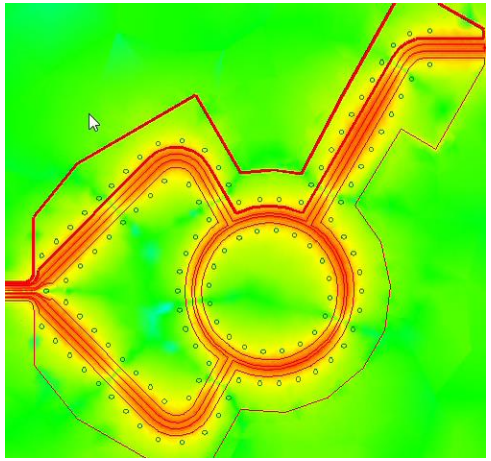
Great effort into the modeling of the SiPh devices but also into the testing board design



High-speed board with
2.92 mm connectors



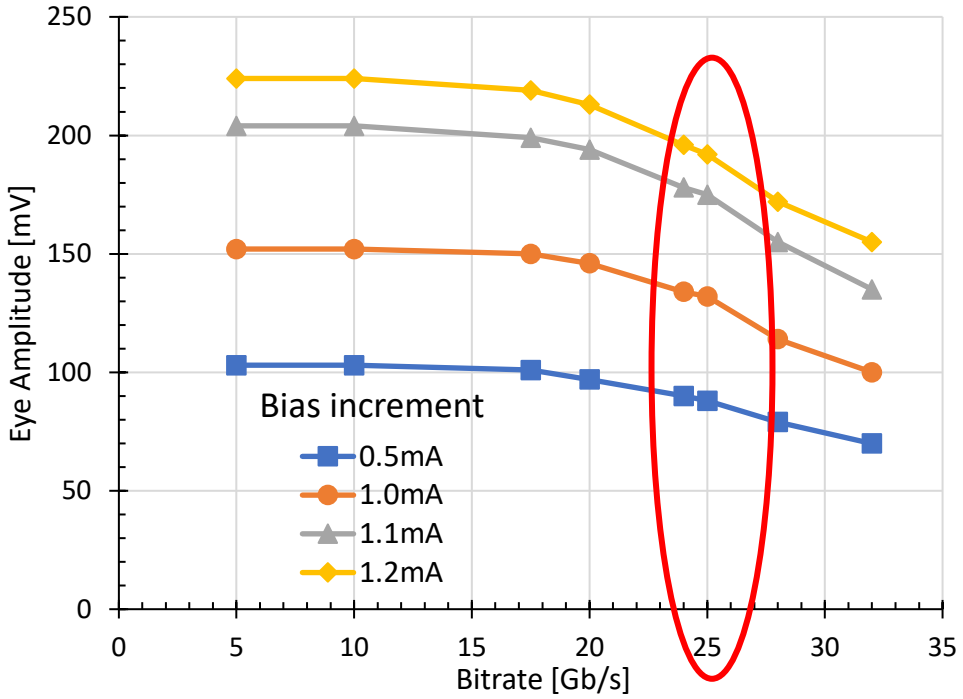
Board etch to reduce the bonding wire length
(bonding capability should be improved)



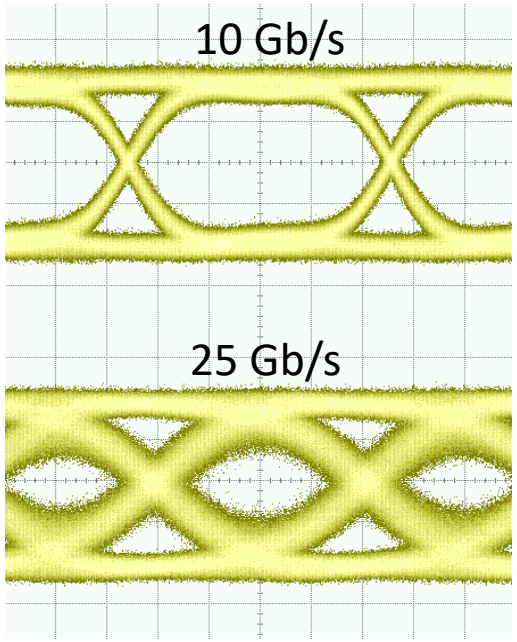
Electro-magnetic simulations

First Electrical Measurements-1

Electrical measurements of the HPC 28 nm driver

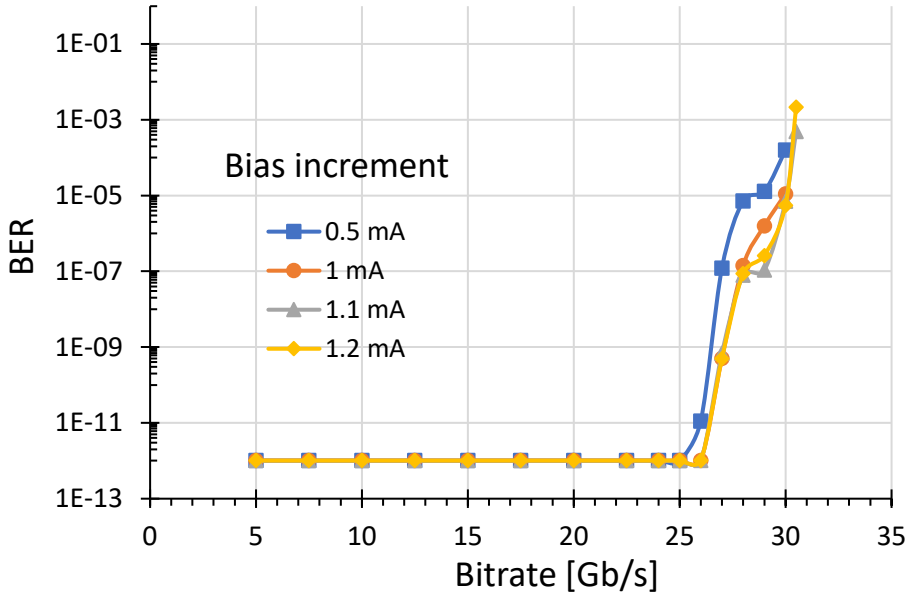


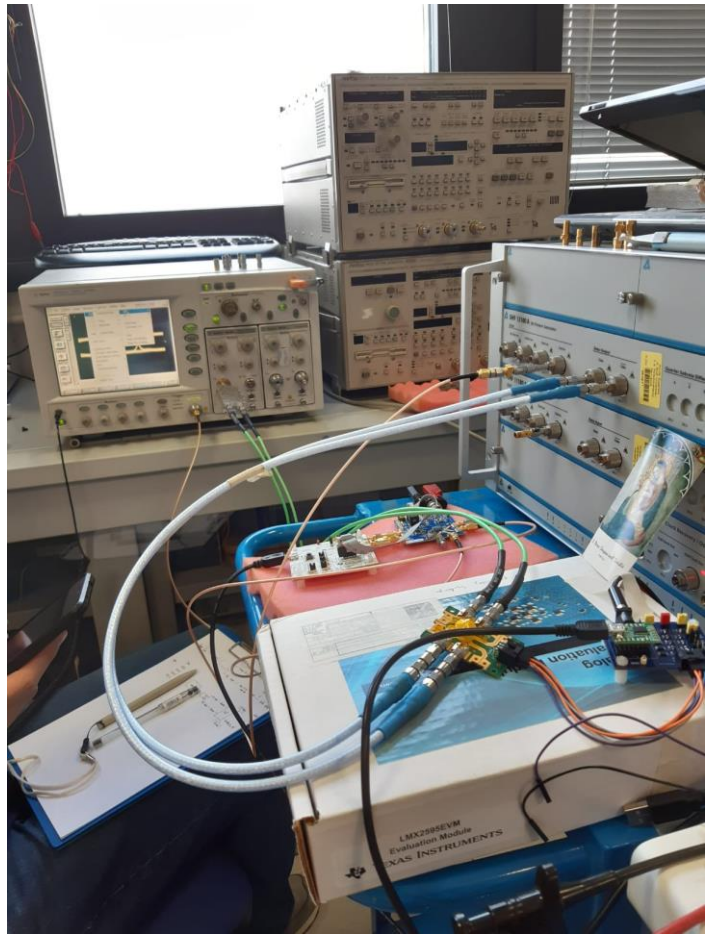
Voltage amplitude divided by a 4 factor (2 for load and 2 for Balun)



The first measurements on the 28 nm driver shown its ability to operate up 25 Gb/s

First Electrical Measurements-2

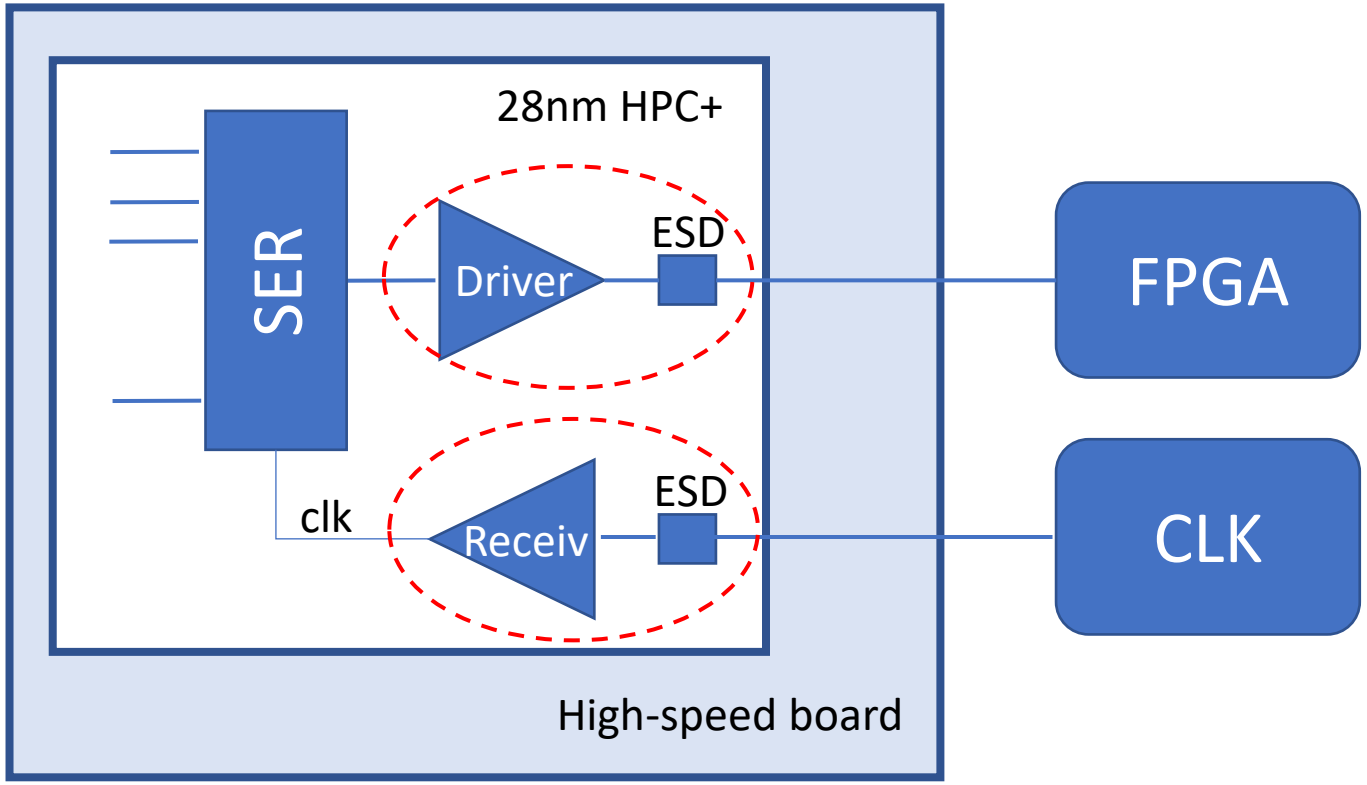




The electrical BER measurements on the HPC 28 nm driver show a value lower than 10^{-12} up to 25 Gb/s

What about radiation? Working in progress…

12.5 Gb/s CML driver in 28 nm HPC+

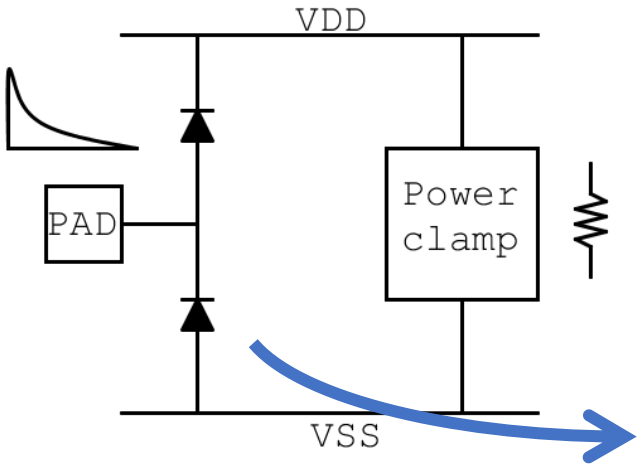


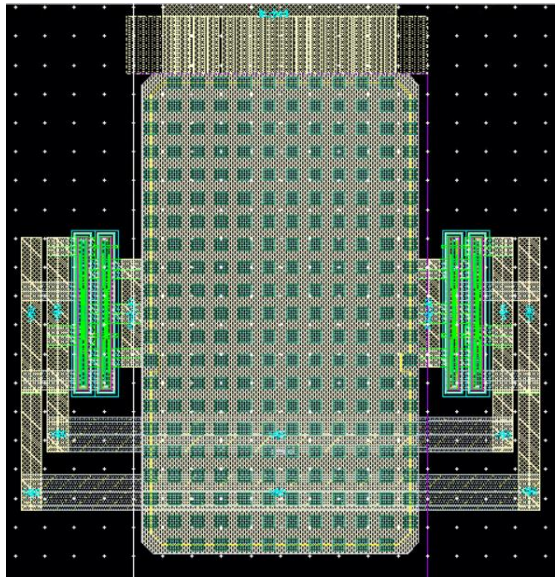
Followed approatch:

Translate the previous 25 Gb/s driver to the HPC+ technology and check its operability

High-speed ESD in HPC+

Translate the custom ESD protections designed in HPC to the HPC+ technology





In-house

- 1 kV HBM ESD with low capacitance (160-200 fF)
- Low resistance Power clamps

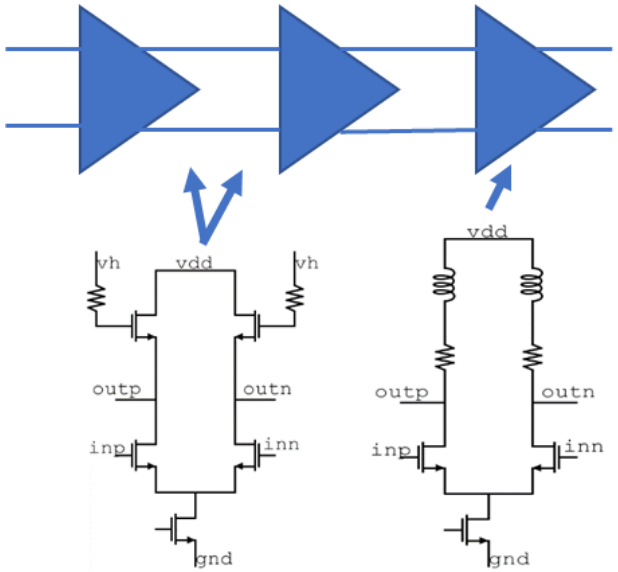
The HPC+ technology held by INFN has its own PADs and ESDs for power and low speed (Guido)

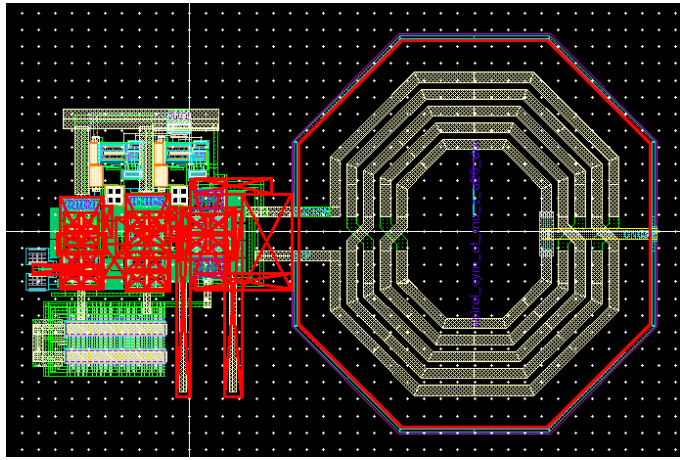
- High-speed ESD only where it is required

Note: Power clamps in HPC have some problems

12.5 Gb/s CML driver in 28 nm HPC+

Same driver's structure of HPC

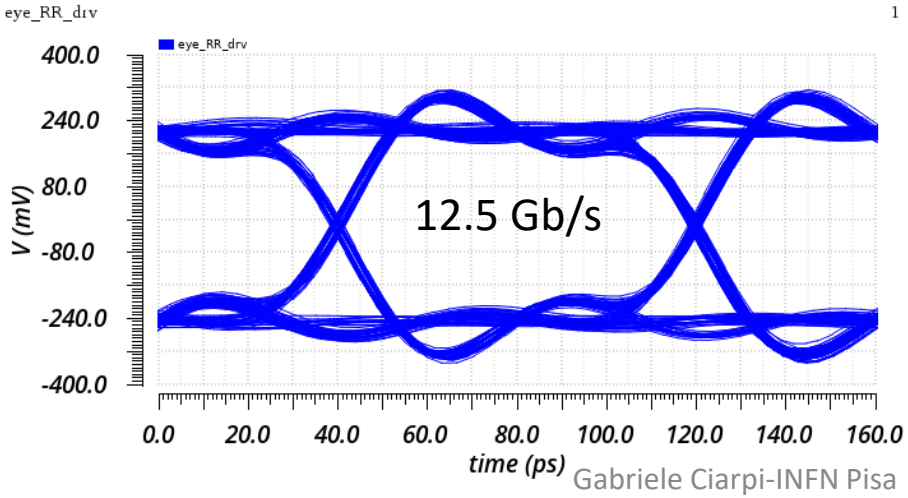




There is still work to be done

- Maximum input capacitance?
- Remove the active peaking?
- Traslate into INFN tech

Simulation of the output signals considering the FPGA loading

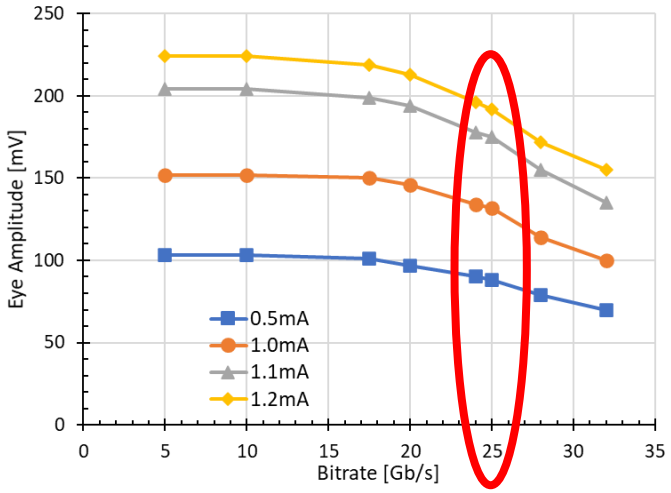


12.5 GHz clock receiver in 28 nm HPC+

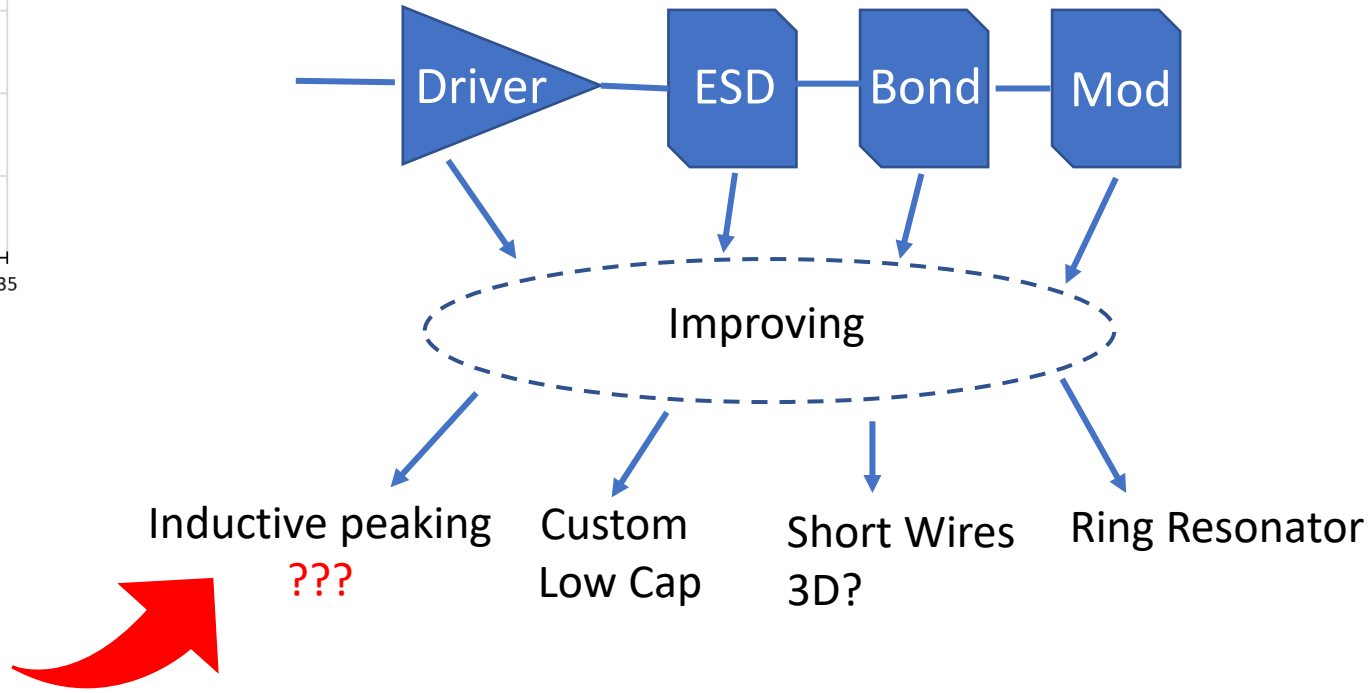
Working in progress…

25 Gb/s driver in 28 nm HPC+

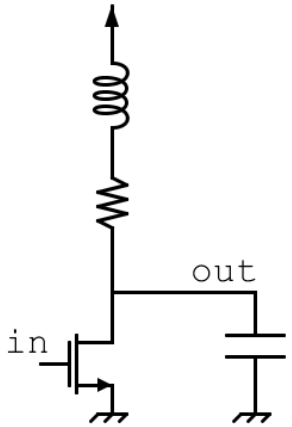
HPC driver results



How can we improve the driver bandwidth?
Which is the main limitation of driver bandwidth?

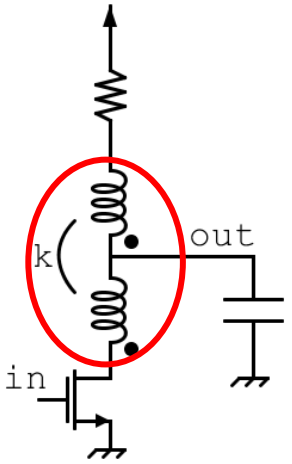


Other bandwidth extension techs



Inductive peaking

BWER ≈ 1.72

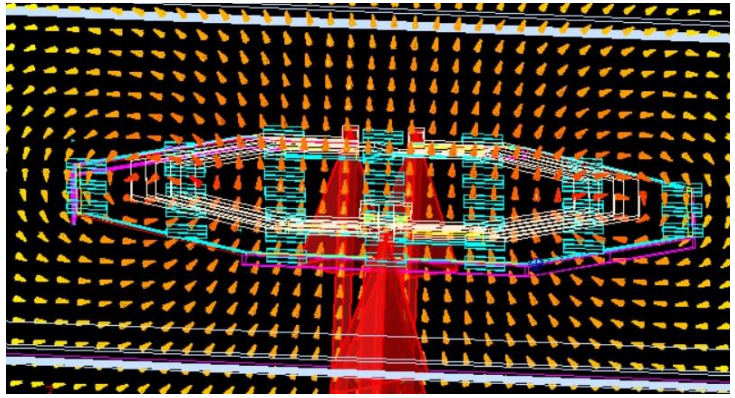


T-coil peaking

BWER ≈ 4.1

Custom design of T-coil transformer:

- First simulations of TSMC library inductors did not match the tech results (10% discrepancy in L and 55% discrepancy in Q)
- Now simulations match technology devices (less 10% discrepancy to be refined)
- Many TSMC inductors show a resonant frequency below 10-20 GHz
- Work in progress…



BWER: Bandwidth Extension Ratio

Next points

- Close the 12.5 Gb/s HPC+ driver for the SERDES
- Design the 12.5 GHz HPC+ receiver for the clock of the SERDES
- Design the 25 Gb/s HPC+ driver for the RR with T-coil and RR model (submission: 3° quarter 2022)
- Expose the 25 Gb/s HPC driver to TID e SEE
- Connect the 25 Gb/s HPC driver to SiPh RR and test them

Thanks for the attention