SER28 Status

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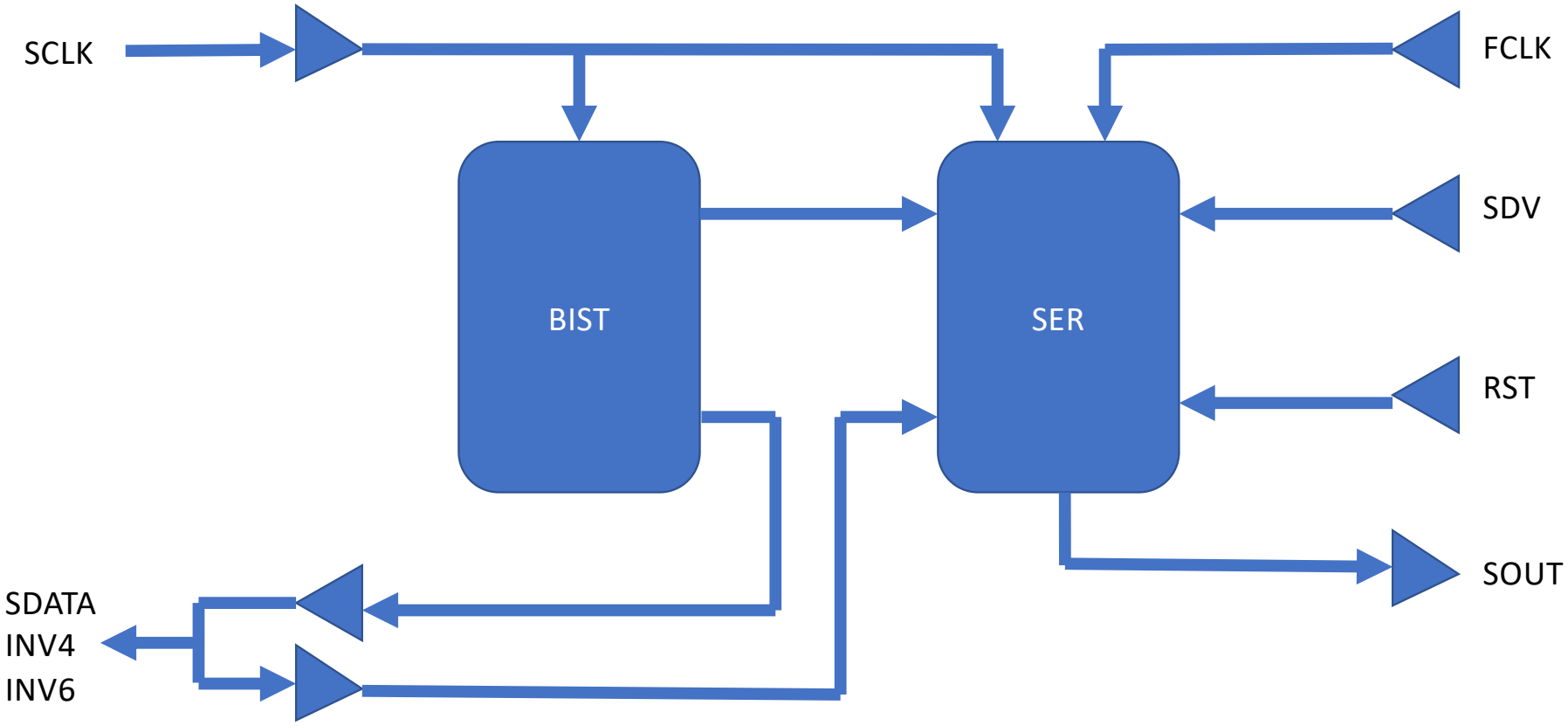
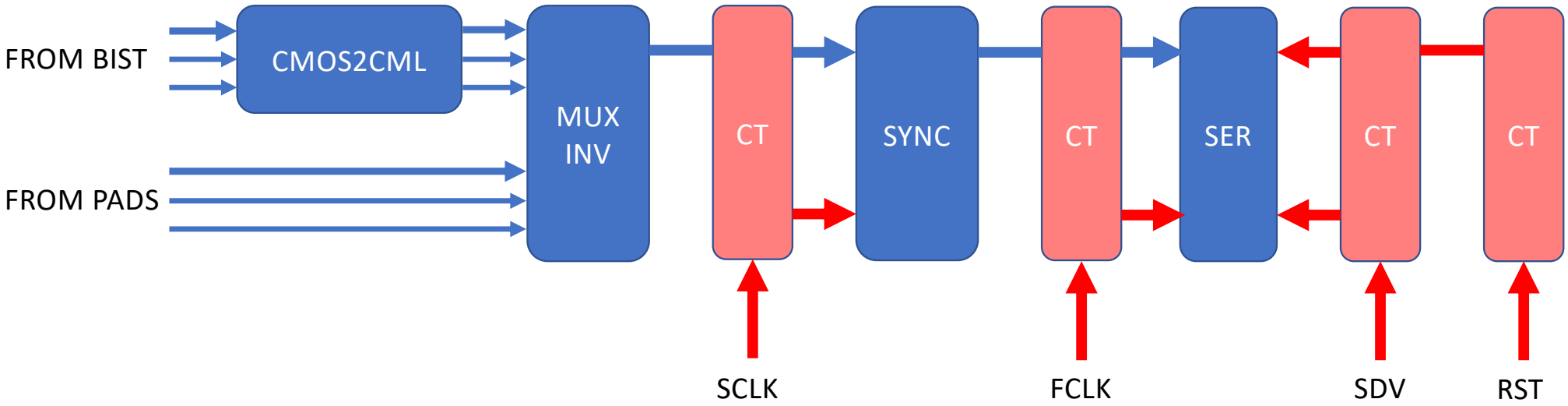
SER28 Status

- Redesign at INFN ongoing
  - New Schematics
  - Two SER architectures ready and under evaluation
    - Quad CELL => 8 DFFMUX / 4 bits
    - Single CELL => 4 DFFMUX / 1 bit
  - Different layout options under evaluation (DFFMUX and 10-bit Shift Register used as test benches)
    - L = 60nm – 2 fingers – Ncell guardring
    - L = 40nm – 2 fingers – Ncell guardring
    - L = 60nm – 1 finger– Nrow guardring
  - Preliminary padring ready (staggered pads)
    - Outer ring for signals
    - Inner ring for power supply, ground and reference voltages
    - Compatible with wire bonding cnstraints (100nm pitch in each ring)

SER28 ASIC Architecture

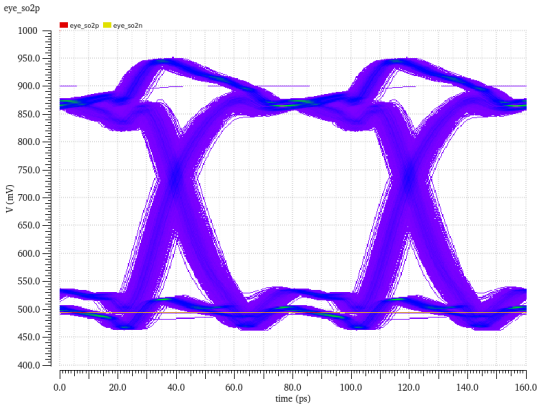


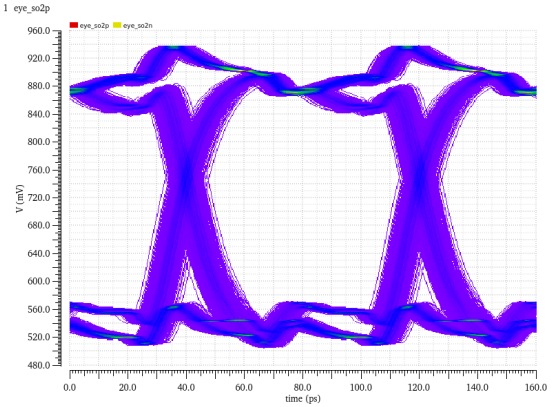
SER28 Architecture

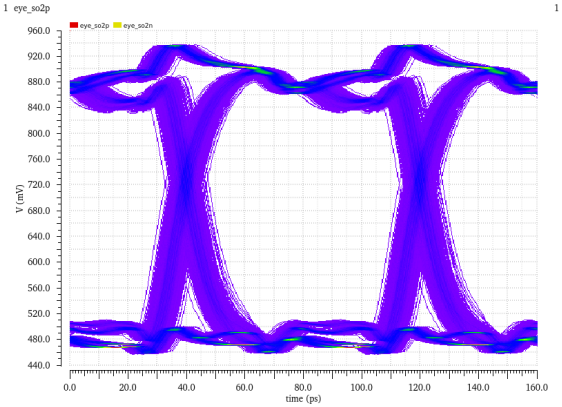


4-Bit SHR (PEX on the DFFMUX)

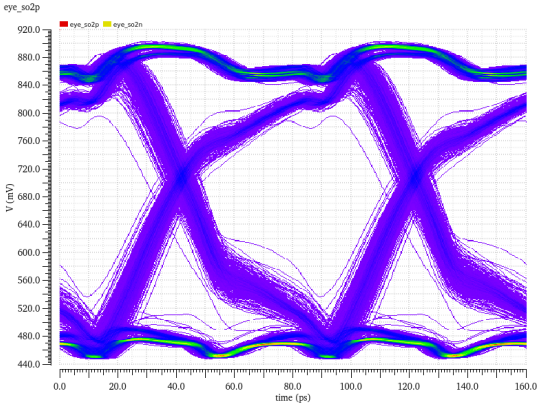
No PEX
(12.5 Gbps)

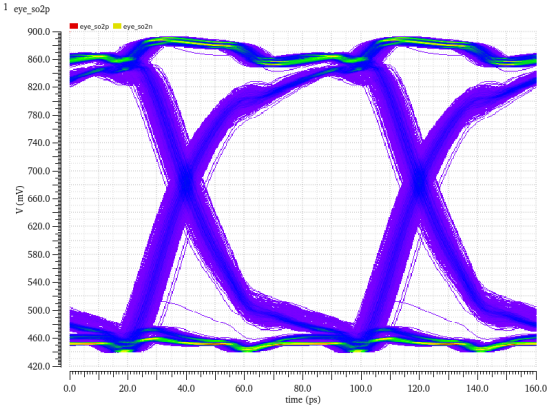


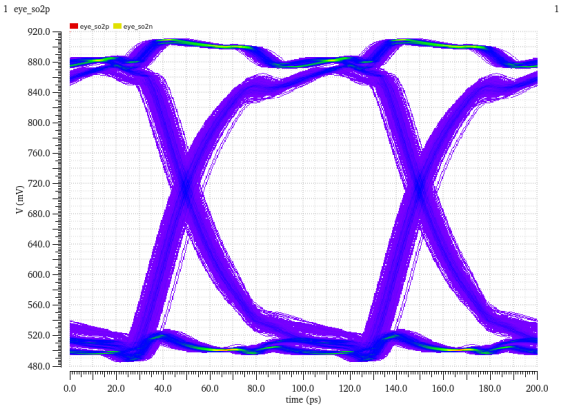




PEX
(12.5 Gbps)





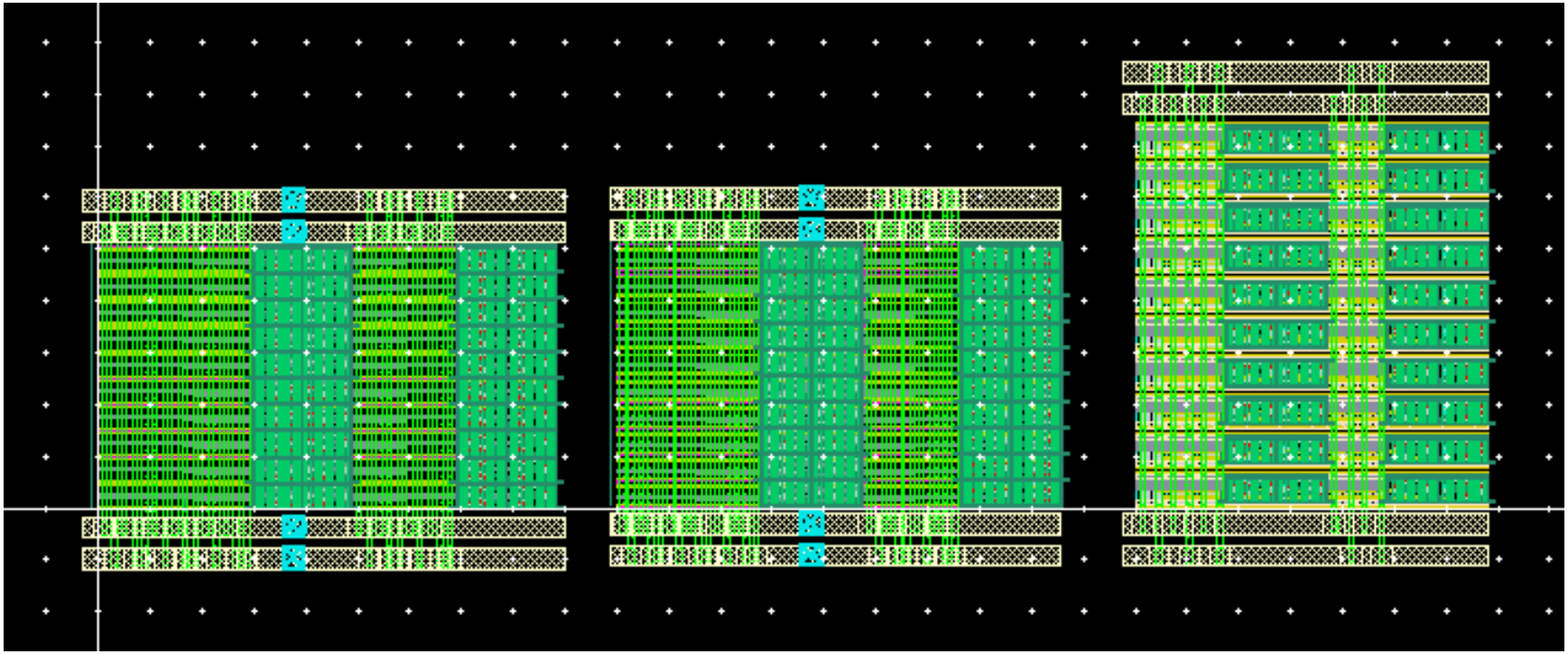


L = 60nm – 2 fingers

L = 40nm – 2 fingers

L = 40nm – 1 finger

10-bit SHR (PEX on the SHR)



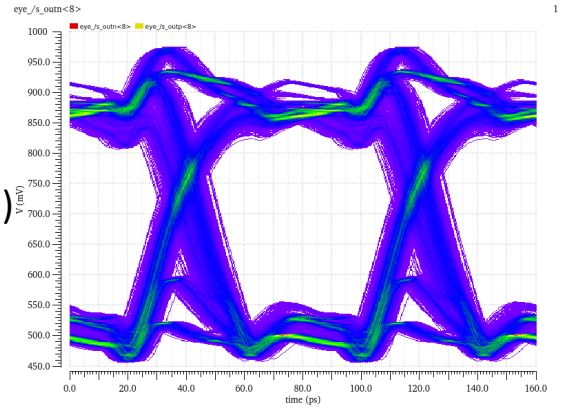
L = 60nm – 2 fingers

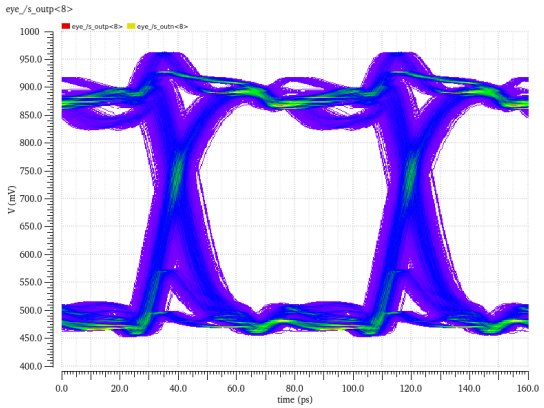
L = 40nm – 2 fingers

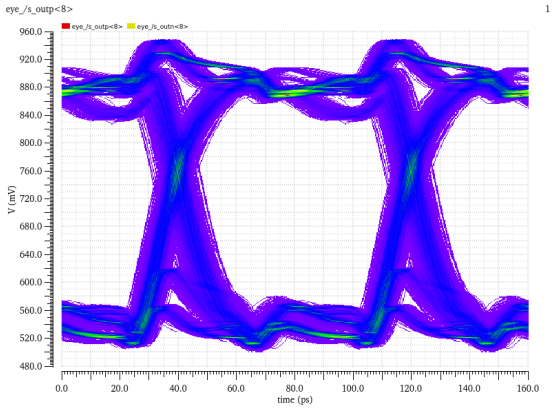
L = 40nm – 1 finger

10-bit SHR (PEX on the SHR)

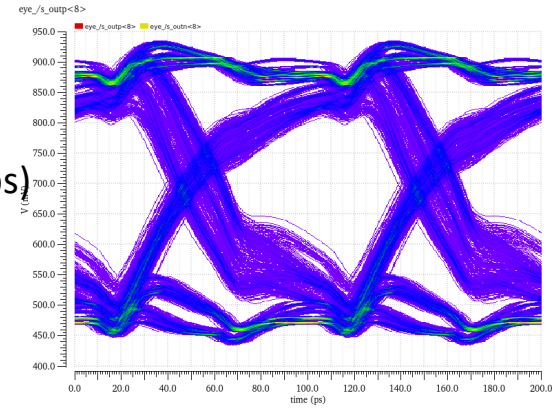
No PEX
(12.5 Gbps)



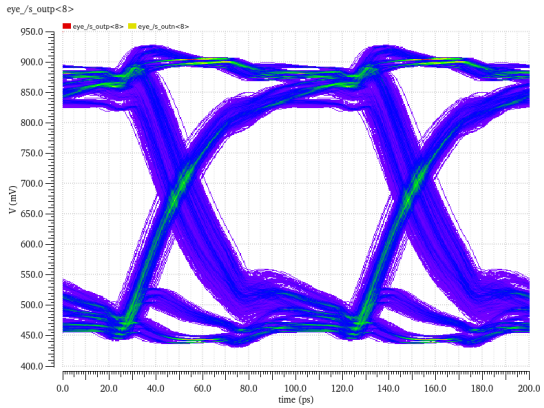




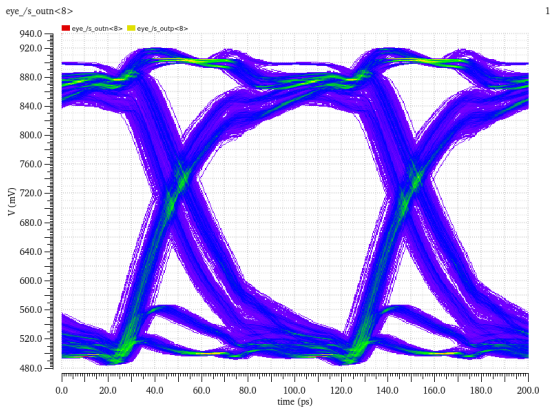
PEX
(10.0 Gbps)



L = 60nm – 2 fingers

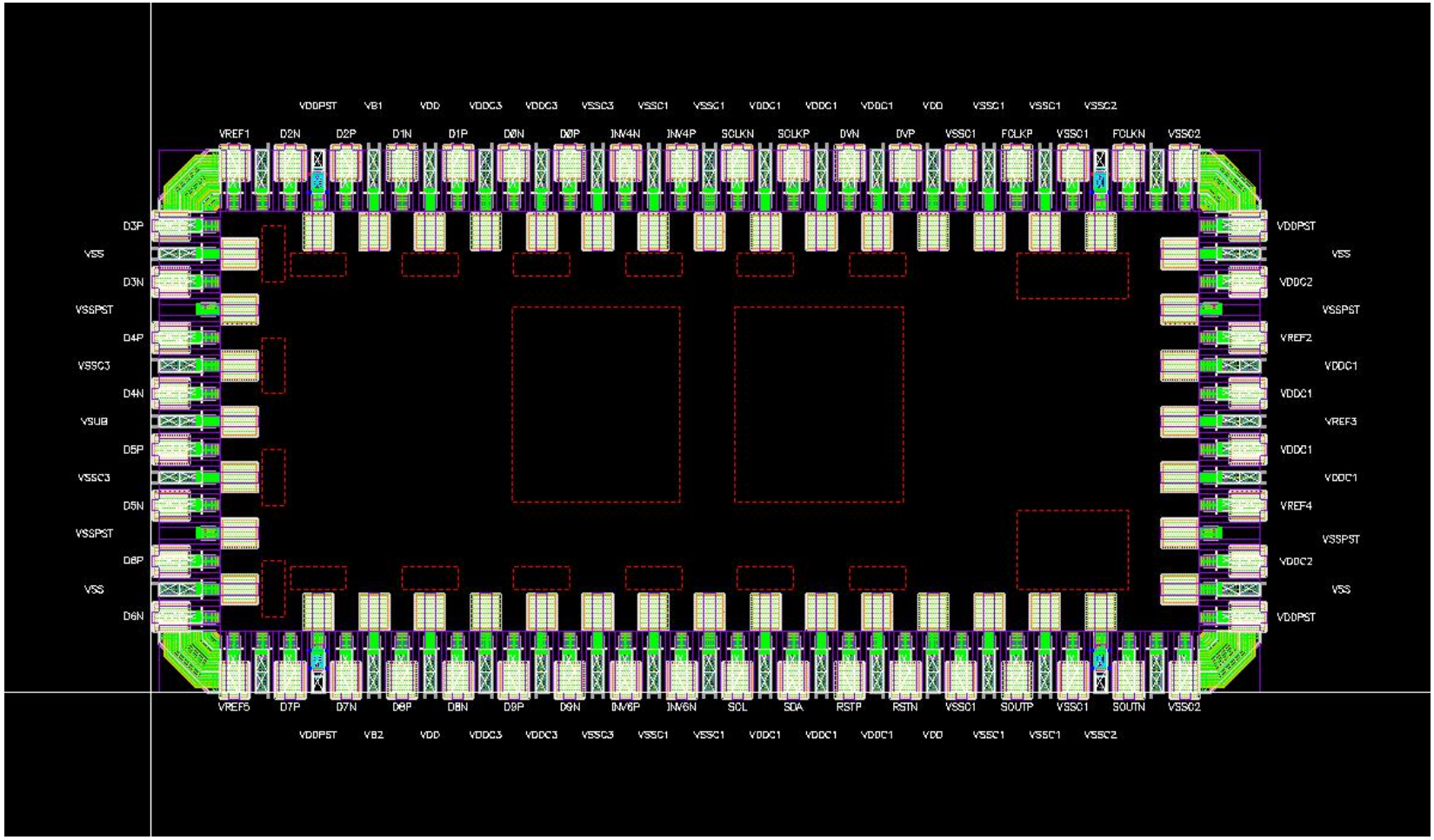


L = 40nm – 2 fingers



L = 40nm – 1 finger

SER28 ASIC Preliminary Pad Rig



SER28 ASIC Preliminary Pin List

- Outer Ring => 52 Pads
- Inner Ring => 44 pads

Signals

- LVDS Signals (36 Pads)
  - SDATA => 10x2, I/O
  - INV4, INV6 => 2x2, I/O
  - SCLK, SDV, RST => 3x2
- CML Signals (4 Pads)
  - FCLK => 1x2, Input
  - SOUT => 1x2, Output
- CMOS Signals (2 Pads)
  - SCL => 1, Input
  - SDA => 1, I/O

Power, Ground & Bias (58 Pads)

- SER (20 Pads)
  - VDDC1 => 10x
  - VSSC1 => 10x
- CML TX/RX (6 Pads)
  - VDDC2 => 2x
  - VSSC2 => 4x (2x?)
- BIST (8 Pads)
  - VDDC3 => 4x
  - VSSC3 => 4x
- LVDS TX/RX (19 Pads)
  - VDDPST => 4x
  - VSSPST => 4x
  - VDD => 4x
  - VSS => 4x
  - VB1, VB2, VSUB => 3x
- VBIAS (5 Pads)
  - VREF1-5 => 5x

Plans

- SER28 ready for mid February (INFN-PI)
- BIST ready for mid February (INFN-MI)
- LVDS TX/RX ready before the end of February (INFN-PI)
- CML TX/RX and High Frequency Pads ready before the end of February (INFN-PI)
- SER28 integration completed before mid March