RD53 pixel chips for the CMS and ATLAS CMS Phase-2 upgrades at the High Luminosity LHC

Flavio Loddo - I.N.F.N. Bari
on behalf of the RD53 Collaboration and CMS/ATLAS testing teams

Introduction

- The Phase-2 upgrades of CMS and ATLAS at the High Luminosity LHC will require new trackers with readout electronics operating in extremely harsh radiation environment and high data rate readout.
- During the Long Shutdown 3, both silicon tracking systems will be entirely replaced because of the accumulated radiation damage and to take advantage of the increased luminosity → **design a new pixel readout chip**

- **Most challenging HEP chip ever made**, from many different points of view:
  - Extreme hostile radiation environment (TID 1 Grad)
  - Extreme SEU/SET issues (50 bit flips per chip per second)
  - Extreme hit (12 GHz per chip), trigger (1 to 4 MHz) and readout (5 Gbits/s per chip) rates
  - Large chip (largest transistor count HEP chip ever made for extreme hostile environment)
  - Novel serial powering with complex on-chip serial power regulator.

- **The chips are being developed by the RD53 Collaboration,** a joint effort between ~ 24 ATLAS and CMS Institutes established in 2013

Annecy-LAPP, Aragon, Bergen, Bonn, CERN, FH-Dortmund, FNAL, INFN (Bari, Milano, Padova, Bergamo-Pavia, Pisa, Perugia, Torino), LBNL, Marseille-CPPM, New Mexico, NIKHEF, Orsay–LAL, Paris-LPNHE, Prague IP-FNSPE-CTU, RAL-STCF, Sevilla

Mandate of RD53 Collaboration:

1. Characterization of chosen **65nm CMOS** technology in radiation environment
2. Design of a **rad-hard IP library** (Analog front-ends, DACs, ADCs, CDR/PLL, high-speed serializers, RX/TX, ShuntLDO, …)
3. Design and characterization of several test chips and a **half-size pixel chip demonstrator (RD53A)** with design variations
4. Design of pre-production (**RD53B**) and production (**RD53C**) pixel readout chips

RD53 chips

Due to mechanical constraints, the two trackers cannot have exactly the same pixel chip

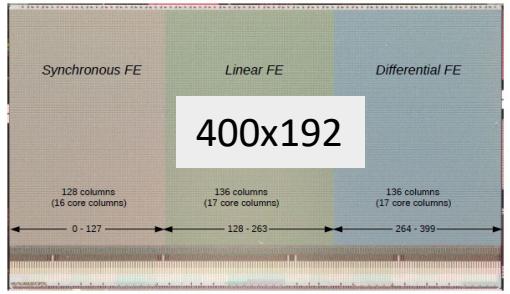
Based on a common set of specifications, RD53 developed a highly configurable chip:

ATLAS and CMS chips are two instances of the same common design, with different

- Size: this is a parameter in the common netlist
- Analog Front-End, chosen according to specific requirements of the experiment

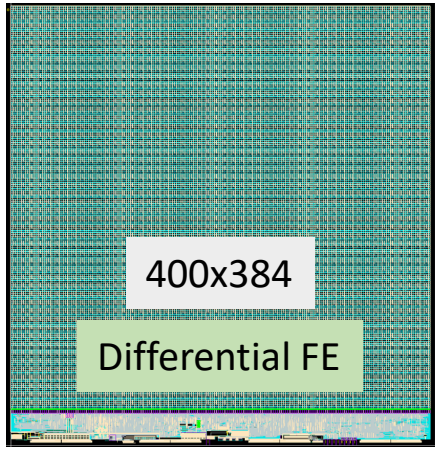
	ATLAS/CMS
Chip size	20x21mm^2/21.6x18.6mm^2
Pixel size	50x50 µm^2
Hit rate	3.5 GHz/cm^2
Trigger rate	1 MHz/750kHz
Trigger latency	12.5 us
Min. threshold	600 e-
Radiation tolerance	> 500 Mrad @-15C
Power	< 1W/cm^2

https://cds.cern.ch/record/2663161



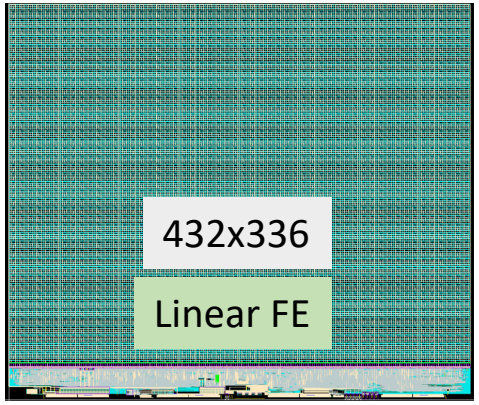
RD53A

- **Half-size demonstrator**
- Size: 20 x 11.5 mm2
- 3 Analog Front-Ends
- 2 readout architectures
- submitted in August 2017



RD53B-ATLAS (ItkPix_V1)

- submitted in March 2020
- size: 20 mm x 21 mm



RD53B-CMS (CROC_V1)

- submitted in June 2021
- size: 21.6 mm x 18.6 mm

RD53C-ATLAS: April 2022

RD53C-CMS: Sept/Oct 2022

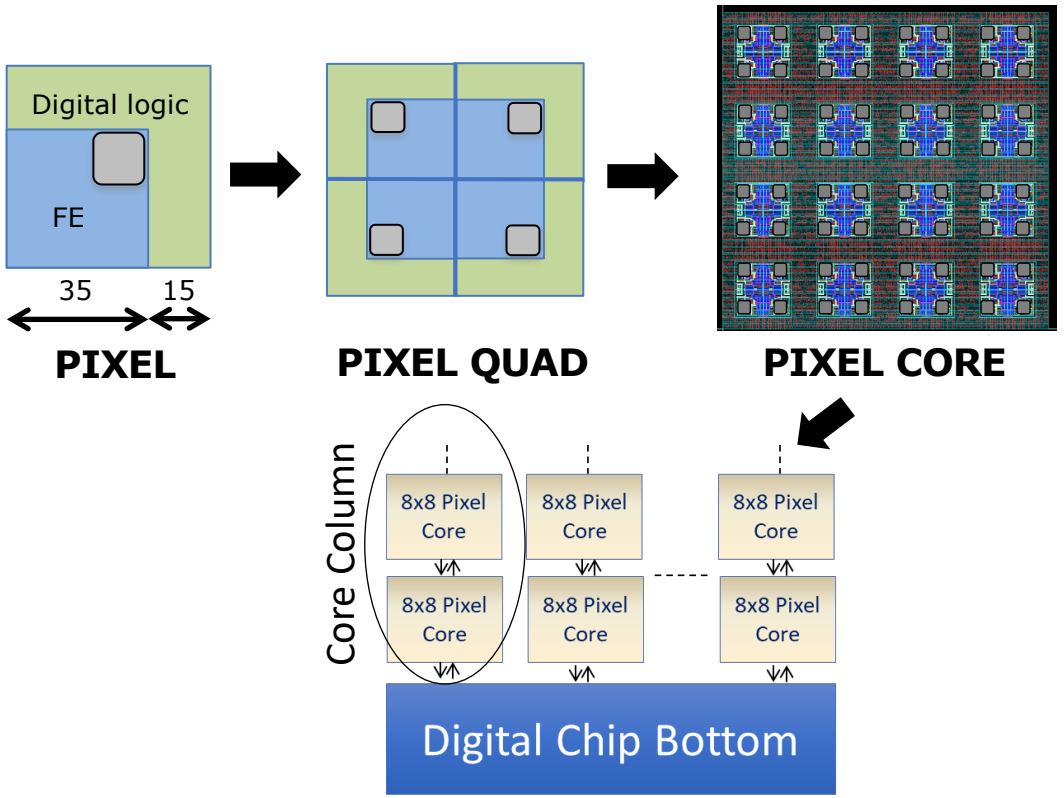
INFN-Bari contribution

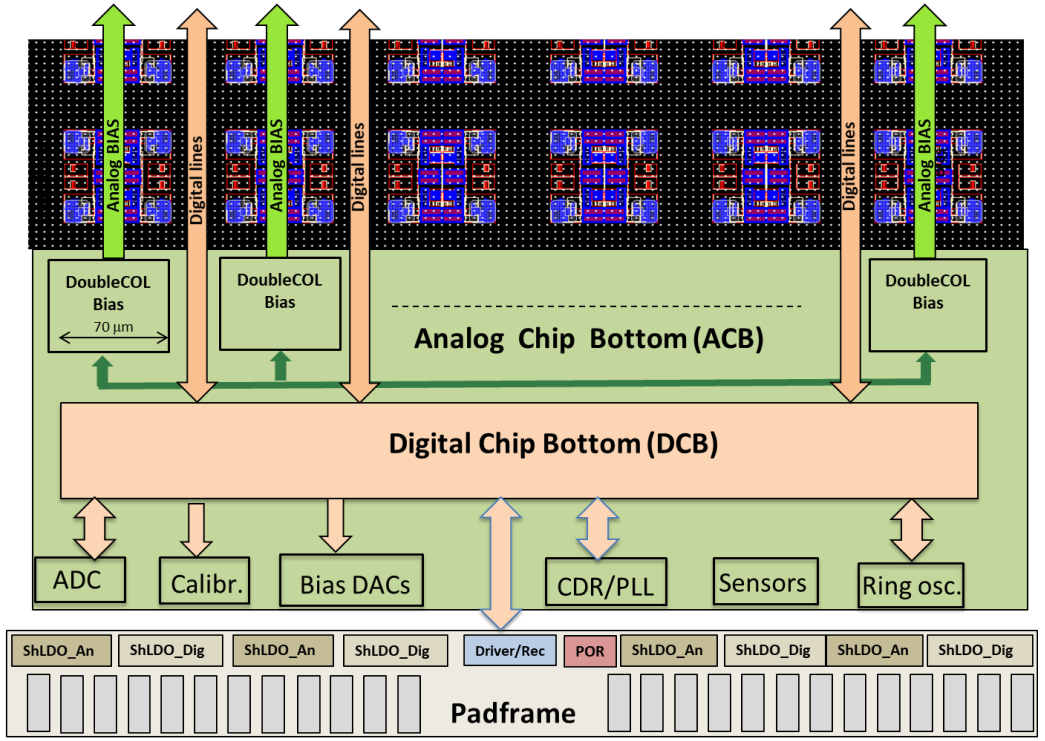
Manpower:
- G. De Robertis
- F. Loddo

Design activity:
- Chip floorplanning
- Rad-hard 10-bit Digital-to-analog converter
- Analog bias network
- Power distribution
- Scan-chain architecture for easier production testing (Design for Testability)
- Sign-off verifications

Responsibilities
- Since June 2016: F. Loddo is the RD53 Project Engineer
- Since May 2018: F. Loddo is the CMS Phase2 Inner Tracker ASIC project coordinator

Floorplan





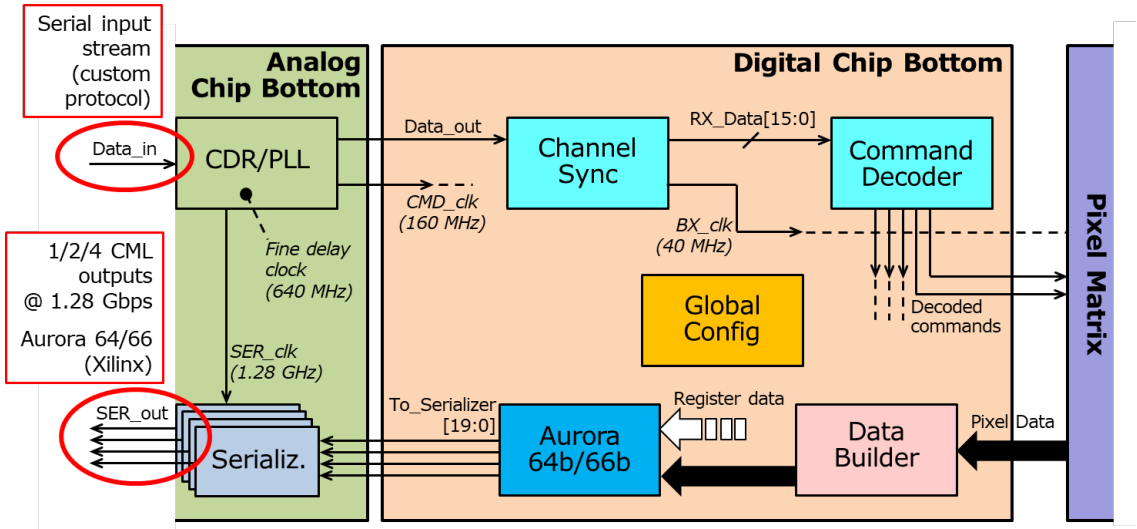
Pixel array

- Built up of **8 x 8 Pixel Cores** → **16 quads**
- All Cores are identical → efficient hierarchical verifications
- Cores are abutted: each Core receives all input signals from the previous one (closer to the DCB) and regenerates them for the next Core → no external routing for connections

Chip periphery

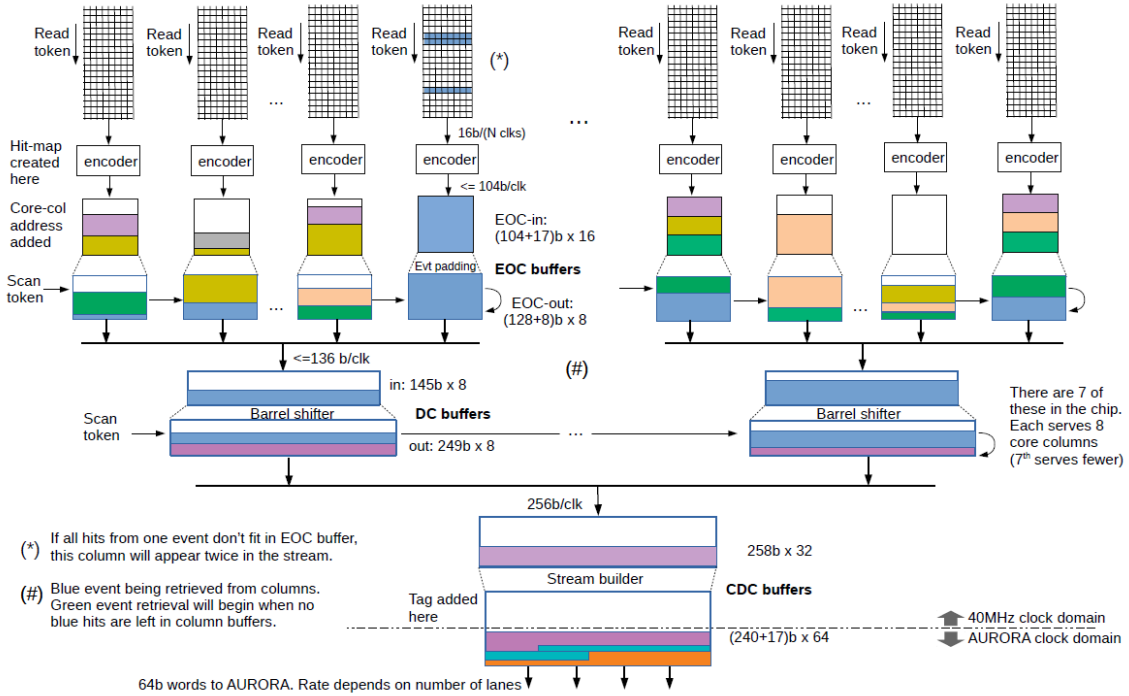
- Analog Chip Bottom (ACB): analog and mixed/signals building block for Calibration, Bias, Monitoring and Clock/Data recovery
- Digital Chip Bottom (DCB): synthesized digital logic
- Padframe: I/O blocks with ESD protections, ShuntLDO for serial powering

Data flow architecture

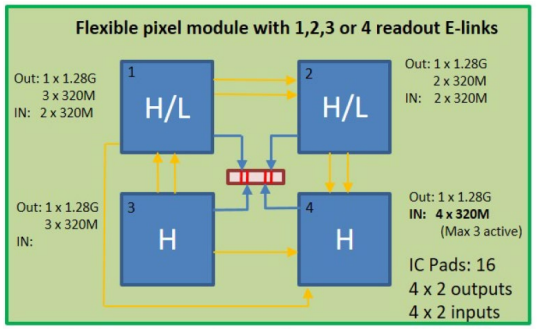


- Hits are stored as Time-over-Threshold, associated to a time stamp
- 6-bit ToT counter, but only 4 bits are stored and read-out
- Each pixel has 8x4-bit ToT memories
  - Support of 6-to-4 ToT mapping (dual slope)
  - Selectable counting clock: 40 MHz or 80 MHz
- The time stamp memory is shared among 4 pixels of the same 4x1 **Pixel Region**

- Token-based readout of hits, organized in Core Columns
- Multiple levels of data processing, event building, buffering and formatting before final readout via serial links

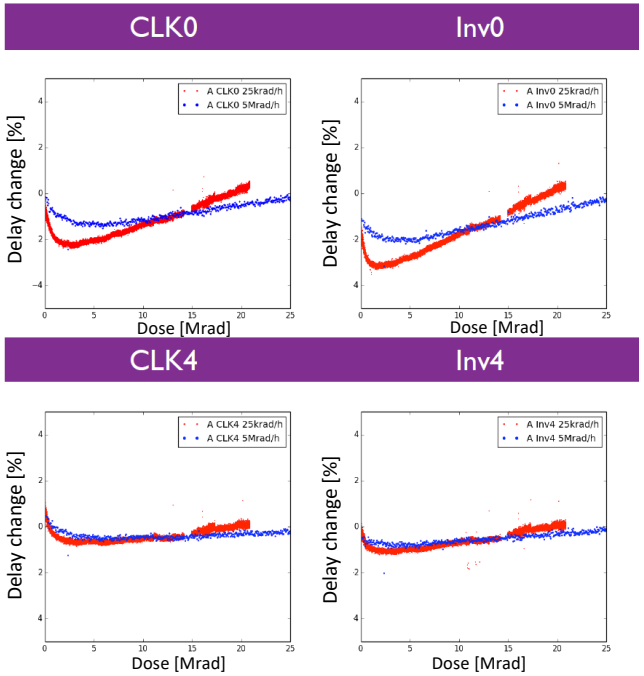


- **Command, control and timing** are provided by a **single 160 Mbit/s** differential control link, driving up to 15 chips (4 bit addressing)
  - CDR/PLL recovers Data and Clock
- **Readout via serial links** (1-4 x 1.28 Gbit/s) using Aurora 64/66 encoding
- **Multi-Chip Data Merging** available for low-rate outer pixel layers: one chip of the module can be configured as "primary" to aggregate serial data from one or more other "secondary" chips and merge them with its own output



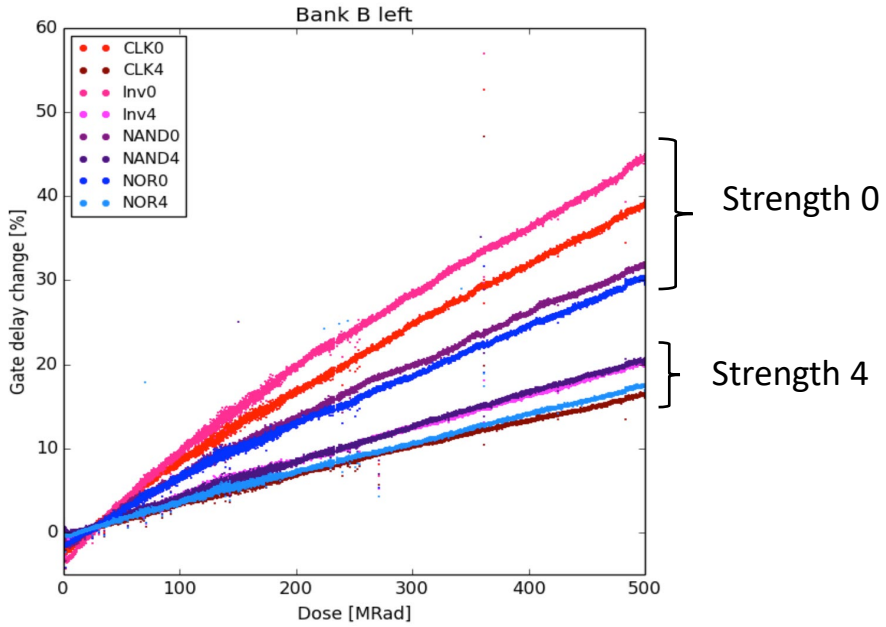
Radiation hardness

- Extensive TID X-ray tests done in the past years on RD53A, RD53B and small prototypes to qualify IPs, analog FEs and digital standard cells
- The TID damage concerns essentially the digital design because of the small area devices
- Tests done at low temperature (-20°C) and high dose rate show that the RD53 chips are operating correctly at least up to 1 Grad
- From measurements on Ring Oscillators (RD53A and RD53B): **gate delay degradation roughly x2 larger for low dose-rate (LDR)**



Compare 5 Mrad/h and 25 krad/h

ROSC	Delay slope [%/MRad]		
	HDR	LDR	Ratio
CLK 0	0.051	0.121	**2.34**
CLK 4	0.012	0.026	**2.32**
Inv 0	0.076	0.176	**2.31**
Inv 4	0.029	0.055	**1.94**
NAND 0	0.034	0.085	**2.52**
NAND 4	0.008	0.016	**1.91**
NOR 0	0.051	0.097	**1.91**
NOR 4	0.031	0.051	**1.61**



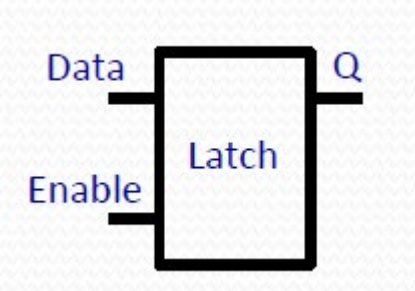
Correction of HDR results using the ratio LDR/HDR

- Irradiation corner models and extreme corners from the foundry were used to predict the TID effect and design to guarantee good timing for the digital design. These corners resulted to be more pessimistic than the extrapolations of low dose-rate tests to 500 Mrad
- These tests, together with the policy to **avoid minimum size digital cells**, give confidence that RD53B chips will meet TID specifications if **operated at cold temperature**. Irradiated chips must be cooled while under power, **since room or high temperature annealing is detrimental**

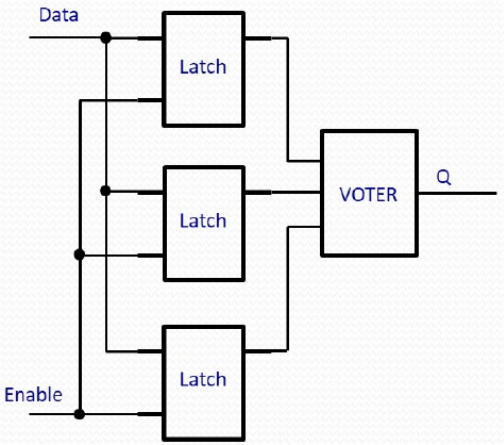
Single Event Effect mitigation

❑ **Pixel configuration registers (8 bits)** → 1.28 Mbit/chip
- The small pixel area does not allow to implement the full protection for all bits
- 3 less critical bits unprotected
- 5 more relevant bits protected with Triple Modular Redundancy (TMR) without self-correction

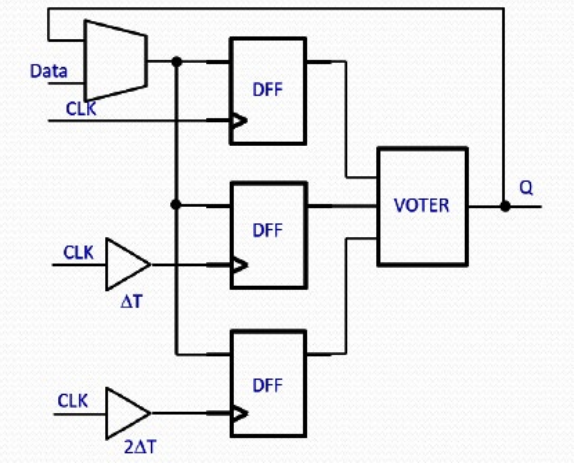
❑ **Global configuration registers and state machines** (~90 kbits)
- TMR with self-correction and triplicated clock with skew ($\Delta T \sim 300ps$) to filter SET glitches



Unprotected latch



TMR latch without correction



TMR latch with correction and triplicated clock with skew

❑ Different structures and critical analog blocks (PLL, Bandgape reference, Bias circuitry) have been verified with analog SEU/SET injection simulations

❑ SEU in the digital logic, including pixel array, are being verified with extensive SEU simulations

SEE test campaigns

- **Centre de Ressources du Cyclotron (CRC) – Louvain la Neuve**
  - Two SEU test beam campaigns: **October 8, 2020** and **November 17, 2020**
  - The chip irradiated in vacuum with several heavy ions flavours (1.3 to 62.5 MeV.cm²/mg)
  - 1 SEL test beam campaign in November 11, 2021
  - Only Xenon ion was used
- **TRIUMF facility**
  - SEU tests campaign done remotely **December 19-20, 2020**
  - 480 MeV proton beam
  - The chip tested under a proton flux of 1.5 10^9 p/cm²/s similar to the hadron flux in the HL-LHC
- **GANIL – Caen**
  - SEU campaign in **April 2021** and dedicated for CDR/PLL
  - Test done with only 1 ion : ^{129}Xe : LET = 30 MeV.cm²/mg
- **KU Leuven-Campus Geel (PULSCAN)**
  - Laser SEU testing **October 5, 2021**
  - 2 photon absorption
  - Pulse energy of 1 nJ and Pulse frequency of 1 KHz
- **PS-CERN Facility**
  - 24 GeV Proton testing : **October 14 to November 4, 2021**
  - The flux is about 40 times higher than in HL-LHC

CRC – Louvain la Neuve

TRIUMF

The flux = 1.5 10^9 p/cm²/s

GANIL

PULSCAN - Leuven

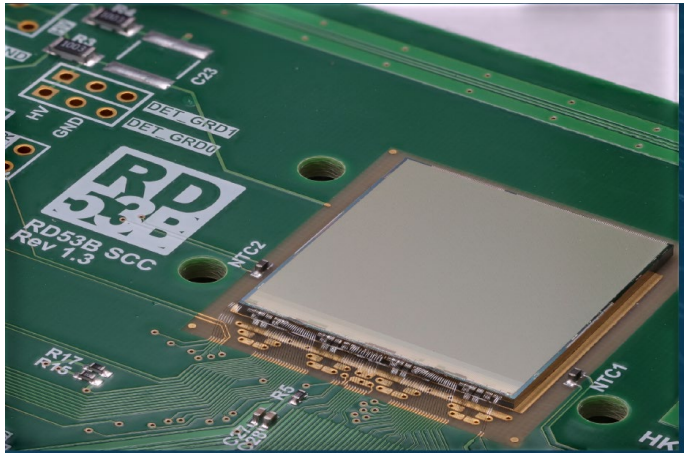
PS-CERN

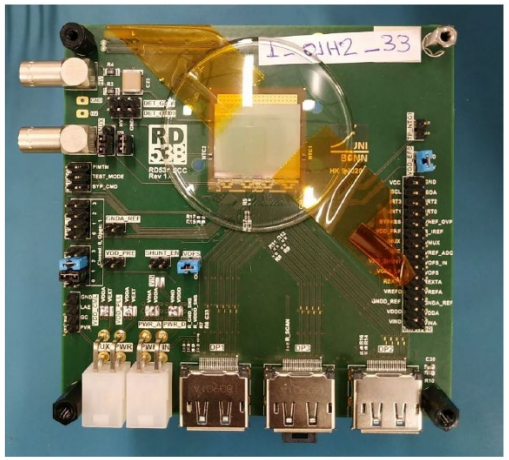
- Global configuration registers: $\sigma_{latch}/\sigma_{TMR\_with\_correction}$ ~ 400
- Pixel configuration registers: $\sigma_{latch}/\sigma_{TMR\_no\_correction}$ ~ 100 (assuming regular refresh)
- The triplication in the Global Configuration registers seems to be efficient
- Configuration registers must be continuously refreshed at recommended rate for Inner layers ~1Hz

	Pixel Config. cross-section (cm²) STD: single latch TMR: without correction	**Global Reg. cross-section (cm²)** TMR with correction and skewed clocks
Calculation for 200 MeV proton based on heavy ion testing (F. Faccio, CERN)	**STD: 8.63 10^{-15}**	**7.86 10^{-17}**
Experimental from 480 MeV proton test	**STD: ~1.2 10^{-14}** **TMR: 1-5 10^{-16}**	**3.57 10^{-17}**

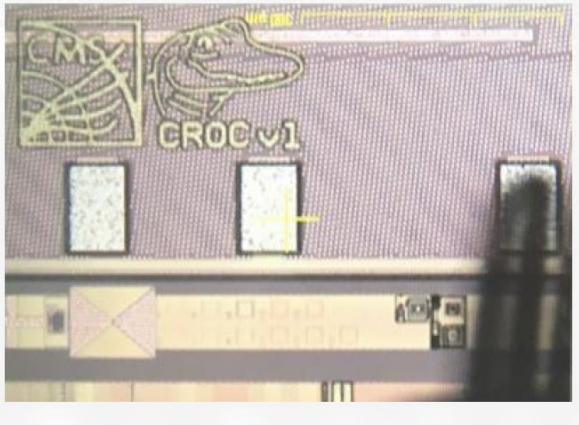
Testing of RD53B chips

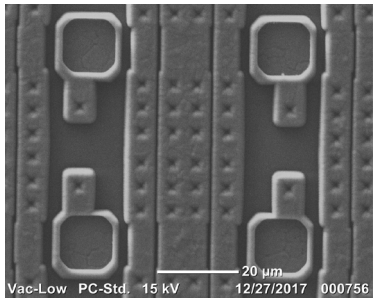
RD53B-ATLAS (ItkPixv1) received in June 2020





RD53B-CMS (CROCv1 received end of August 2021





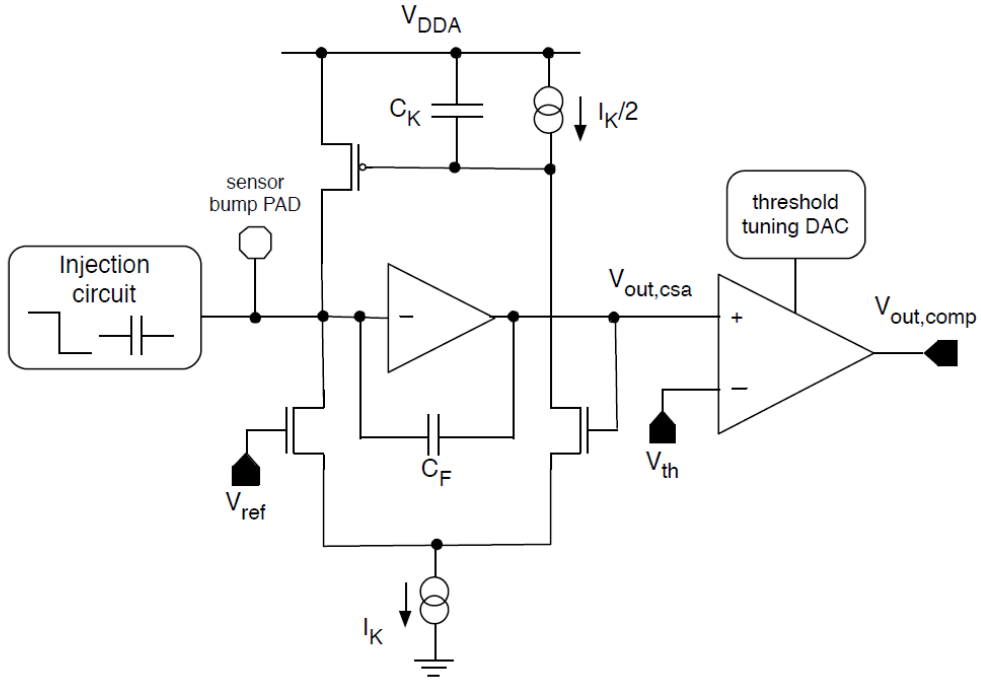
50 um

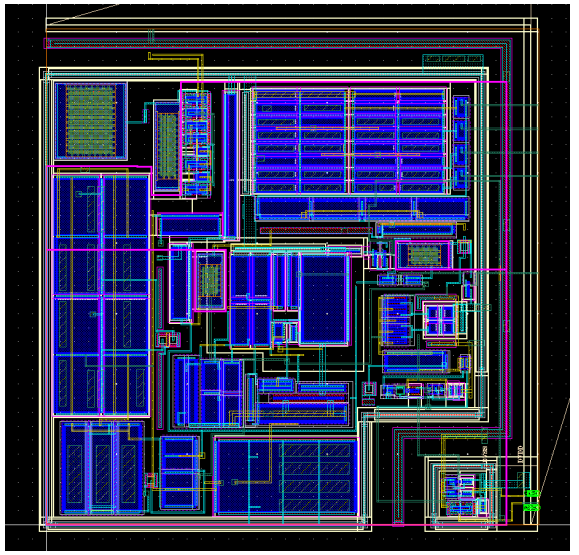
50 um

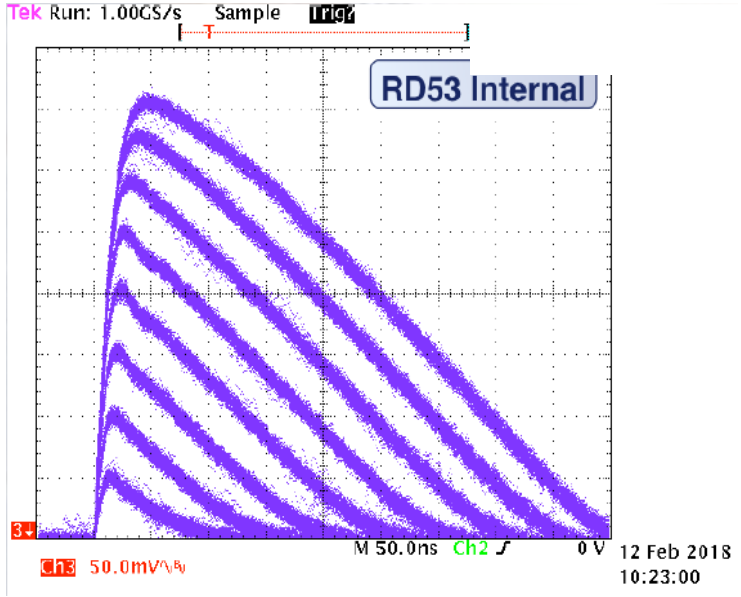
<u>The chips work without major issues so far</u>:

- ✓ Power consumption as expected
- ✓ Aurora link stable at 1.28 Gbps and 640 Mbps
- ✓ Start-up and communication without problems
- ✓ Analog and digital scan work fine: all pixels respond to injections
- ✓ Analog Front-Ends (two versions): tuning capability demonstrated with low ENC
- ✓ Bug in the ToT memory of ATLAS chip was fixed in the CMS chip and now works as expected
- ✓ ToT counting works in all the programmable modes, with the exception of a misbehaviour in the ToT counting at 80 MHz in the asynchronous sampling mode (bug-fix has been proposed for the final chip)
- ✓ ADC/DAC linearity measured, Ring oscillators tested
- ✓ Chip data merging under test now: so far no problems
- ✓ Software/firmware development ongoing for more tests

Linear Front-End (RD53B-CMS)







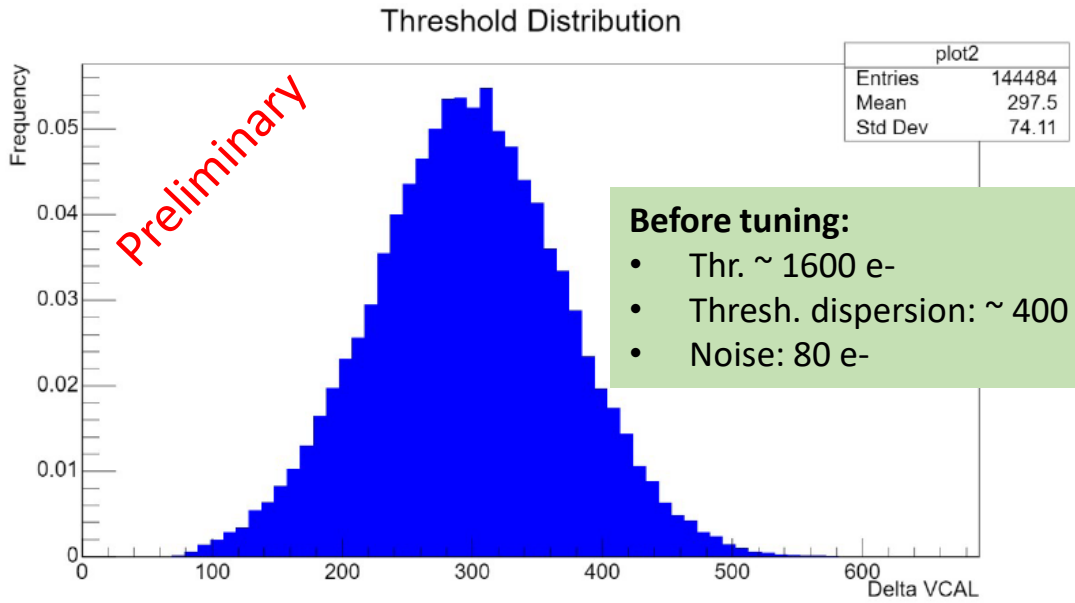
- **Charge sensitive amplifier**

- **Krummenacher feedback for return to baseline and leakage current compensation**

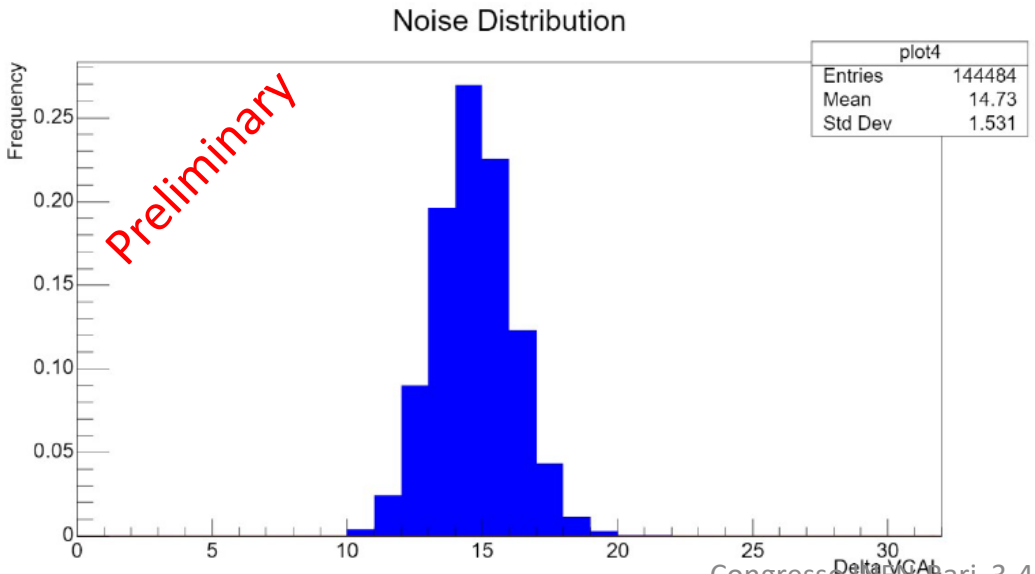
- **Comparator**
  - ❖ **10-bit DAC for global threshold**
  - ❖ **5-bit local trimming DAC for threshold tuning**

CROCv1 Front-End threshold tuning and noise

Before tuning

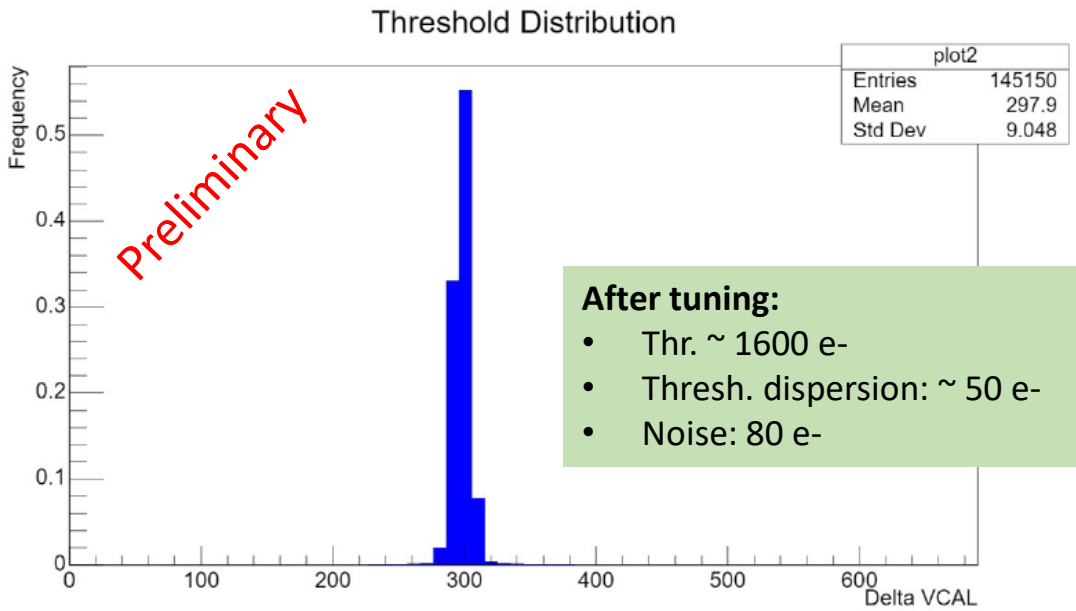


Before tuning:
- Thr. ~ 1600 e-
- Thresh. dispersion: ~ 400 e-
- Noise: 80 e-

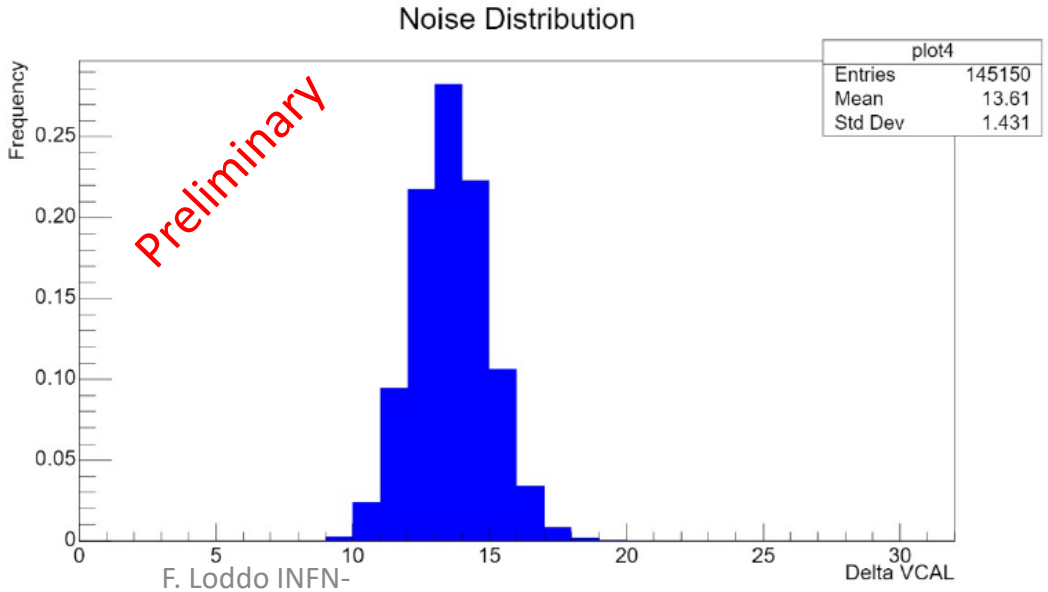


1 DeltaVCAL ~5.5 e-

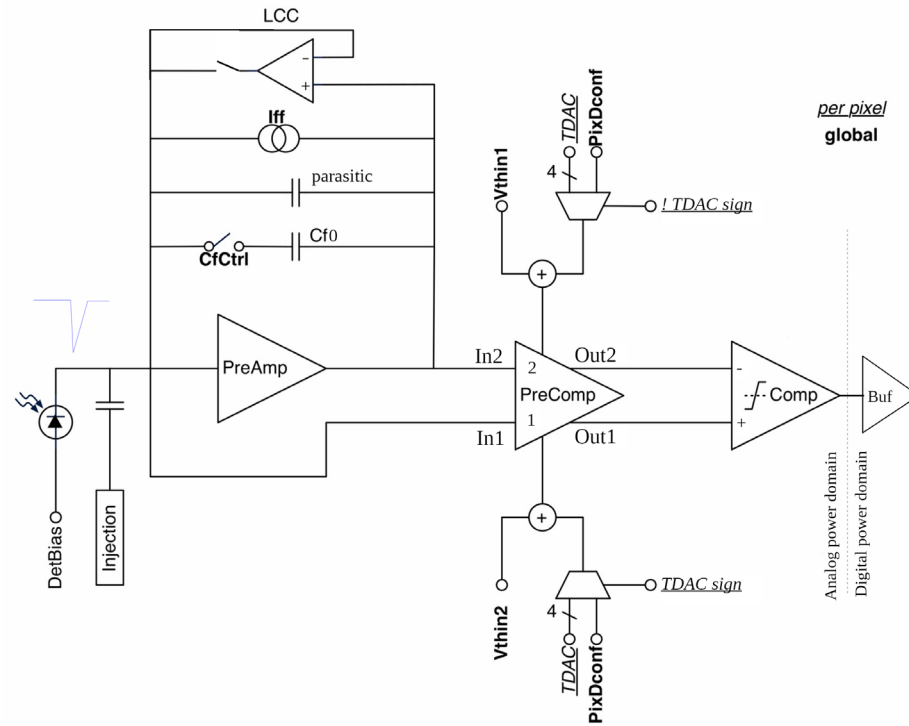
After tuning

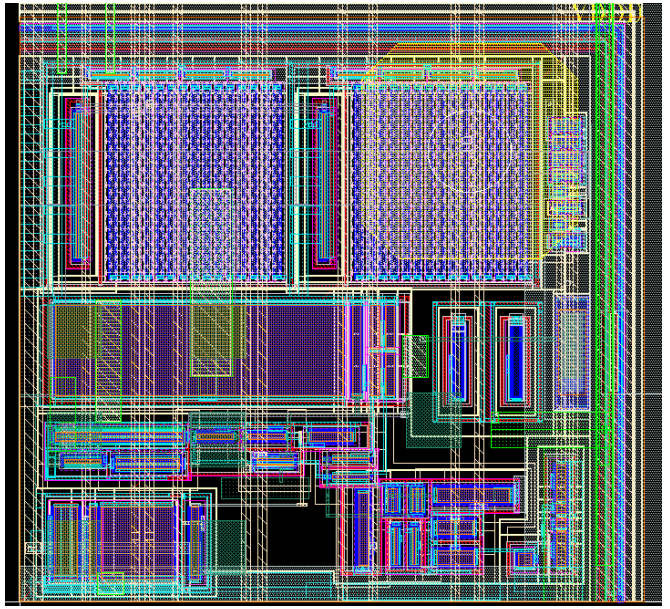


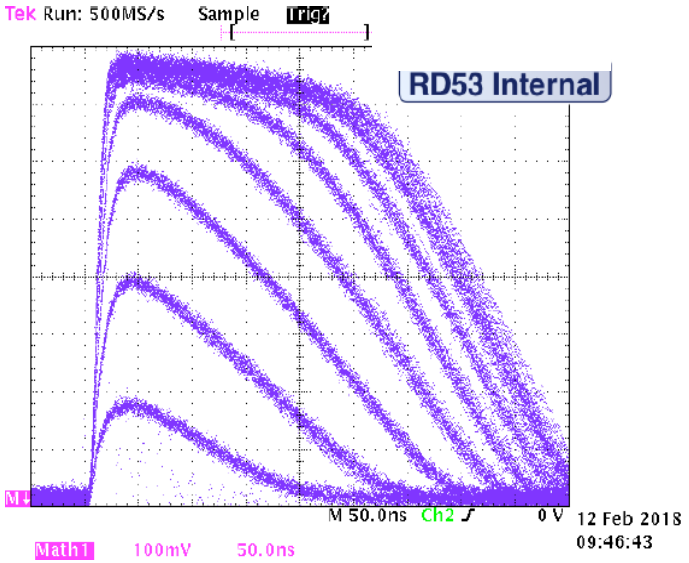
After tuning:
- Thr. ~ 1600 e-
- Thresh. dispersion: ~ 50 e-
- Noise: 80 e-



Differential Front-End (RD53B-ATLAS)

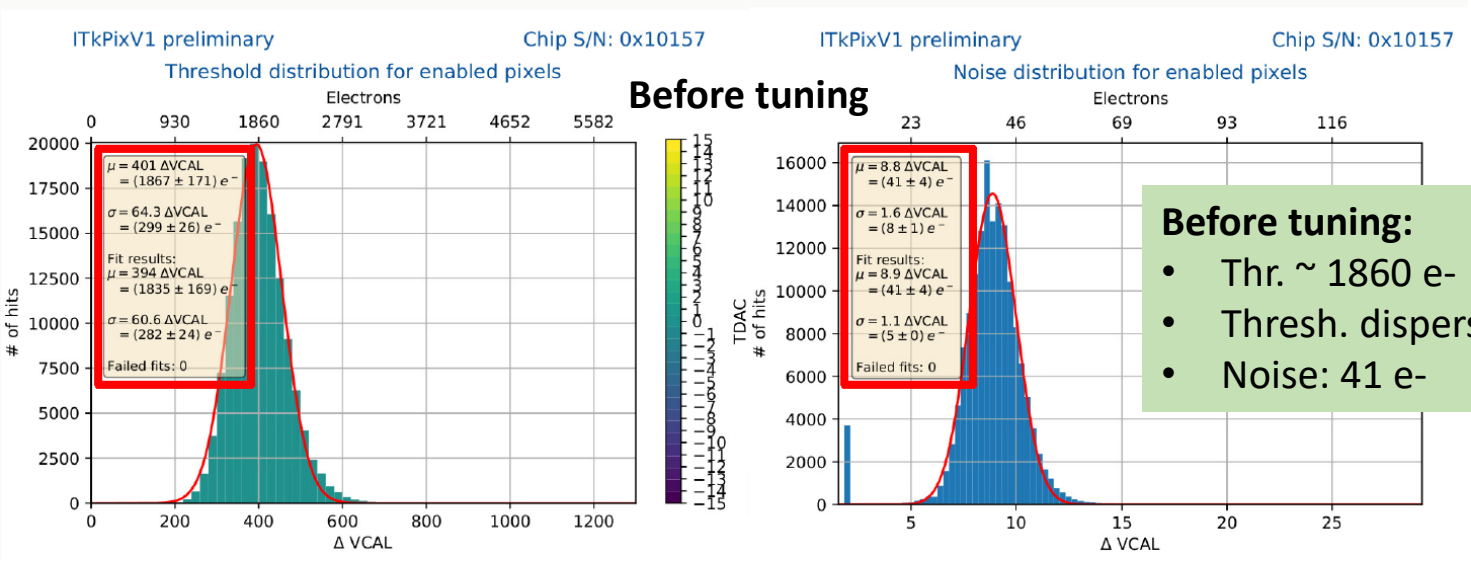






- **Charge sensitive amplifier**
- **Leakage current compensation circuit**
- **Continuous reset integrator, with tunable feedback current (global setting)**
- **DC-coupled pre-comparator stage**
  - ❖ **10-bit DAC for global threshold**
  - ❖ **4+1 bit local trimming DAC for threshold tuning**
- **Fully differential input comparator**

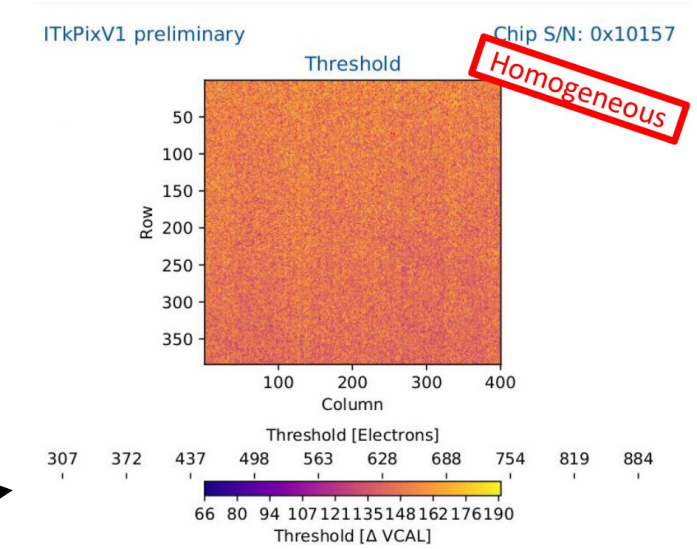
ITkPixV1 Front-End threshold tuning and noise

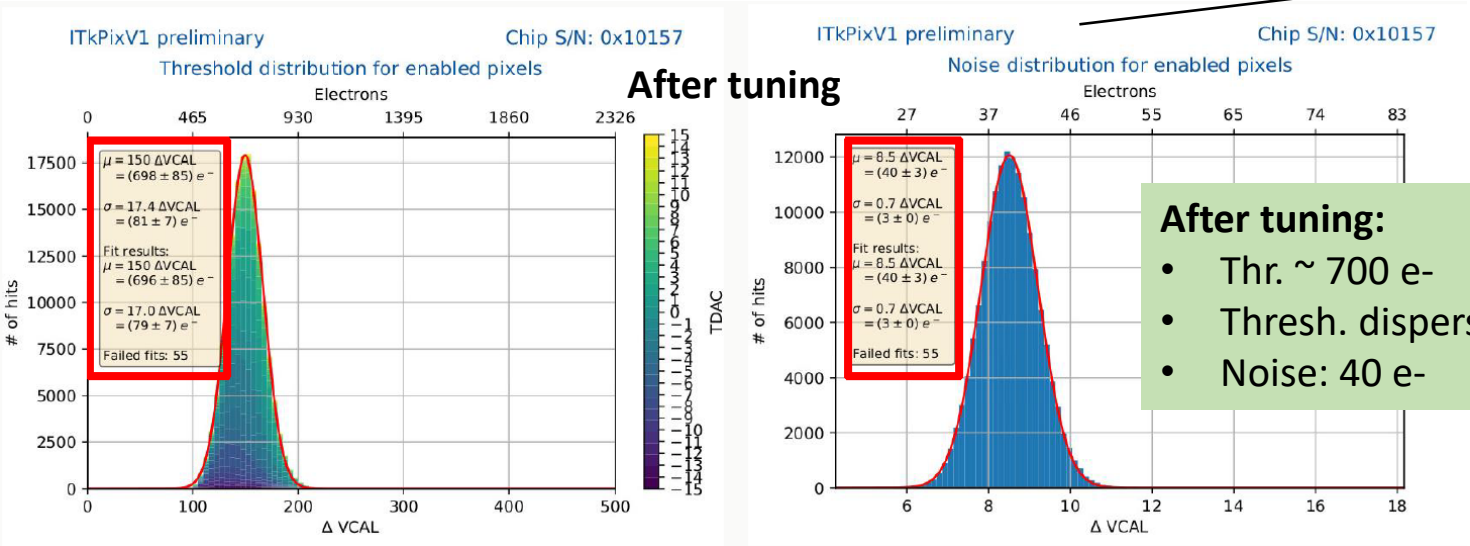


Before tuning

Before tuning:

- Thr. ~ 1860 e-
- Thresh. dispersion: ~ 300 e-
- Noise: 41 e-

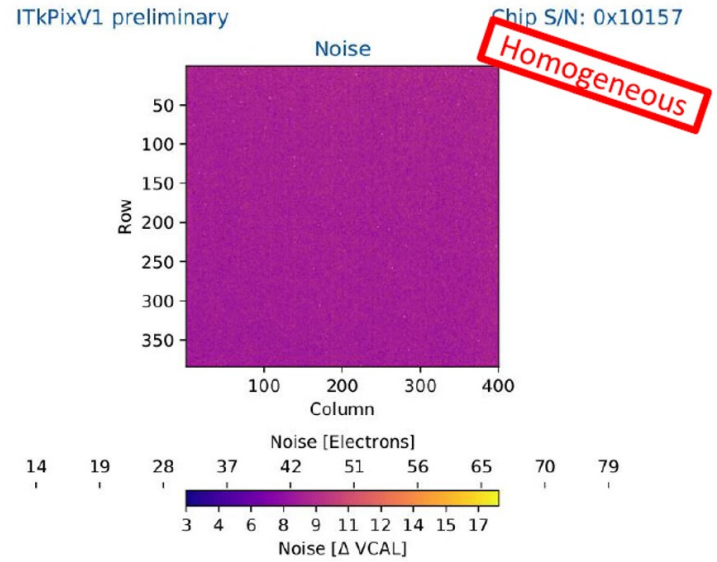




After tuning

After tuning:

- Thr. ~ 700 e-
- Thresh. dispersion: ~ 80 e-
- Noise: 40 e-



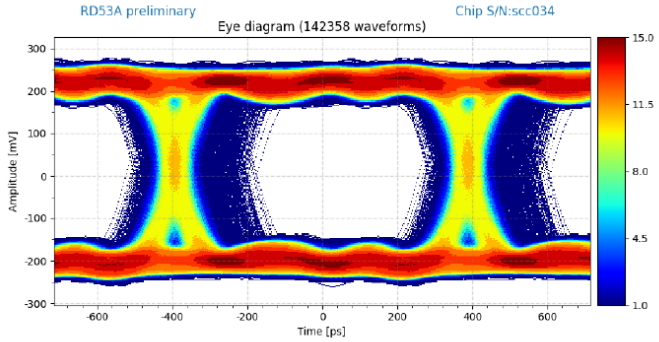
CDR/PLL

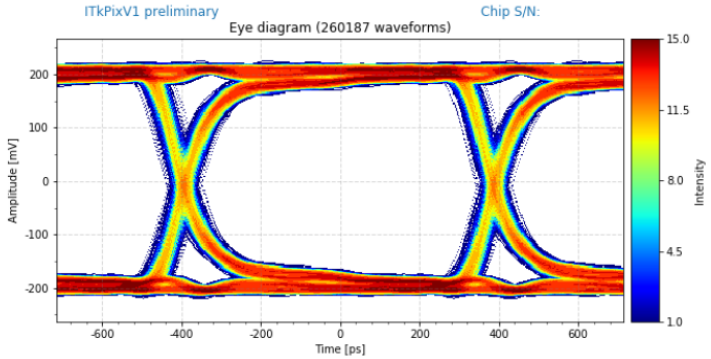
- **CDR/PLL greatly improved compared to RD53A in terms of jitter and start-up reliability**
- **Aurora output link stable with good quality**

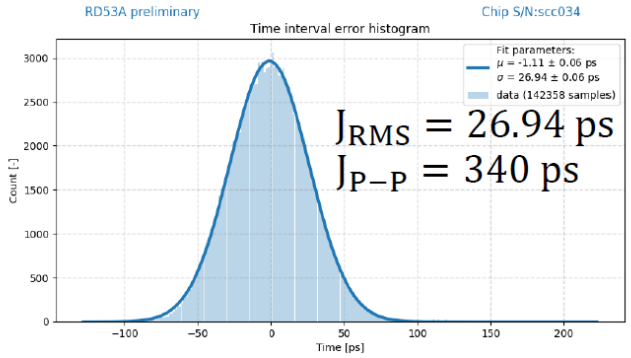
Input jitter = 5ps rms

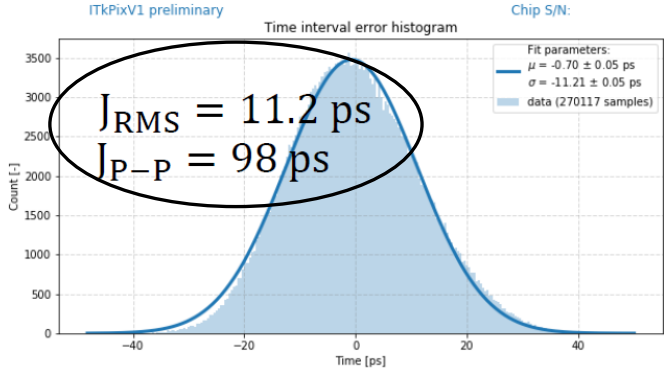
- **RD53A**
- Input: Threshold scan
- Output: Aurora (1.28 Gbps)

- **ITkPixV1**
- Input: PRBS5
- Output: Aurora (1.28 Gbps)





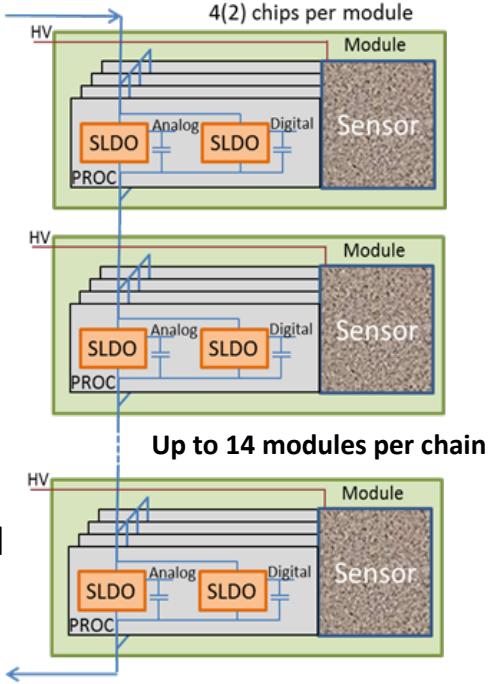


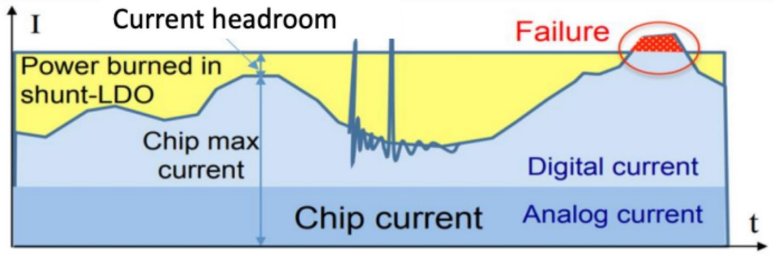


ShuntLDO for Serial powering

ATLAS and CMS will adopt for the upgrade pixel detectors a **serial powering scheme:**

- Based on **ShuntLDO** regulators in the readout chips (1 for Analog, 1 for Digital domain)
- **Constant input current Iin** is shared among chips (2÷4) on the same module (less cables)
- Modules are in serial chains: "recycle" current from one module to another
- I_{in} dimensioned to satisfy the highest load, with ~20% headroom for stable operation, absorbed by the Shunt device
- In case of chip failure, its current can be absorbed by the other chips of the module
- Not sensitive to voltage drops (low mass cables)
- On-chip regulated supply voltages, low noise
- Radiation hardness (> 500 Mrad) silicon proven
- **ItkPixV1 and CROCv1 testing show that ShuntLDO works well and system tests with pixel modules have started**

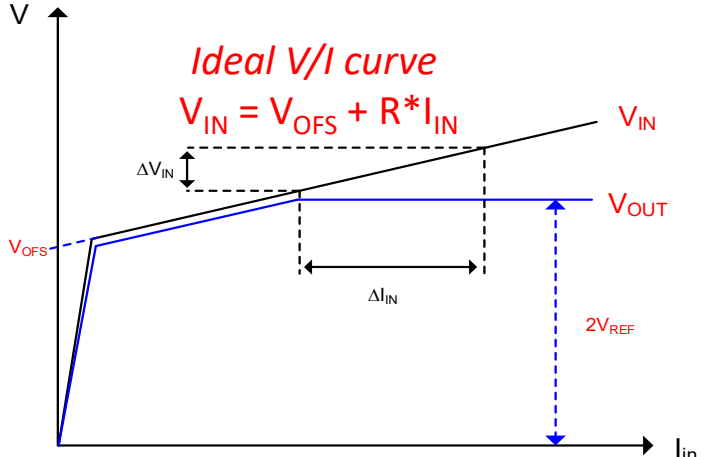




Example current consumption of one readout chip

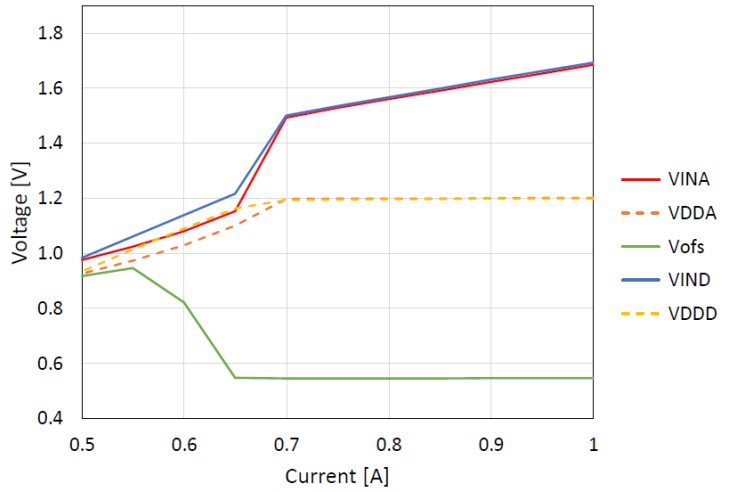
Protections:

- *Over-voltage protection*: V_{IN} clamped to 2 V
- *Under-shunt protection*: V_{OUT} decreased in case shunt current goes below a certain threshold (due to excess load current)



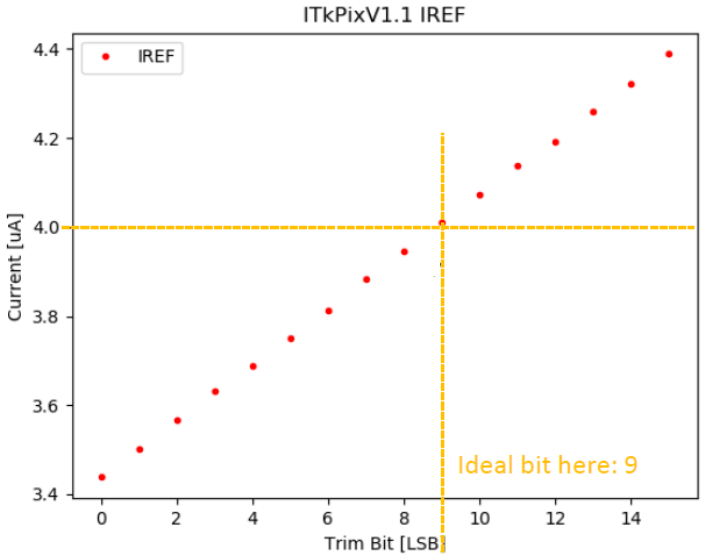
- V/I curve parameters (Voffset, slope) defined by external resistors
- V_{OUT} tunable by chip configuration

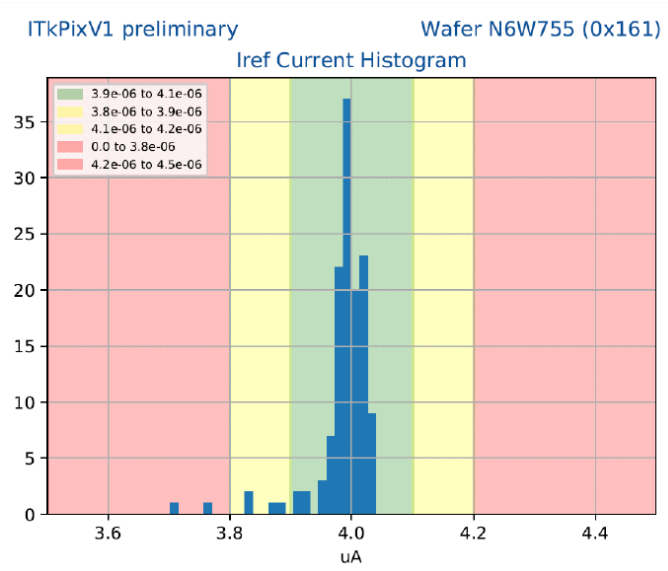
ITkPixV1.1 measurement at room T, pre-rad

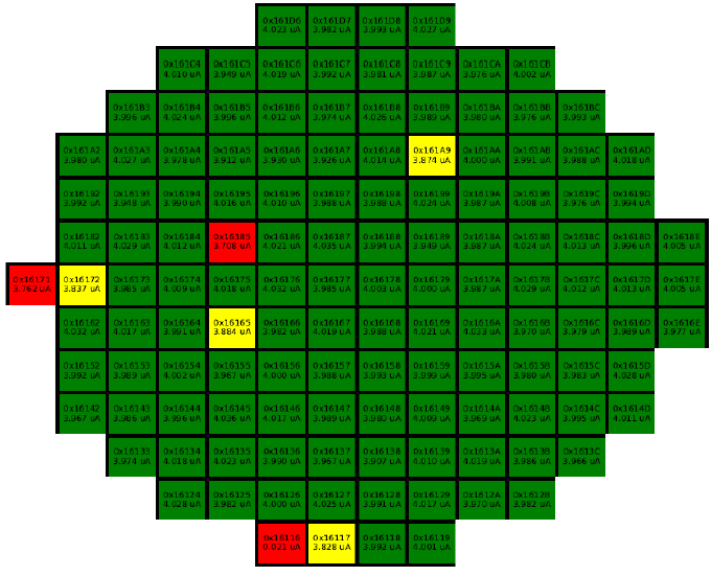


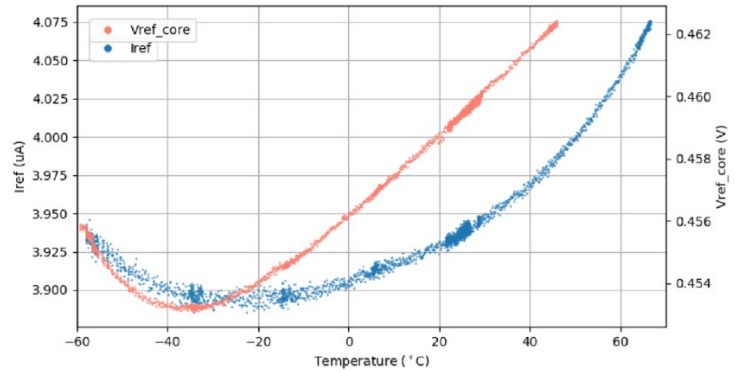
Bias circuit

- BIAS network is based on Bandgap reference circuits, to provide a reference voltage/current with low sensitivity to temperature variations
- Tuning by means of 4 wire-bond trimming pads (no risk of SEU bit flips), whose optimal value is found during **wafer probing**
- The tuned current I_{ref} is replicated and used as reference to 23 Digital-to-Analog converters to bias the analog Front-end, the CDR and other IPs

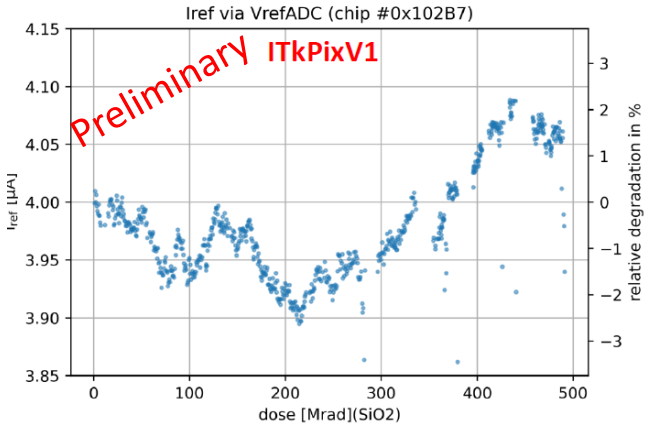






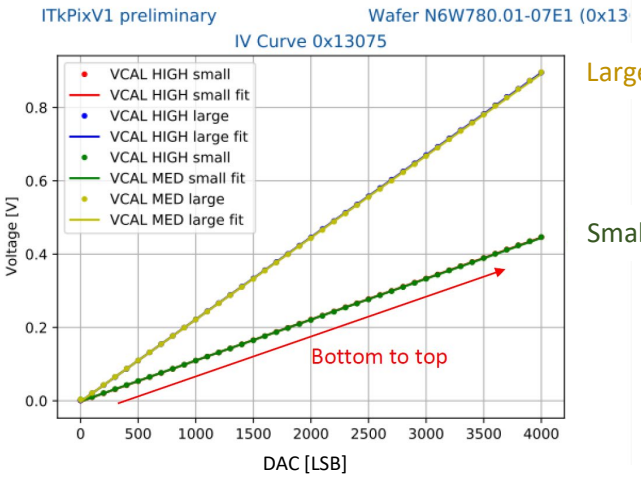


4% difference over
120°C temp. range



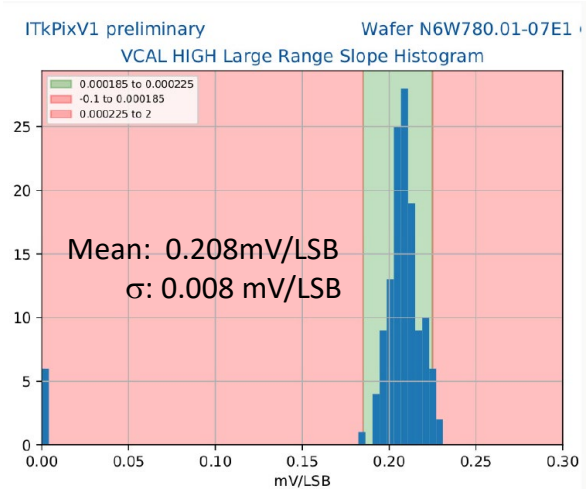
Calibration circuit

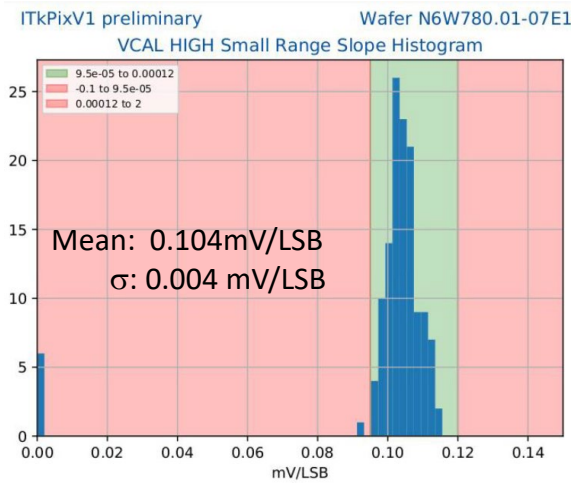
- Each pixel is equipped with a calibration injection circuit for test and calibration purpose
- The analog injection uses two distributed voltages, provided by two 12-bit voltage DACs, to generate a precise voltage step fed to an injection capacitor
- Two selectable ranges



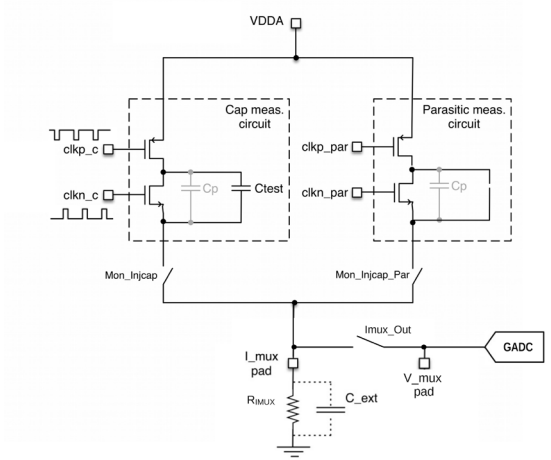
Large VCAL range

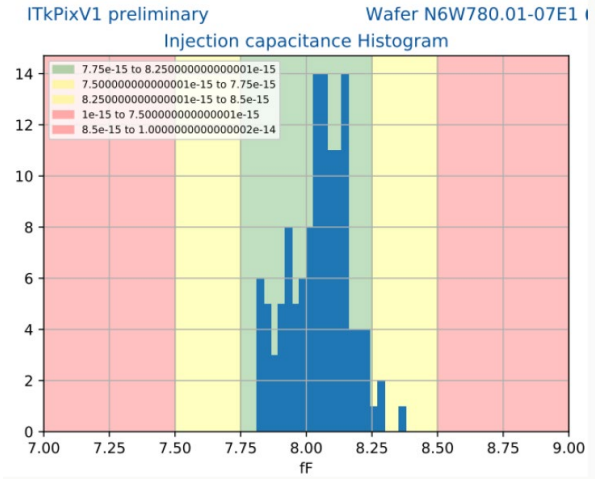
Small VCAL range





- Possibility to measure the value of injection capacitor using a dedicated circuit



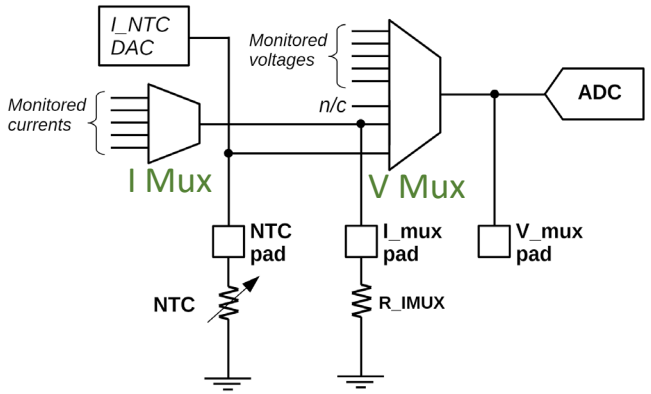


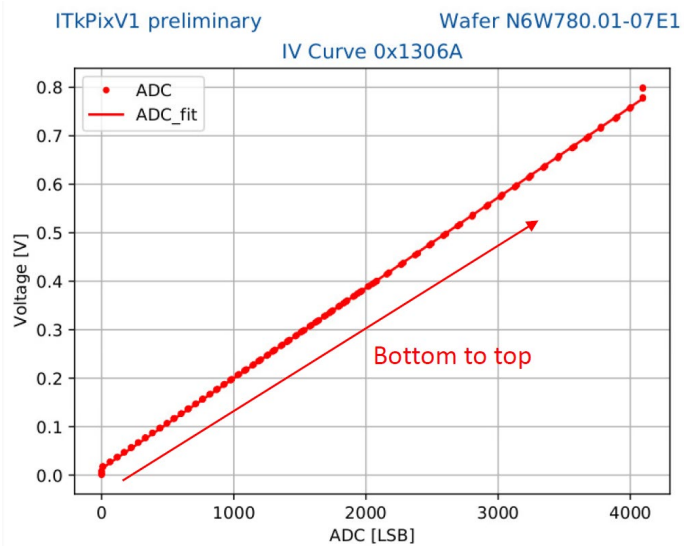
Mean: 8.05 fF (expected 8.02 fF)

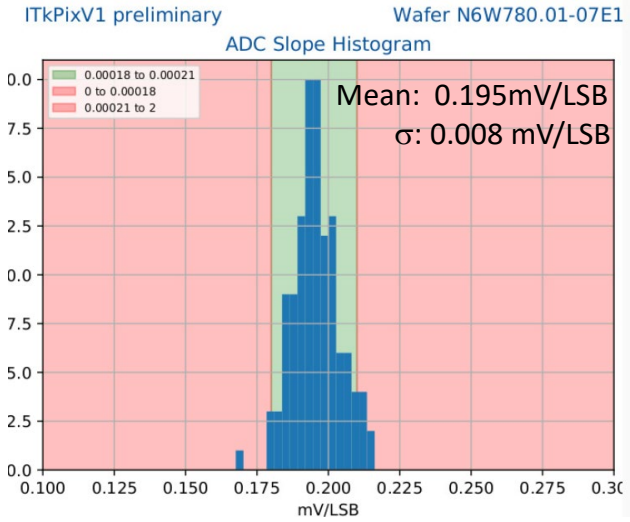
σ: 0.11 fF

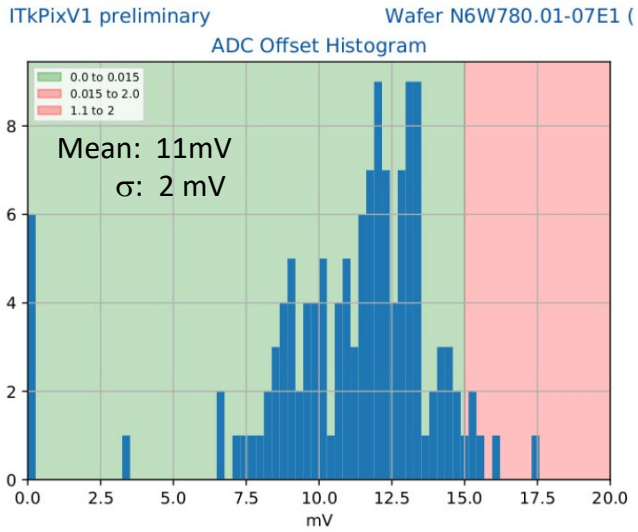
Monitoring block

- The Monitoring block enables digitization and readout of internal parameters (T, voltages and currents from different parts of the chip)
- Consists of a current mux, a voltage mux and a 12-bit Analog to Digital Converter (ADC)
- Monitoring can be performed at any time, also during data-taking, via the normal data output links
- 5 temperature sensors in different positions
- Ring oscillators → measurements of digital cells speed degradation with TID

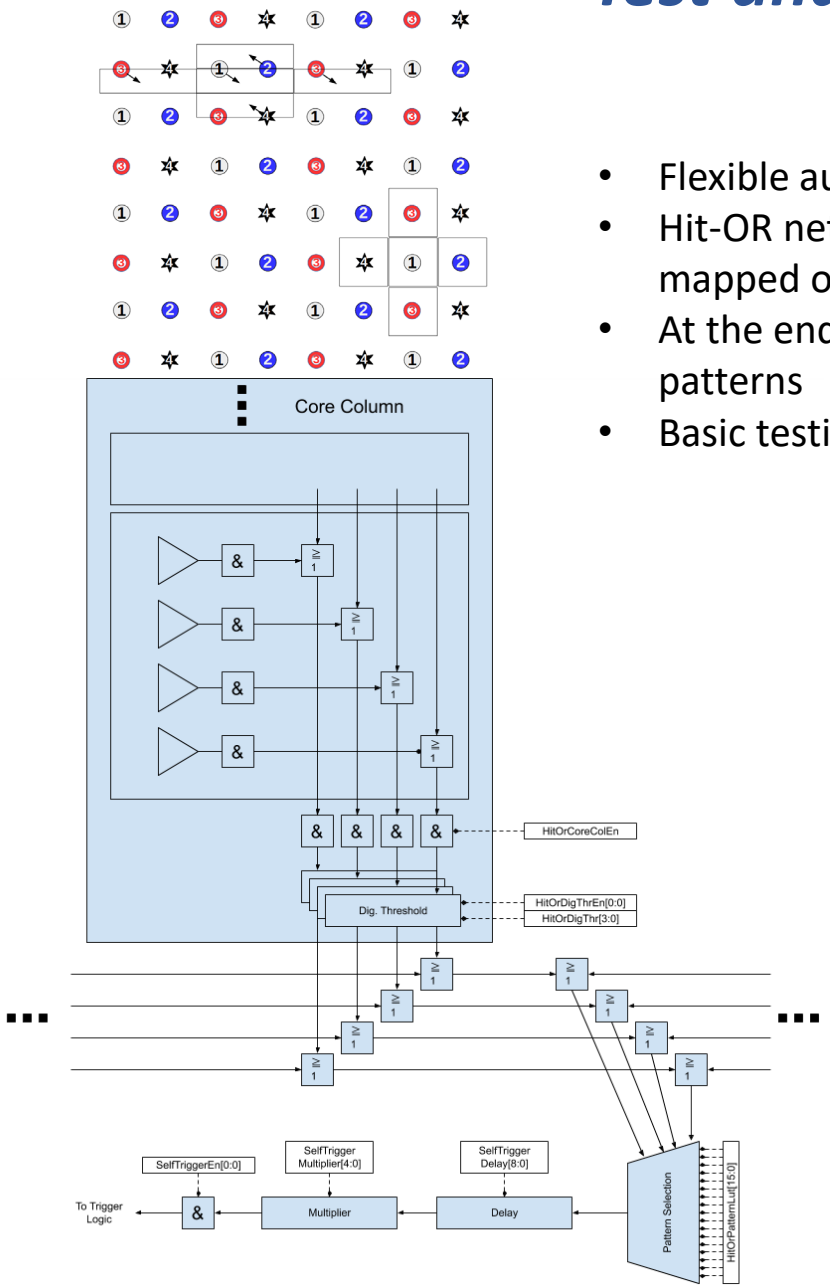




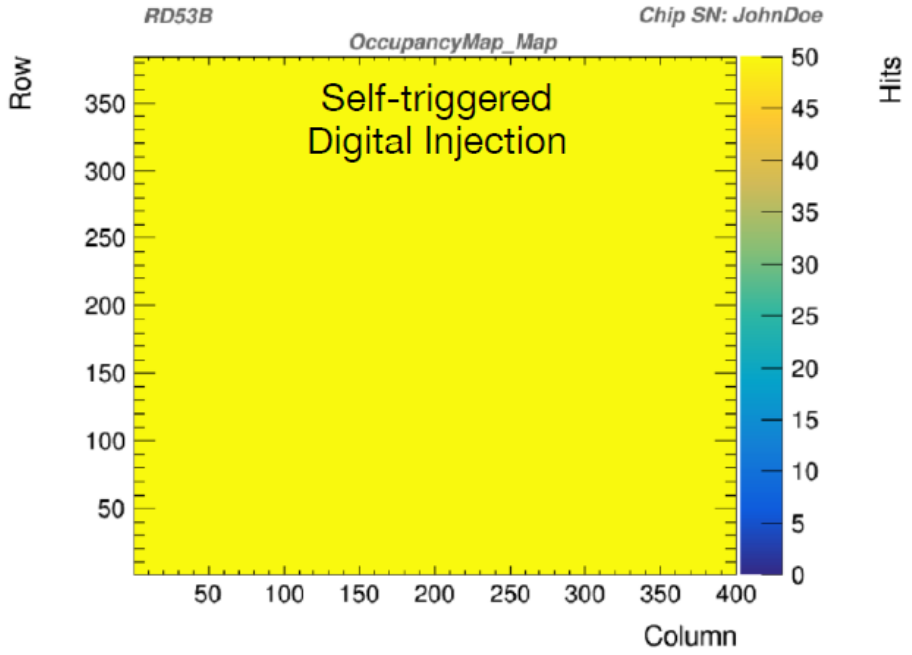




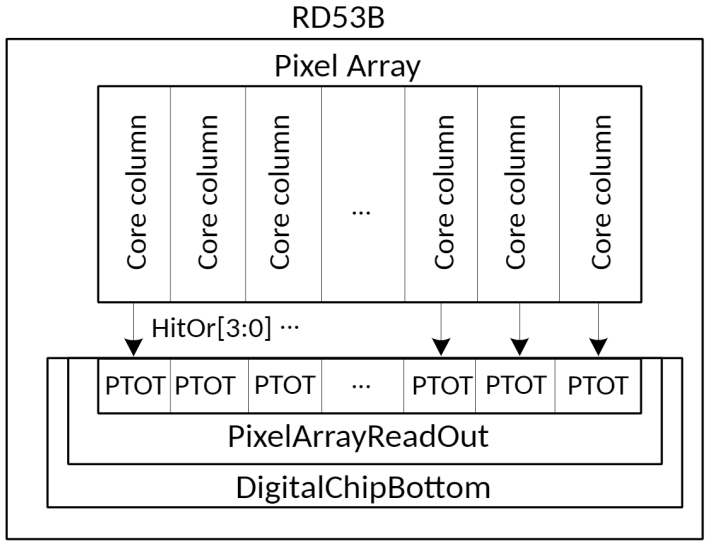
Test and debugging features: Self Trigger



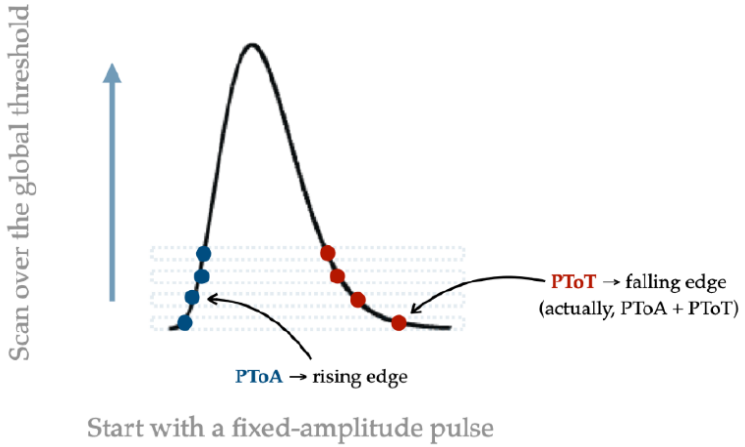
- Flexible auto trigger function, based on a Hit-OR network from the pixel array
- Hit-OR network consists of 4 OR lanes per Core Column, with a mapping such that neighbor pixels are mapped on different lines
- At the end of Core Column, the 4 lanes are combined to build the global Hit-OR with programmable patterns
- Basic testing with digital injection show that is **working as expected**



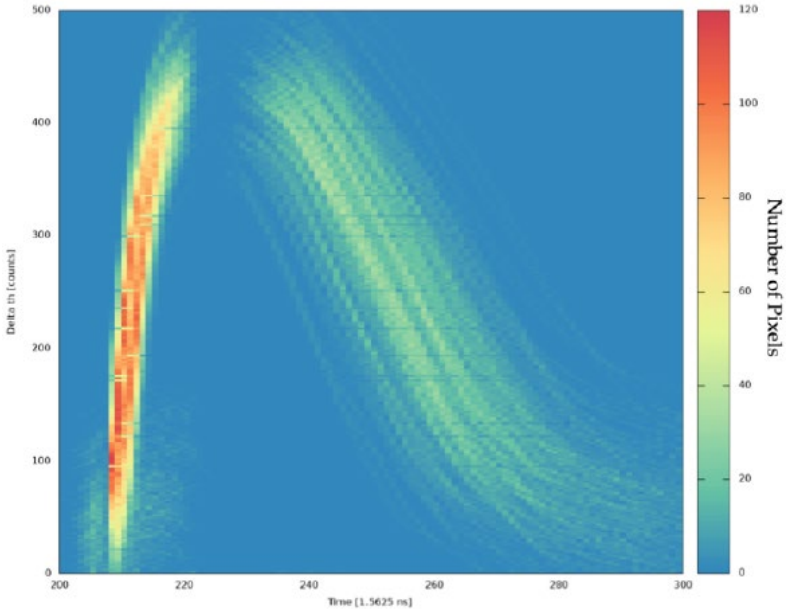
Precision ToT and ToA

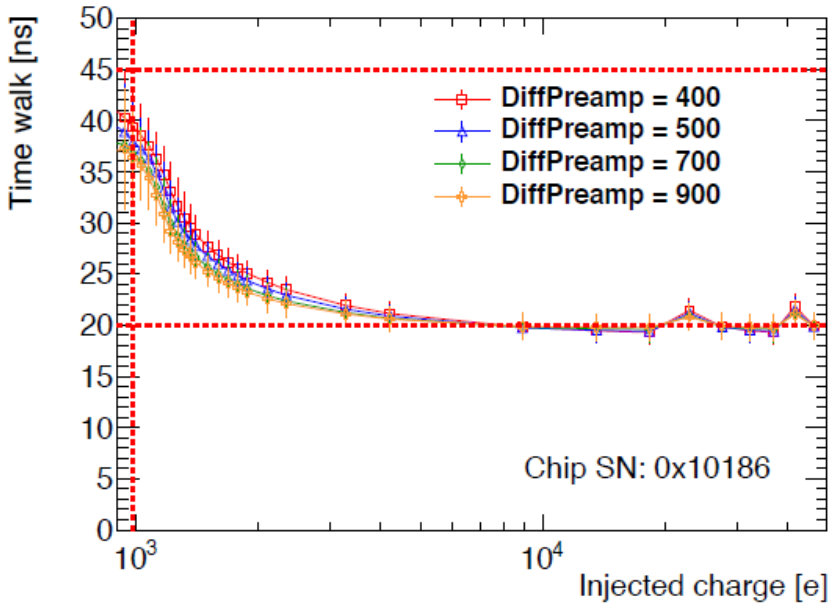


- PTOT module can be used for high resolution **Time over Threshold** and **Time of Arrival** measurement of the HitOR lines, using 640 MHz counting clock (1.5625ns resolution)
  - 11-bit PToT counters
  - 5-bit PToA counters, measuring the phase difference from HitOr leading edges and next BX clock rising edge
- Each Core Column is equipped with a PTOT module. Can be triggered for readout via the normal path, just like a Pixel Core
- Can be used to make precision measurements of analog front-end, like time walk
- Allows to reconstruct the amplifier output waveform (sort of oscilloscope)



- Inject fixed calibration pulse
- Scan the threshold
- Sample PToA and PToT at each step





Summary

- The readout chips for the ATLAS and CMS HL-LHC pixel detectors are being developed by the RD53 Collaboration
  - **INFN-BARI is contributing to the project with key responsibilities in the chip design and project management**

- RD53B is a configurable design in CMOS 65nm technology implementing **the same chip** in **two versions** having different sizes and different analog Front-ends

- RD53B-ATLAS (ITkPixV1) was submitted in March 2020. A bug in the ToT memory did not prevent its characterization and was corrected in the CMS chip

- RD53B-CMS (CROCv1) was submitted in June 2021. In addition to fixes for all known bugs, it also contains some additional features to improve calibration, monitoring and diagnostic.

- All measurements up to now indicate that the chips are generally working fine, with few other minor bugs that have been fixed for the final submissions.

- X-ray irradiations show that the chips should be capable to operate at least until TID= 1Grad

- SEU mitigation techniques seem effective to decrease the SEU rate. However a continuous refresh of the configuration memory (~ 1Hz) will be recommended

- Final production chips are expected be submitted in April 2022 (ATLAS) and September/October 2022 (CMS)

BACKUP

RD53C organization (on Jan. 2022)

Collaboration board chair:
Lino Demaria, Torino

Interface to experiments: Co-spokespersons
Jorgen Christiansen, CERN (CMS) ,
Maurice Garcia-Sciveres, LBNL (ATLAS)

Experiment observers
Duccio Abbaneo, CERN (CMS) ,
Kevin Einsweiler, LBNL (ATLAS)

RD53 design framework: Flavio Loddo, Bari, Tomasz Hemperek, Bonn

Floorplan/integration:
Flavio Loddo, Bari

Analog front-ends:
CMS: Luigi Gaioni, Bergamo/Pavia:
ATLAS: Amanda Krieger, LBNL,
Aikaterini Papadopoulou, LBNL

Monitoring:
Mohsine Menouni, CPPM;

IO PAD frame:
Hans Krueger, Bonn

Digital:

RTL, Design flow, P&R, Timing:
Tomasz Hemperek, Bonn;
Roberto Beccherle, Pisa
Luca Pacher, Torino

Simulation & Verification:
Jaya John, Oxford;
Stefano Esposito, CERN
Attiq Rehman, Bergen,
Alessandra Fioriti, Milano

Design for testability:
Giuseppe De Robertis, Bari

SEU/SET
Rafael Girona, Seville
Wojciech Bialas, CERN
Fernando Munoz Chavero, Seville

Serial Powering:
Michael Karagounis, Dortmund
Alvaro Pradas, ITAINNOVA

IPs: Support and possible updates
Current DAC: Bari
Voltage DAC: Prague
Bandgaps: Bergamo
ADC, mux, temp: CPPM
PLL & serializer: Bonn
Diff IO: Bergamo/Pavia
Power on reset: Seville
Ring oscillator: LAL
Analog buffer: RAL

Testing

Organization: ATLAS: Timon Heim, LBNL, CMS: Stella Orfanelli, CERN
Many RD53 and ATLAS/CMS groups: LBNL, Bonn, Oxford, CERN, CPPM, LAL, Torino, Aragon, ETH, Florence, Zurich , , ,
RD53 test systems: YARR (LBNL), BDAQ53(Bonn)

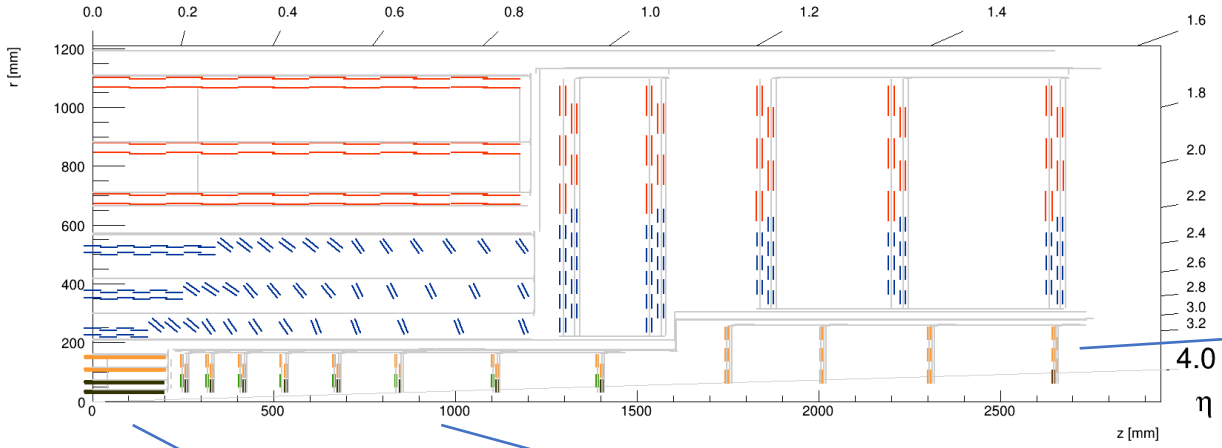
Requirement and documentation

https://cds.cern.ch/record/2663161

Technology	65nm CMOS
Pixel size	50 µm x 50 µm
ATLAS (CMS) pixel rows/columns	384 (336) / 400 (432)
Detector capacitance	< 100 fF (200fF for edge pixels)
Detector leakage	< 10 nA (20nA for edge pixels)
In-time threshold	< 1200 e-
Noise hits	$< 10^{-6}$
Hit rate	< 3 GHz/cm^2 (75 kHz avg. pixel hit rate)
Trigger rate	≤ 4 MHz (trigger only, without readout)
Trigger latency (L0)	≤ 12.5 µs (programmable)
Readout latency (L1)	≤ 25 µs
Manual readout rate	≤ 1 MHz
Hit loss (in-pixel pile-up + other sources)	≤ 2%
Charge resolution (Time over Threshold)	4 bits ToT (also 6-to-4 dual slope mapping)
Readout data rate	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
Radiation tolerance	≥ 500 Mrad, 1 10^{16} 1Mev n.eq/cm^2 (at -15°C)
SEU	< 0.05 /hr/chip at 1.5GHz/cm^2 particle flux
Power consumption at max hit/trigger rate	< 1W/cm^2
Temperature range	-40°C ÷ 40°C

- RD53B Design manual and user guides: https://cds.cern.ch/record/2665301
- RD53B requirements: https://cds.cern.ch/record/2663161

CMS IT Mechanical Structures



TEPX

Tracker Barrel PiXel
4 layers

TBPX

Tracker Extension PiXel
4 disks

TFPX

Tracker Forward PiXel
8 disks

CMS IT Electronics System

- Disk system tests with RD53A modules
  - **TFPX R1 topology**
    - Four **digital** quad modules
    - Powered serially through the Al flex
    - Readout with ring flex (20 differential pairs + 2 for testing)
    - Demonstrated combination as potential solution: Cu ring flex readout on top of Alu power flex
  - **TEPX disk R1 & R3 topologies**
    - Five **digital** quad modules for R1 and nine for R3
    - Powered serially through the disk PCB
    - Readout with traces on the disk
    - Threshold trimming and noise level as good as in single modules
    - BER studies ongoing with good preliminary results
- **Switching to complete RD53A demo modules for further system tests**
  - **Delays due to demo module availability**
  - **Final serial powering validation delayed by CROC submission delay**
    - By about 6 months