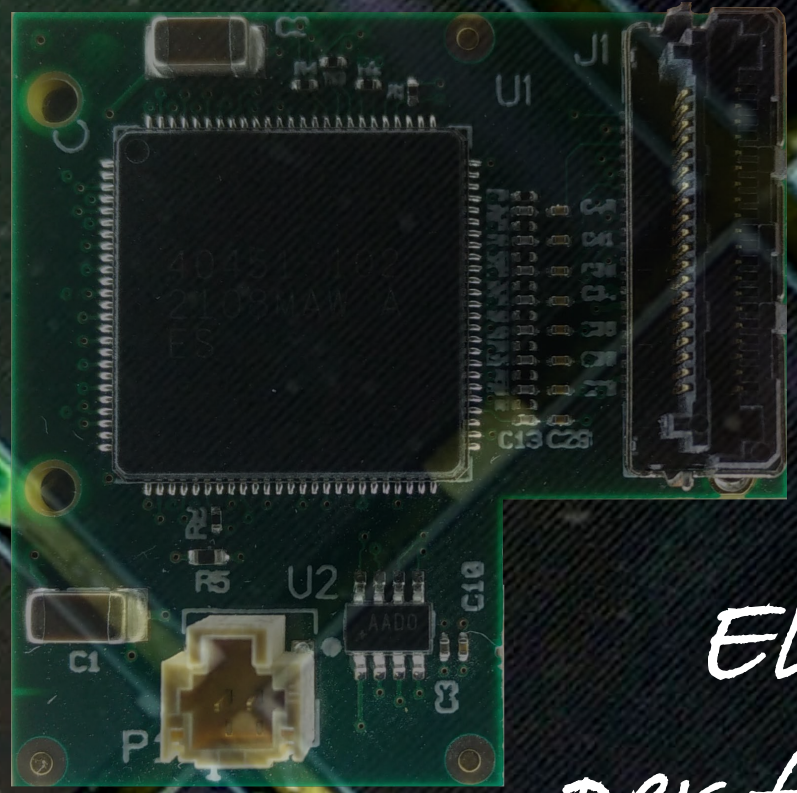
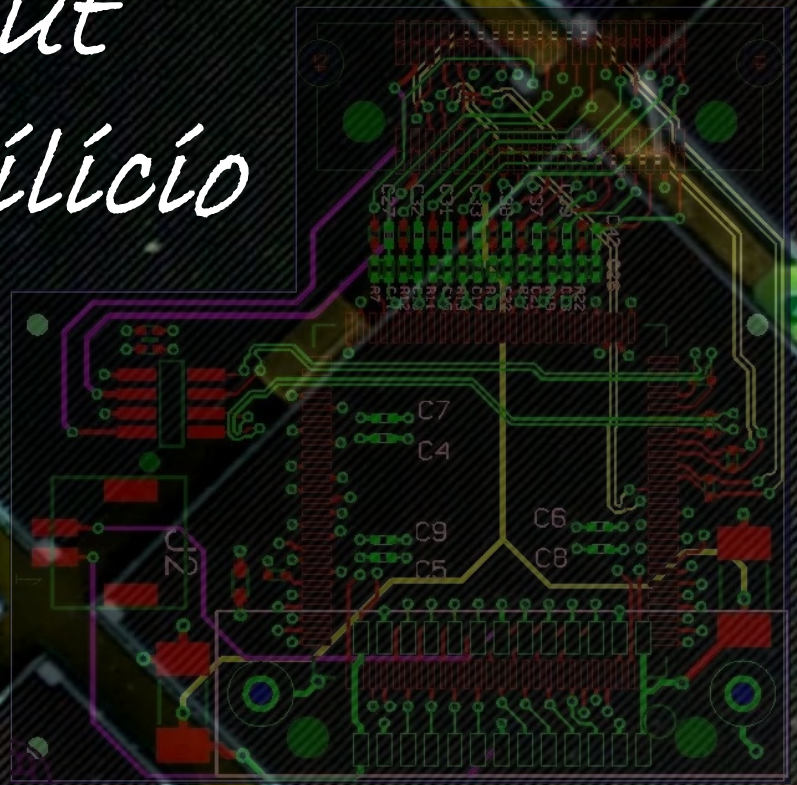


Elettronica di readout per foto-rivelatori al Silicio

F. Licciulli
francesco.licciulli@ba.infn.it



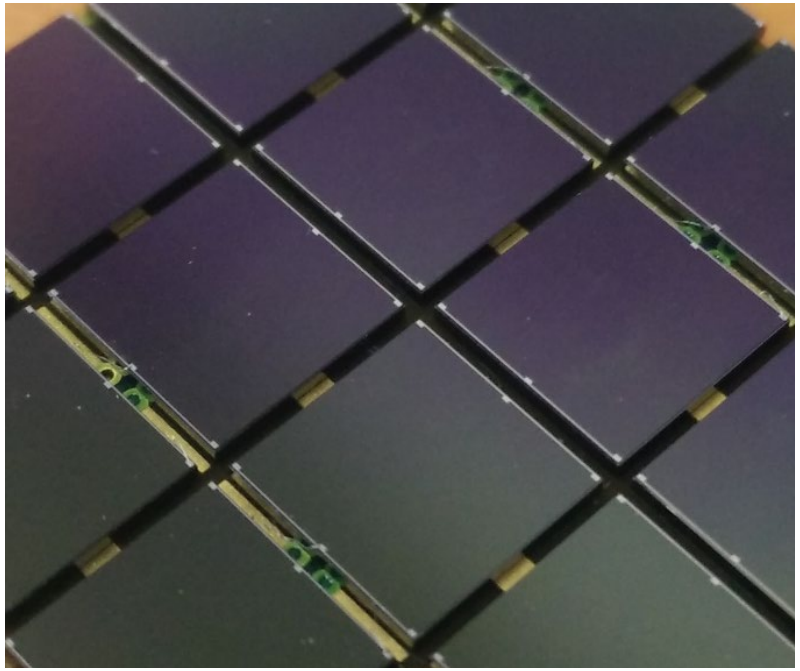
Outline

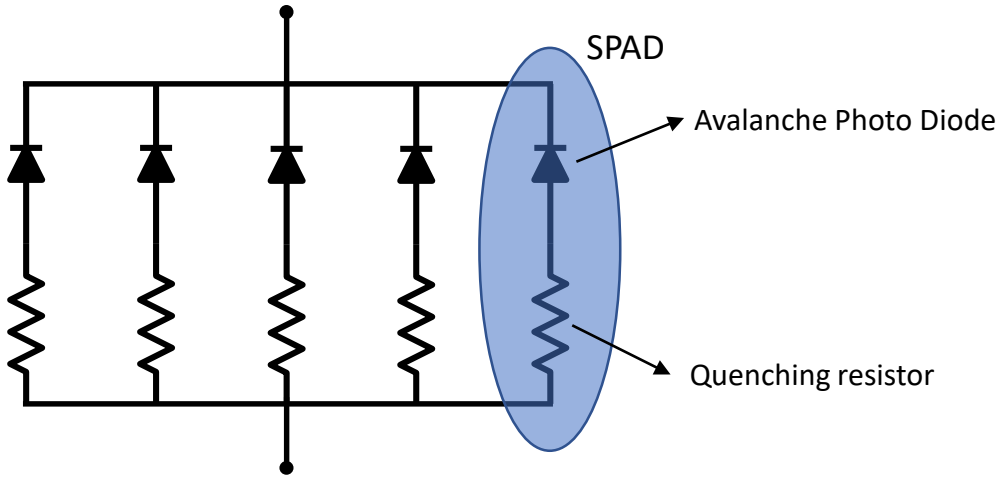
- Silicon PhotoMultiplier: structure and working principle
- SMART2: an ASIC for the CTA experiment
- PETIROC_FEB: a front-end board for general applications
- Future perspectives

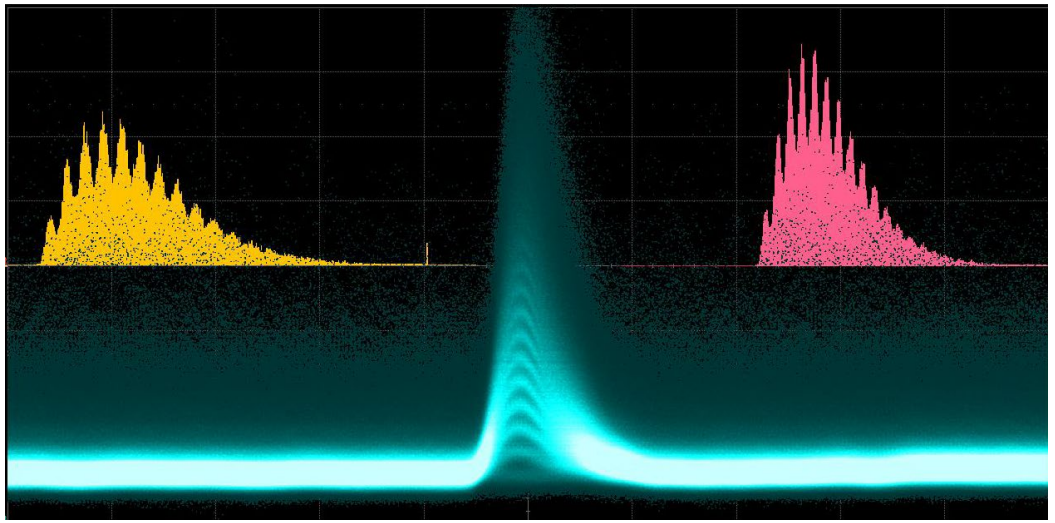
Silicon PhotoMultiplier

Silicon PhotoMultiplier (SiPM):

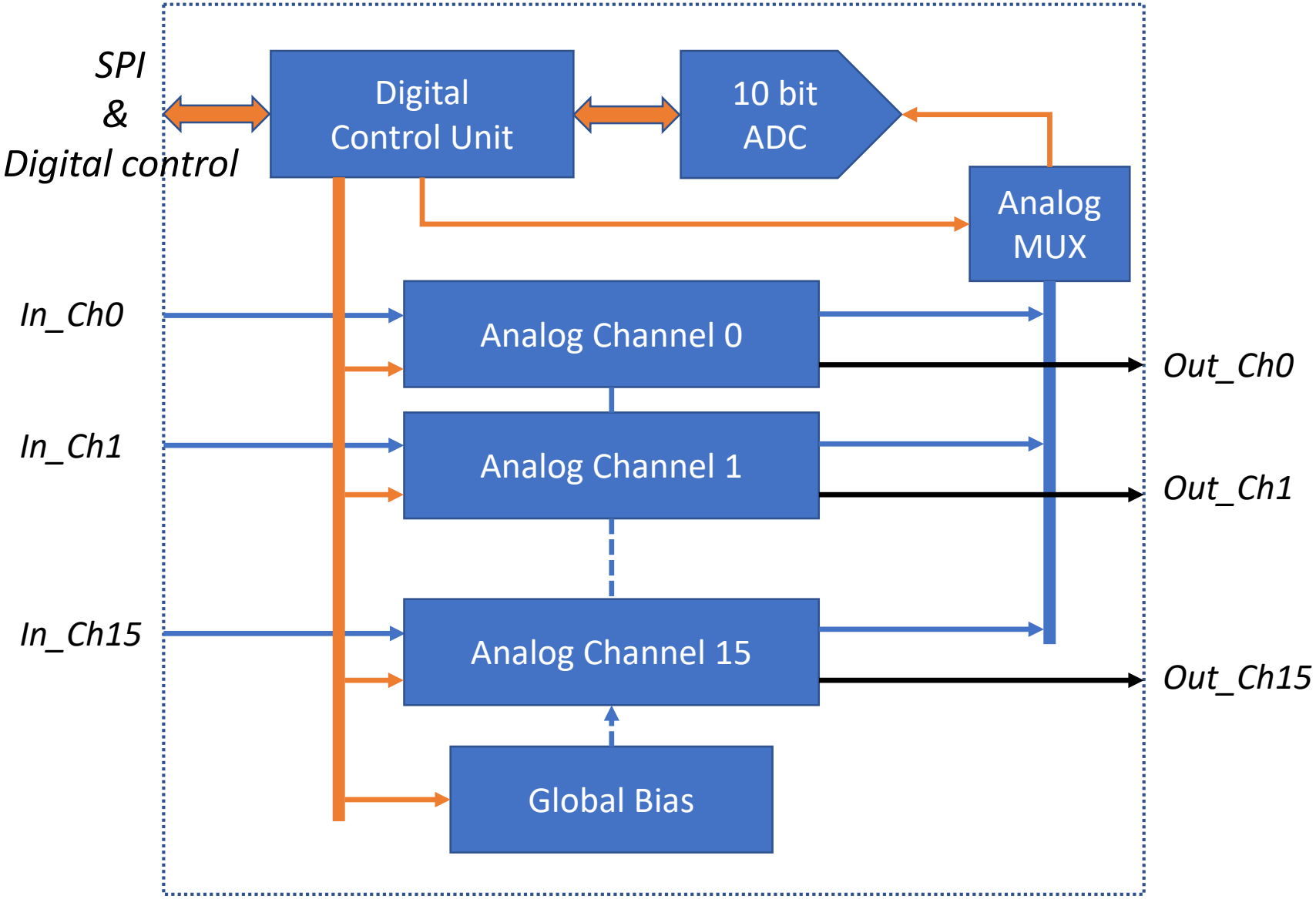
- Matrix structure of microcell connected in parallel
- Microcell: SPAD (Single Photon Avalanche Diode) operating in Geiger mode
- SPAD: it detects the single photon producing a current pulse whose charge in controlled by the SiPM bias point
- The SiPM output is a fast rising edge current pulse whose charge is proportional to number of detected photons







SMART2: ASIC architecture overview



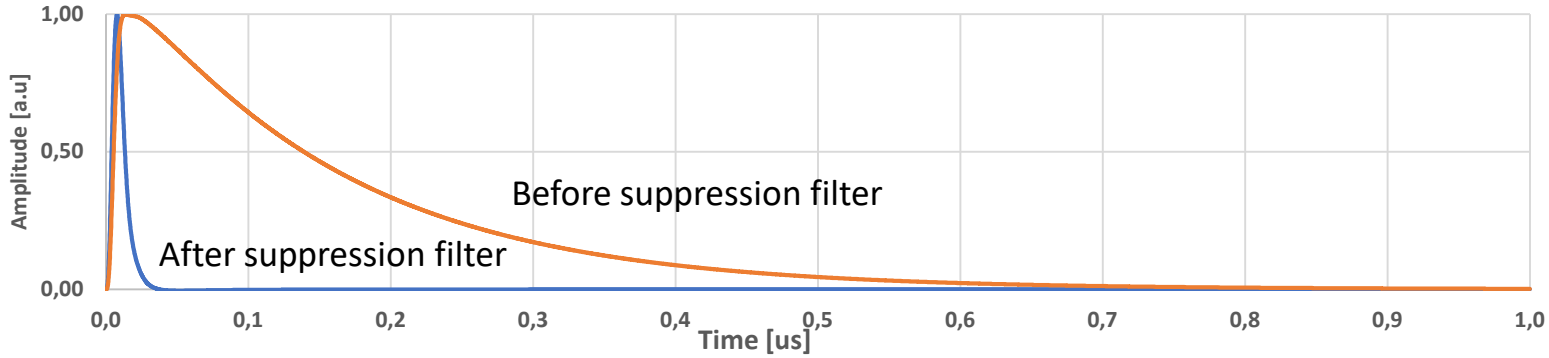
Analog Section:

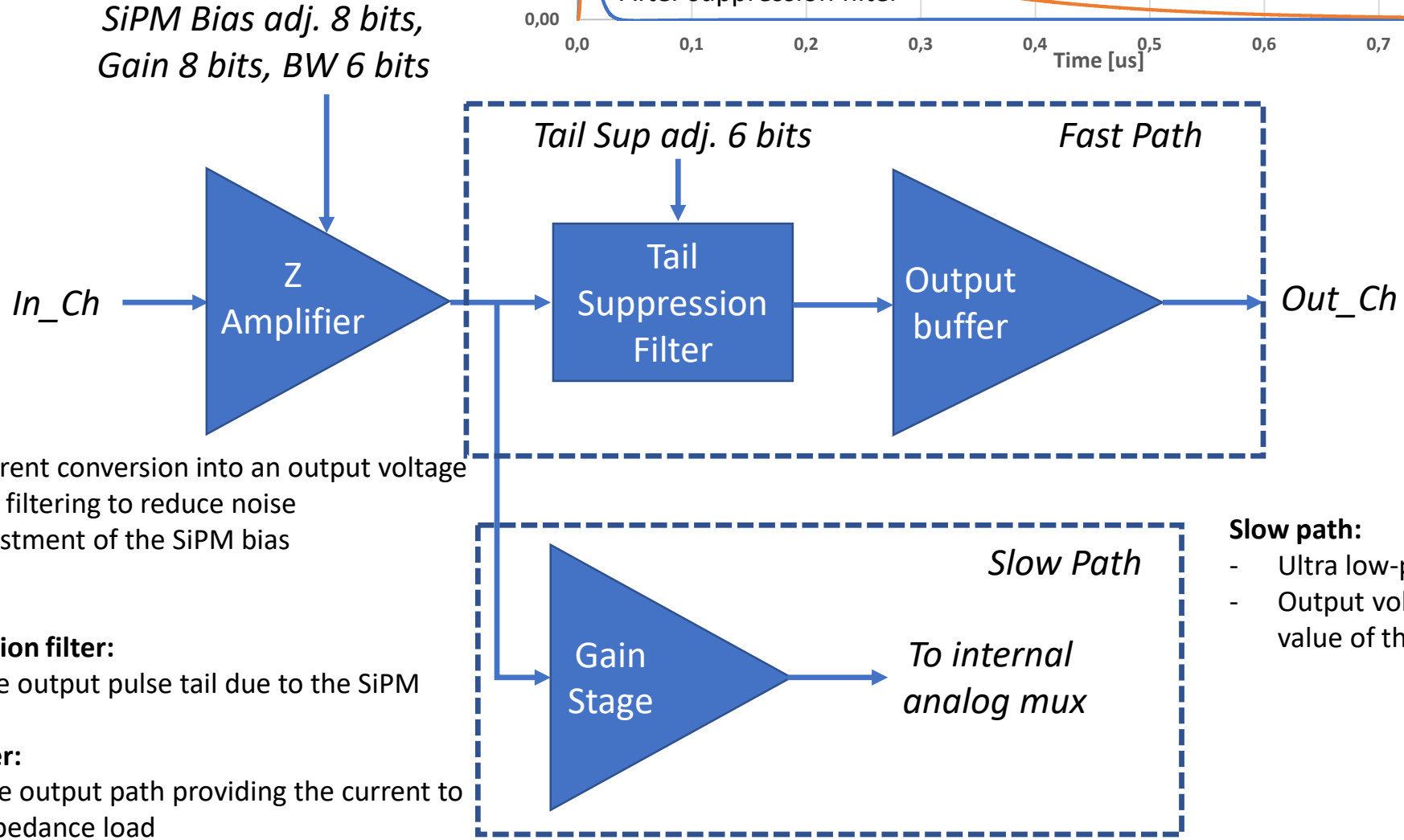
- 16 Front-end channels:
  - Direct output: designed for photon-counting
  - Internal output: SiPM mean current measurement
- Global Bias: temperature and power supply independent
- 10 bit 1MHz SAR ADC for channel internal output conversion

Digital Section:

- Control Unit:
  - 1MHz SPI LVDS link
  - Channel & Global bias adj. bits
  - ADC control

SMART2: Channel architecture overview





Z-Amplifier:

- Input current conversion into an output voltage
- Low pass filtering to reduce noise
- Fine adjustment of the SiPM bias

Fast Path

Tail suppression filter:

- Filters the output pulse tail due to the SiPM recovery

Output buffer:

- Drives the output path providing the current to a low impedance load

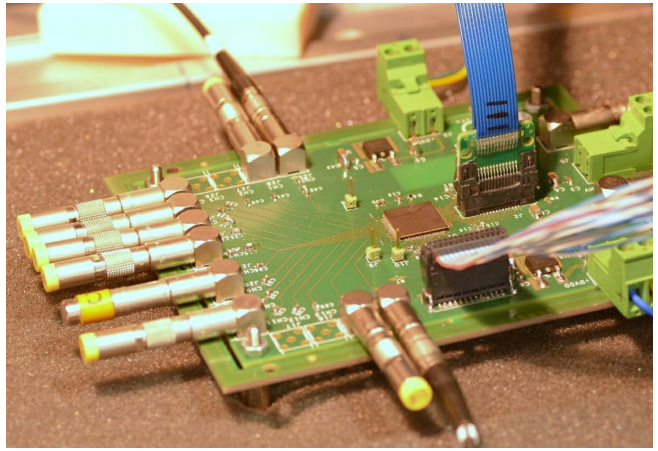
Slow path:

- Ultra low-pass voltage amplifier
- Output voltage proportional to the mean value of the SiPM current

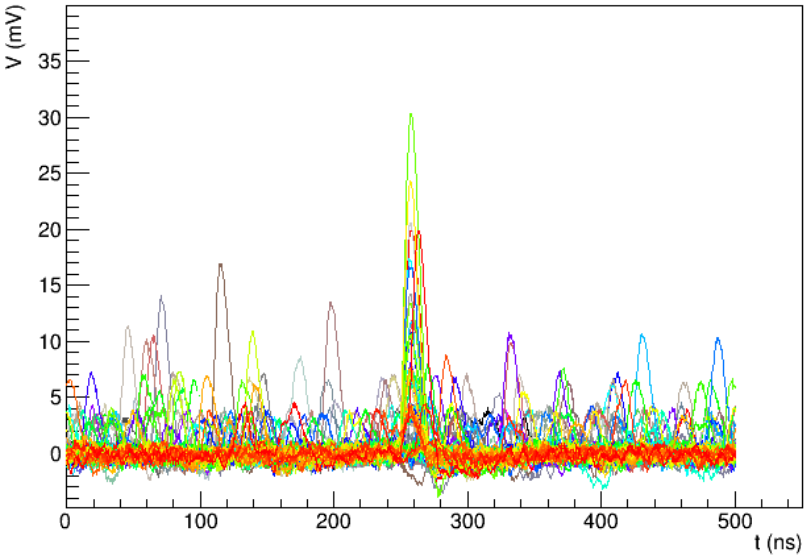
SMART2 characterization tests: Fast Path

Characterization setup:

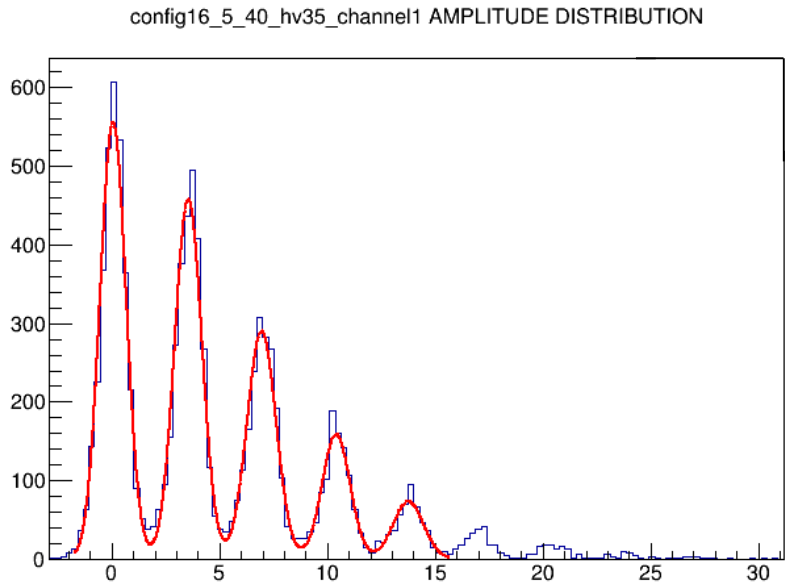
- PCB designed ad-hoc for testing
- PCB with FPGA for remote control: SMART2 configuration
- Oscilloscope
- Laser in pulse mode
- SiPM bias power supply with pico-ammeter
- Acquisition & elaboration software



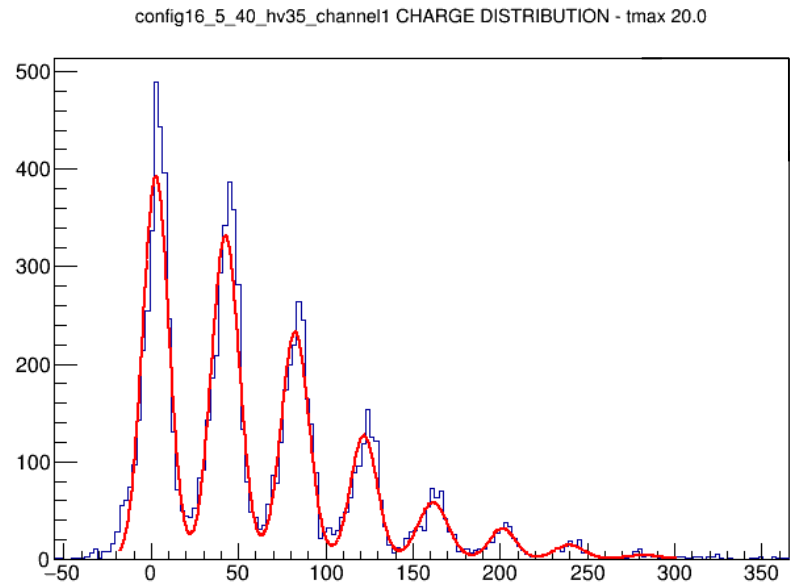
Measurement conditions: SiPM FBK NUV-HD 6x6 mm^2, 35 V bias voltage, SMART2 conf. R = 16, C = 5, PZ = 40



Fast-path output waveforms

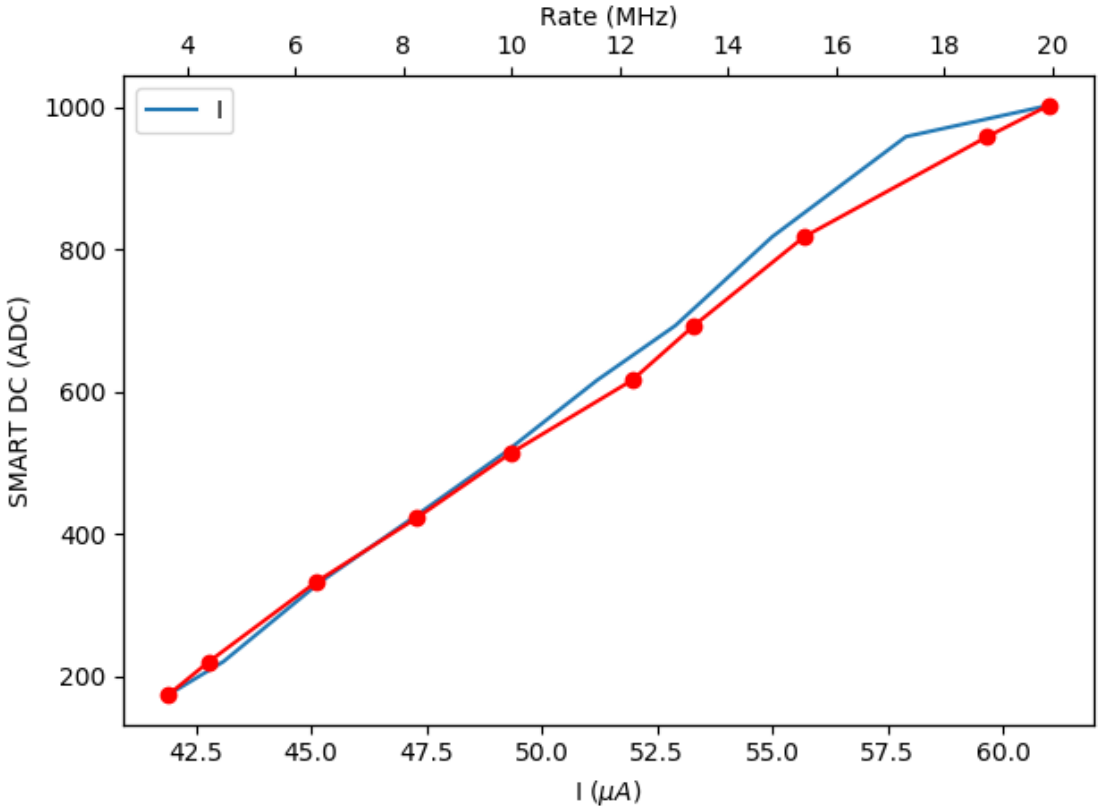


Amplitude distribution: Gain= (3.44 ± 0.01) mV/pe
SNR= 5.64 ± 0.09

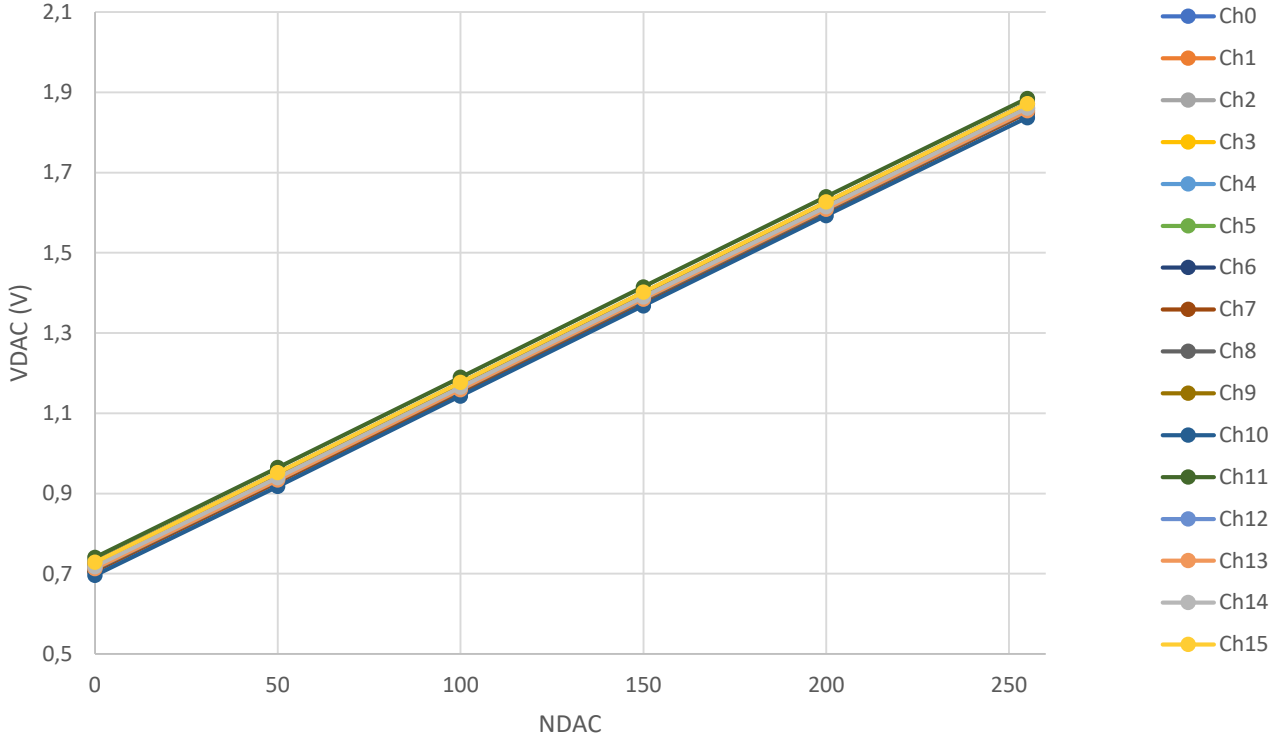


Gain= (39.72 ± 0.12) mV*ns/pe
SNR= 5.30 ± 0.07

SMART2 characterization tests: Slow Path & SiPM bias adj.



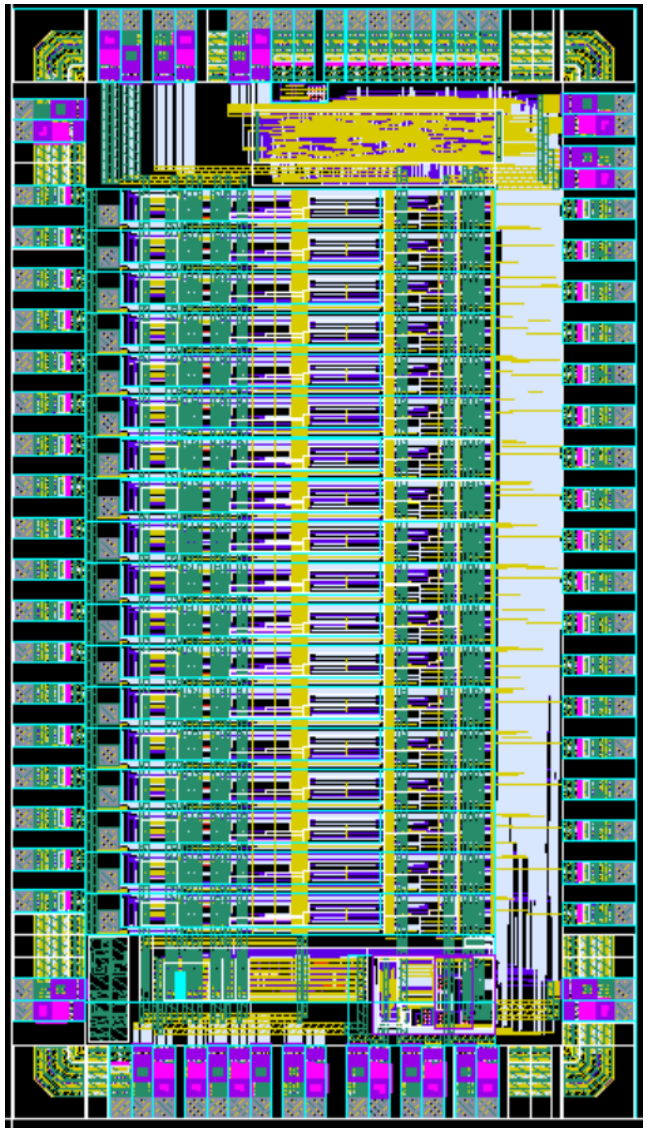
Slow-path measurements for a single channel, laser in continuous mode: max pulse rate 20 MHz



Channel input voltages as a function of the DAC configuration

SMART2 features

- AMS 0.35 μm SiGe technology node
  - 3.3 V power supply
  - Die size: 2.9 mm x 5.1 mm
- 16 front-end channels
  - Input impedance ≈ 12.5 Ω
  - Current consumption: 5 mA
- 20-bit global adjustment: gain (8 bits), bandwidth (6 bits), PZ (6 bits)
  - Gain at the Fast Path output: 0.5 mV/pe ÷ 3.5 mV/pe
  - FWHM at the Fast Path output: 8 ns ÷ 20 ns
- 8-bit DAC for SiPM bias adjustment (one per channel):
  - 1.2 V adjustment range
- Slow monitoring of SiPM mean current (16 channels multiplexed)
  - Rate resolution: 20 kHz/LSB ⇔ Current resolution: 25 nA/LSB
- 10-bit ADC
- 1 MHz SPI interface

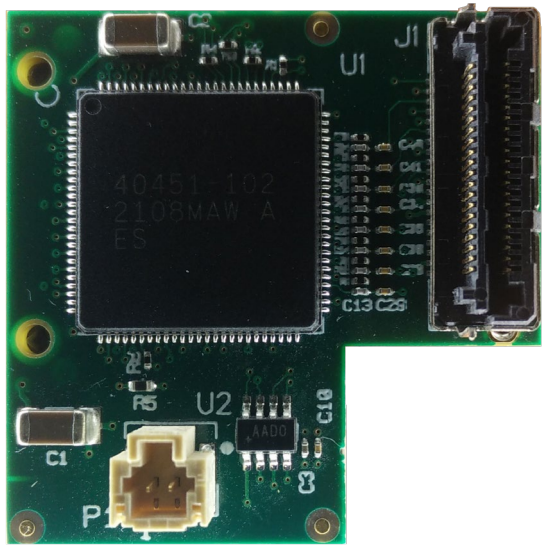


SMART2 layout

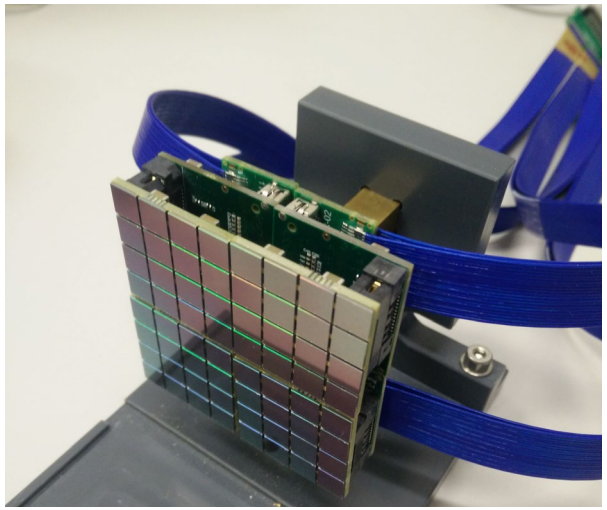
SMART2 for the CTA experiment

SMART2 for CTA telescope (talk by L. Di Venere):

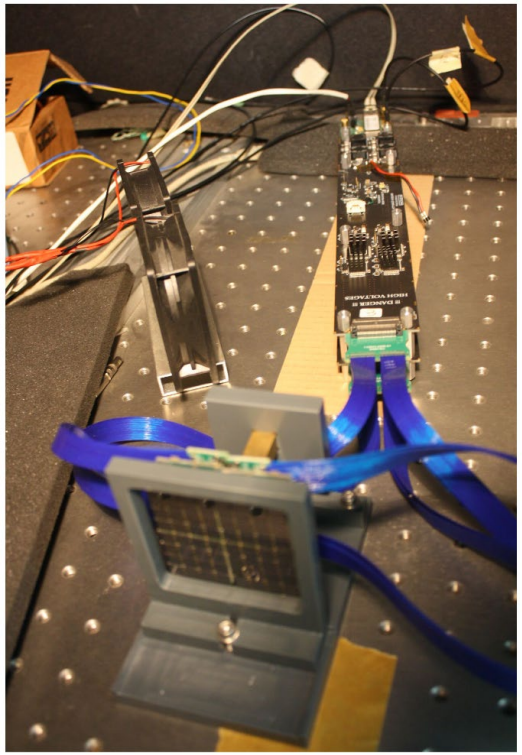
- 1000 SMART2
- 1000 front-end boards
- Semi-automated test stand for mass production test
- 750 front-end boards assembled and tested



SMART2 front-end board

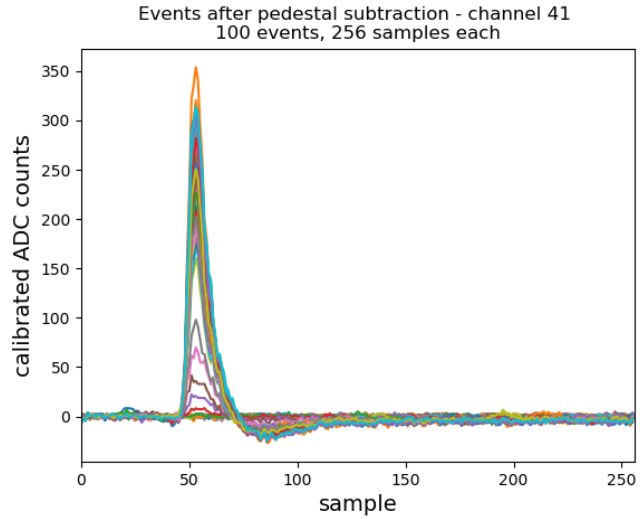


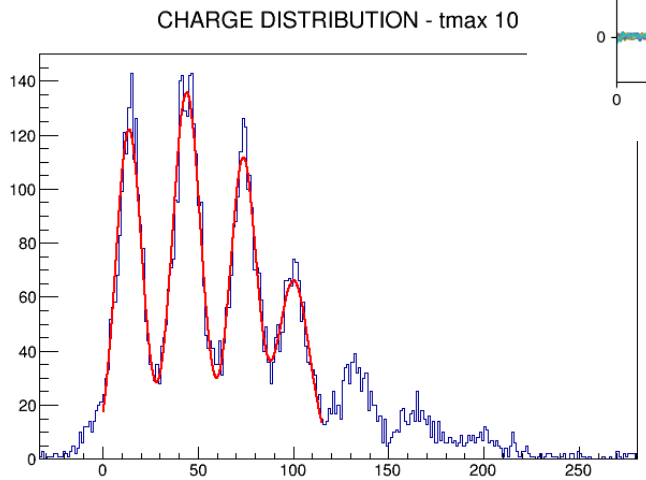
Front-end boards coupled to SiPM matrixes



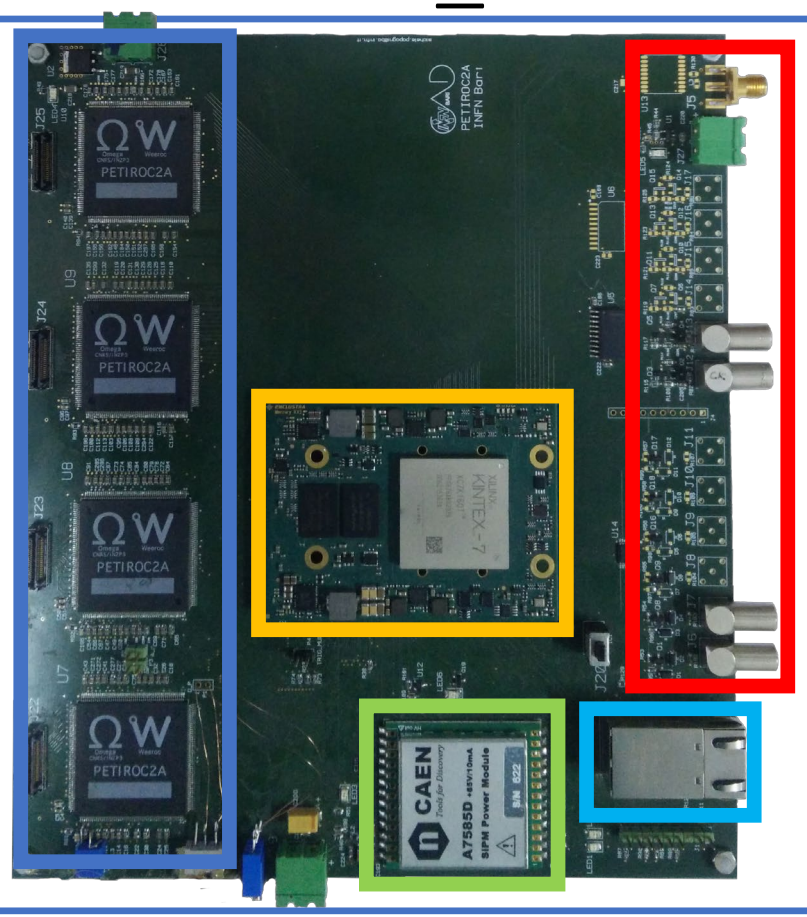
Quality control setup

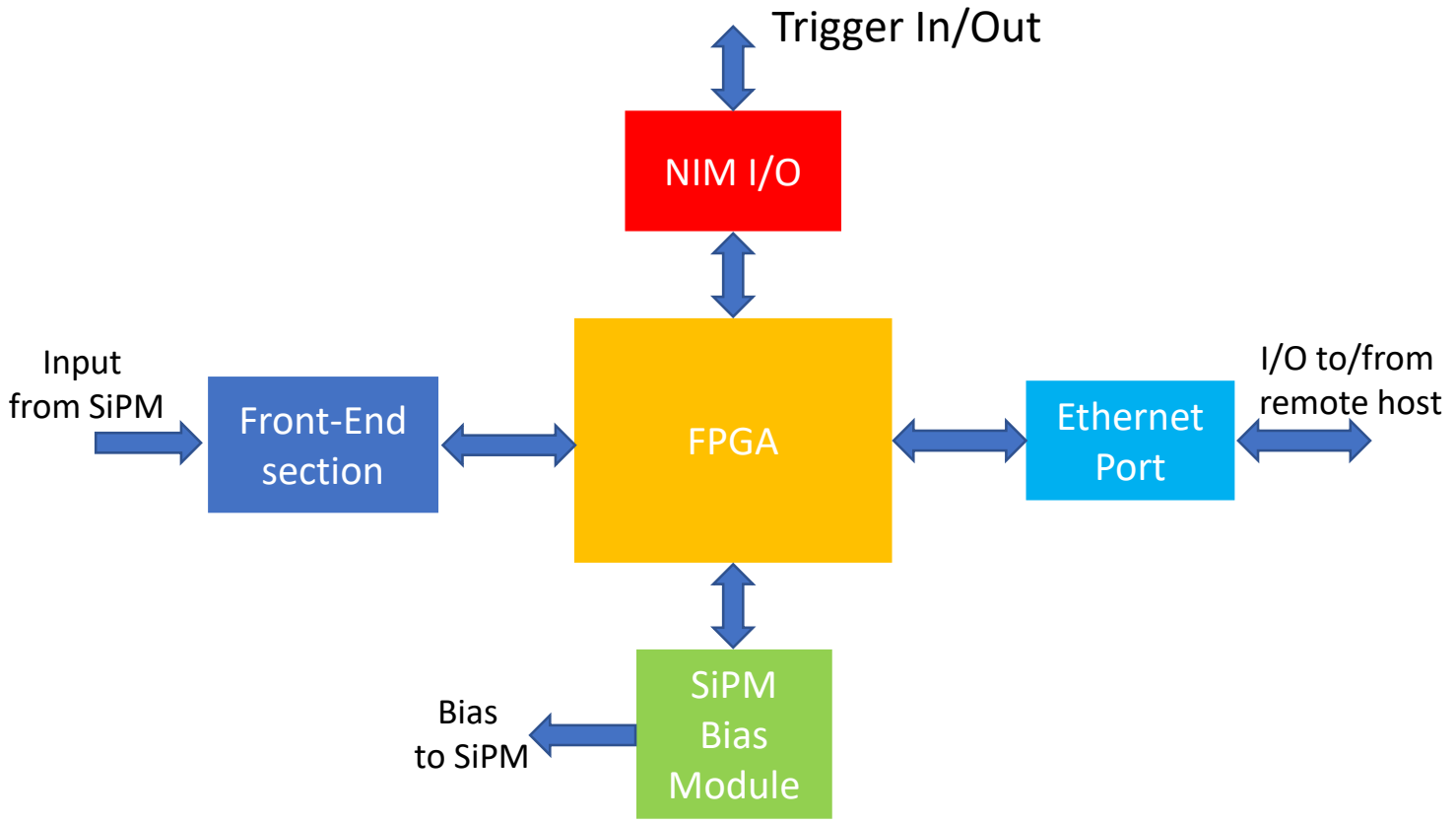
CTA camera acquisition and control module





PETIROC_FEB: Architecture overview





Front-End
- 4 PETIROC ICs:
  - 32 front-end channels
  - ADC for charge measurements
  - TDC to measure the arrival time
  - 32 digital outputs for triggering

FPGA:
- I/O data managment
- Trigger
- Coincidence

SiPM Bias Module:
- SiPM bias voltage regulation up to 80 V

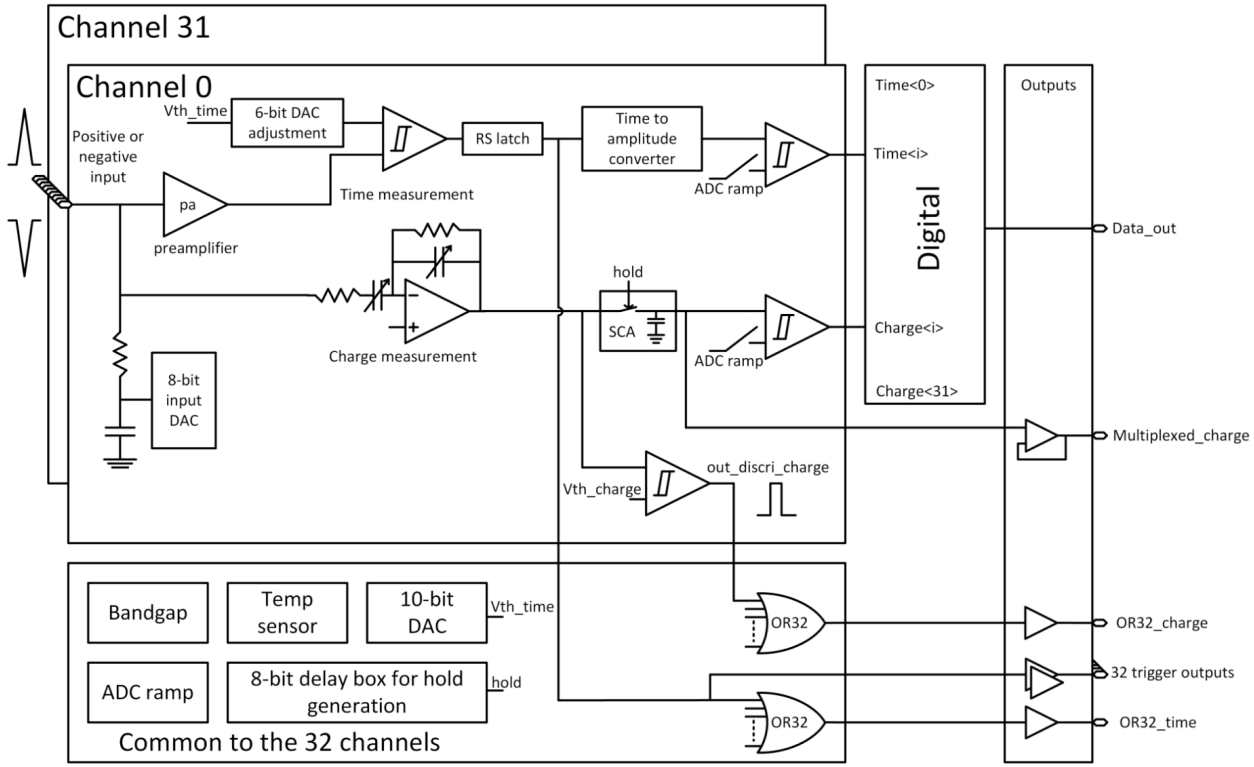
Ethernet port
- Data I/O to a remote host

NIM I/O
- Trigger

PETIROC: chip architecture

Analogue section:

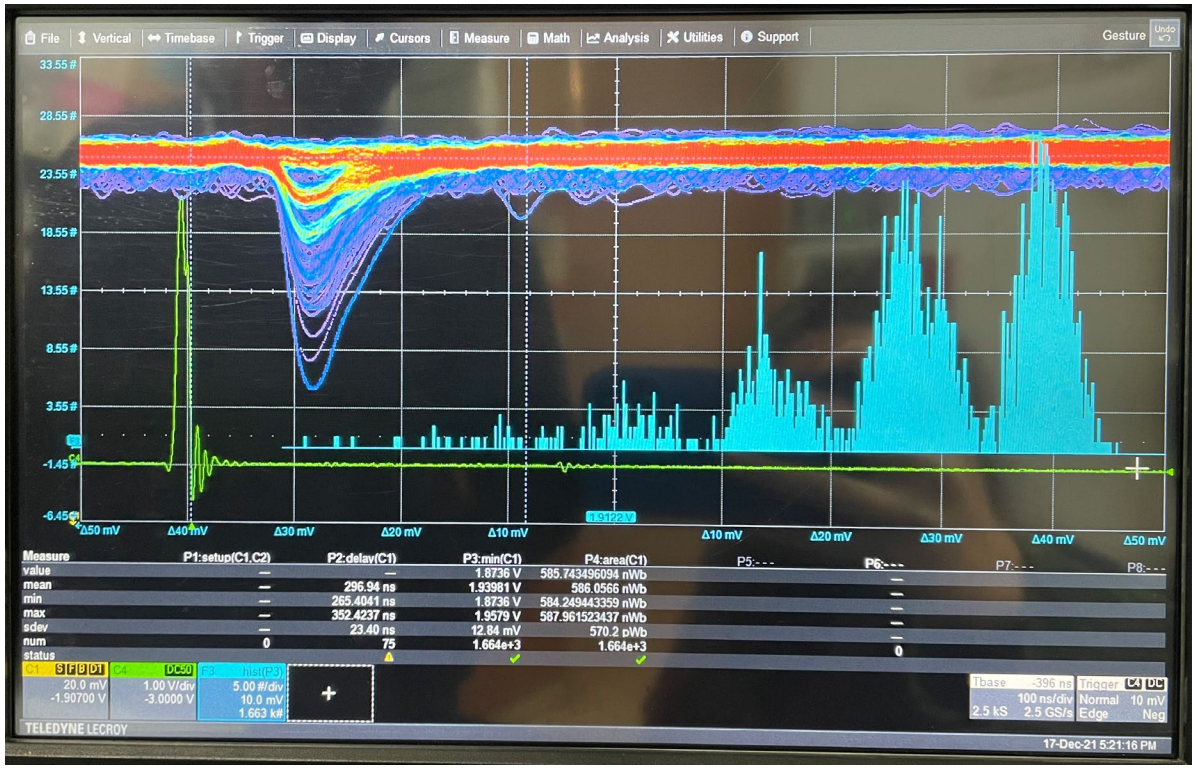
- 32 channel front-end IC
  - Fast trigger line for timing measurements
    - Preamplifier + fast discriminator
    - Time to amplitude converter (res. 37 ps)
  - Charge measurement line
    - Variable time shaper (25 ns to 100 ns)
    - Programmable Sample&Hold
    - 10 bit Wilkinson ADC



Digital section:

- 32 trigger outputs
- 12 μs conversion time + acquisition

PETIROC_FEB experimental measurements



Single strip of SiPM array output, charge path output

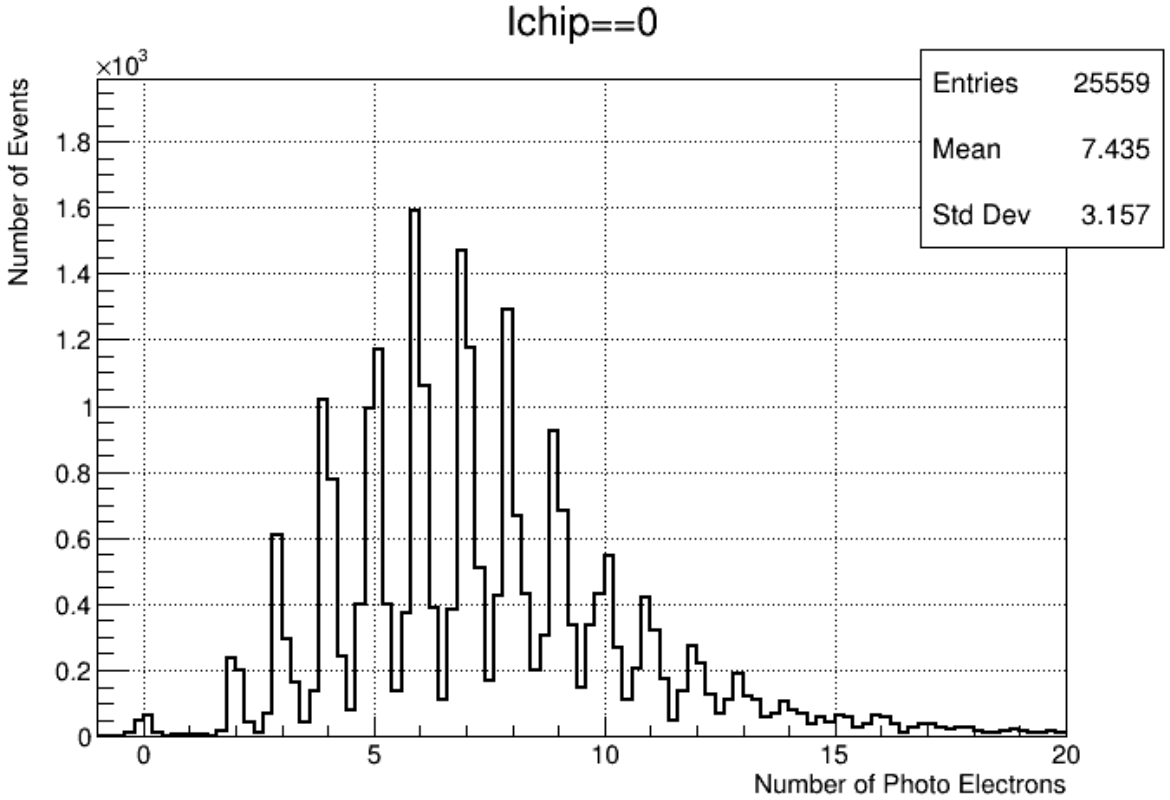
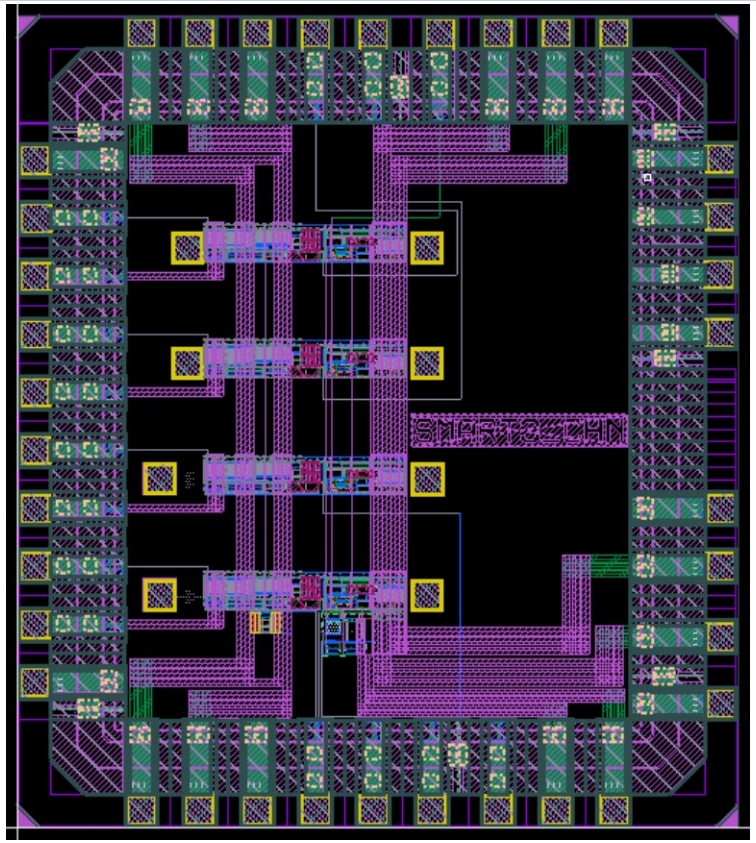


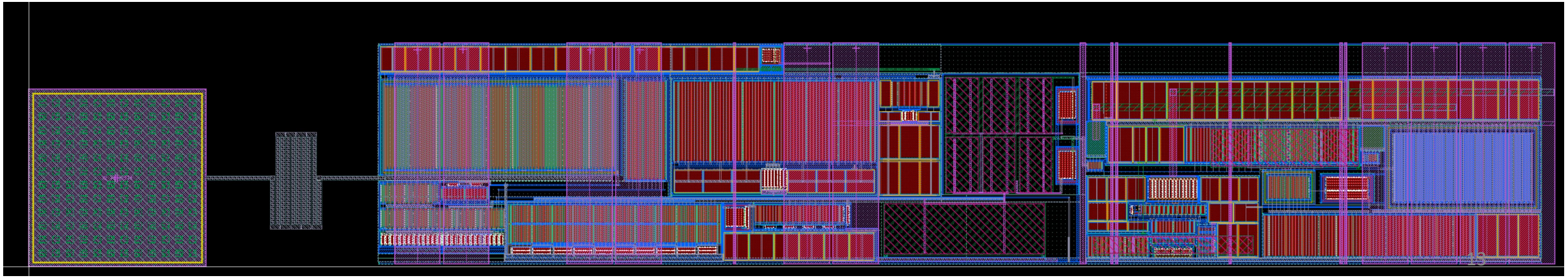
Photo-electron distribution, strip of SiPM array read by the PETIROC_FEB using an external trigger

For applications and more measurements: **talk by R. Pillera**

Future perspective

- New channel architecture developed
- First prototypes produced in LF110 nm
- First characterization tests in March 2022





Thanks