CYGNO Photomultiplier DAQ development

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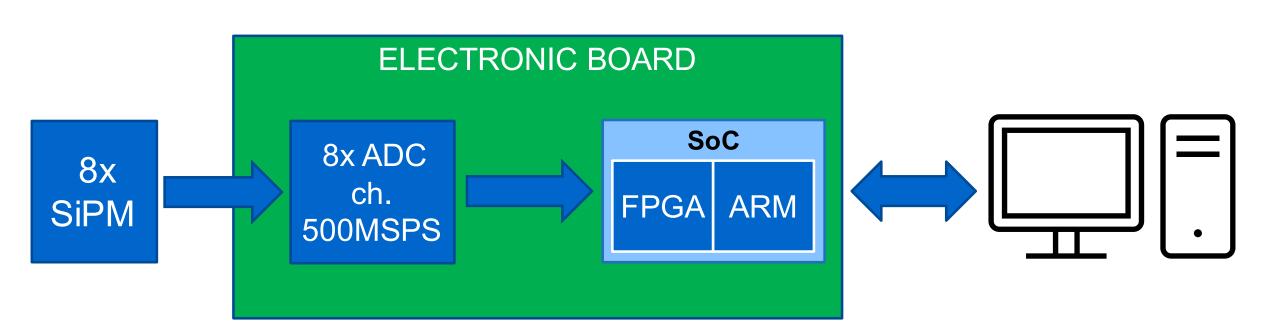




- The basic features of the DAQ Module;
- Brief presentation of the initial scope for the electronic board and what we have changed;
- The new and current project;
- Development kit;
- Embedded Linux and the other needs for using the ARM processor;
- Computer visualization of the acquired data;
- Current DAQ Module development overview.

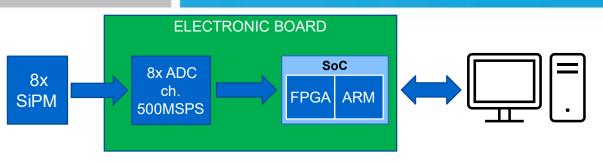
DAQ Module overview

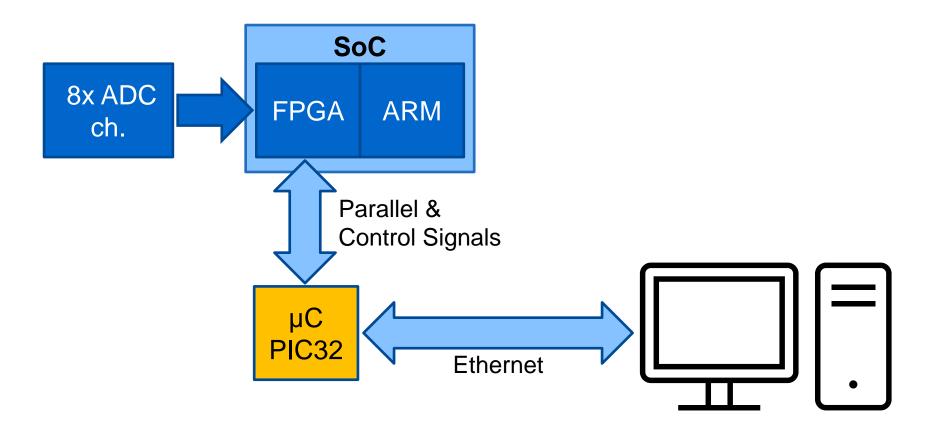






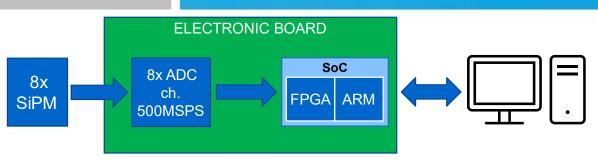
First Scope







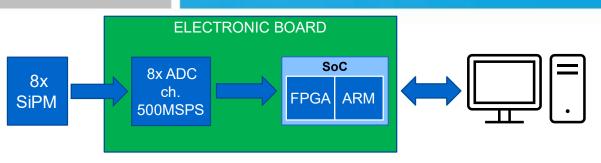
Current design

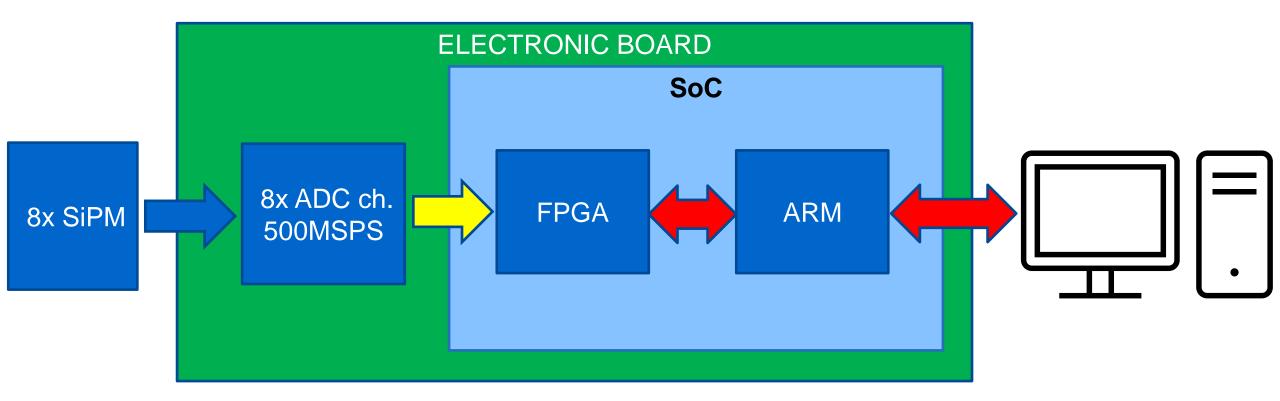






Current design

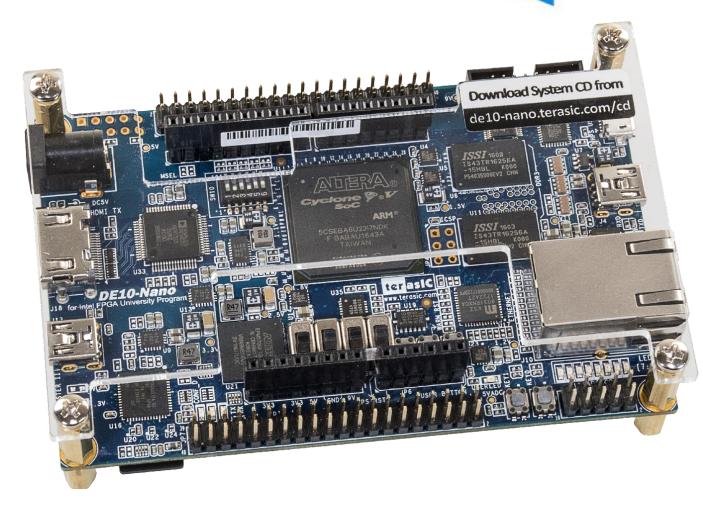






Development Kit: DE10-Nano from Terasic

- Based on the Cyclone V SoC, which pairs a Cyclone V FPGA with a dual-core ARM® Cortex®-A9 processor.
- The hard processor system includes a full set of peripherals and interfaces. It is equipped with 1 GB of DDR3, a microSD card socket, an ADC, gigabit ethernet, USB-Blaster II onboard for programming; JTAG Mode, USB OTG, UART to USB, and more.





Software Tools

- Use of embedded Linux distribuition, called RSYocto*, from Yocto Project;
- Django Project for rapid web development;
- Visual Studio Code Insiders;
- Quartus Prime Lite;
- Altium Designer;
- Programming Languages: Python and Verilog.



YOCTO • PROJECT www.yoctoproject.org



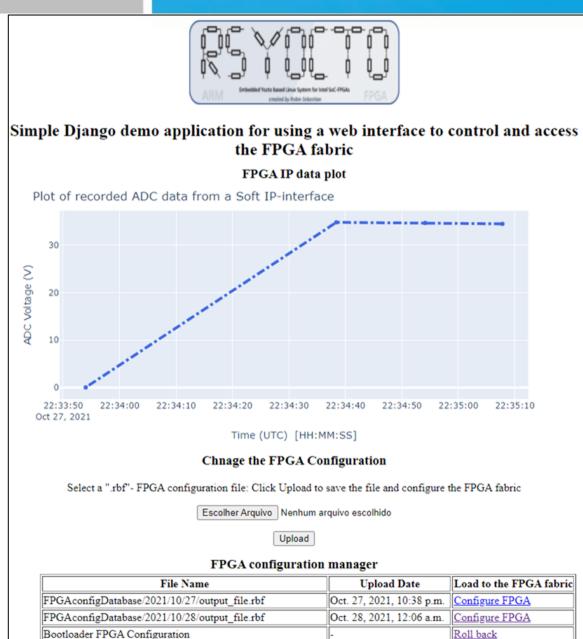
www.djangoproject.com



* https://github.com/robseb/Django2FPGAdemo



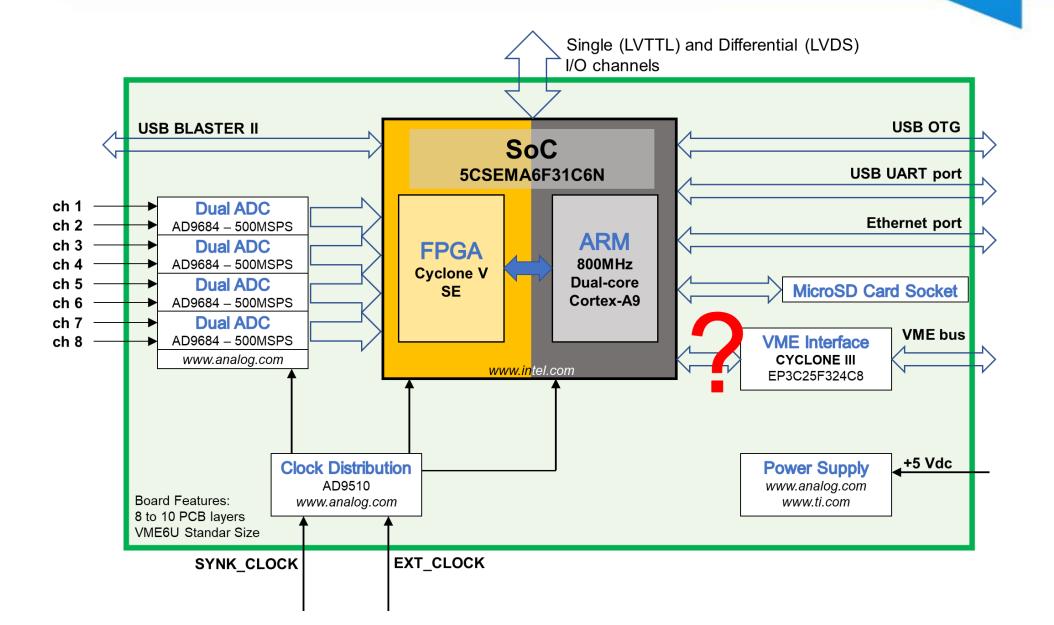
Software Tools for the current development



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V EDITORES ABERTOS	🍨 adcTest.py
🔎 🍦 adcReadO	annel.p 30
🔶 🗙 🍨 adcTest.p	31 # The Lightweight HPS-to-FPGA Bus base address offset
	0] 32 HPS_LW_ADRS_OFFSET = 0xFF200000 33
^o [™] > _pycache_	33 34 # LTC2308 Address offset
> .cache	35 ADC_ADDRES_OFFSET = 0x40
7.5511	36
> .vscode-server	
	mo 38 ###### Register Set of the Intel University program Analog Devices LTC2308 Soft-IP 39 #
≣ .bash_history	40
.wget-hsts	41 # ADC data register no for channel (read only)
ಿ adcTest.py	42 ADC_REG_OFF_DATACH = ADC_CH*4
🔮 blinkingFPGAle	
blinkLed.py	44 # ADC Control register no (write only)
≣ blinky_nano.rb	45 ADC_REG_OFF_UPDATE = 0 # Update the converted values 46 ADC_REG_OFF_AUTO_UPDATE = 4 # Enables or disables auto-updating
🔮 devmem.py	47
fpgalnputDem	48 # The number of available number
fpgaLedCounte	49 ADC_KEG_KANGE= 28
≡ gpiConfNano.r ♦ gsensorDemo.j	50
 gsensorDemo.j serialEchoDem 	
SenalechoDen	
	54 # Read the name of the used development board
	55 #-> Only the Terasic DE10 Standard and Nano Boards are allowed!
	56 # The Board name for the image is located here: "/usr/rsyocto/suppBoard.txt"
	57 if os.path.isfile("/usr/rsyocto/suppBoard.txt"): 58 supportStr = ""
	59 with open("/usr/rsyocto/suppBoard.txt", "r") as f:
	60 supportStr = f.read()
	61 if not supportStr.find('Terasic HAN Pilot') ==-1 :
	62 print('The Terasic HAN Pilot Board has no LTC2308 and is not supported!')
	63 sys.exit() 64
	65 # The ADC is only supported with rsyocto Version 1.04 or later
	PROBLEMAS SAÍDA TERMINAL PORTAS CONSOLE DE DEPURAÇÃO 🛛 🕥 sh 🕂 🗸 🛄 💼 ^ X
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× SSH: rsYocto 🐉 master* ↔ ⊗ 0 Δ 0 👷 0 Ln 48, Col 1 Espaços: 4 UTF-8 LF Python 🖗 🗘	



DAQ Module overview







- Survey and selection of technologies/devices: ADC, FPGA, μC. DONE
- Drawing electrical schematics: analog input circuit, ADC connections, microcontroller circuit.
 DONE
- Survey of other FPGA due to software licence issue (Quartus Prime). New FPGA family selected: Cyclone V. DONE
- Second ADC option selected due to transceiver speed limitation in Cyclone V. DONE
- Drawing electrical schematics: FPGA circuit. **DOING**
- Defining and drawing ADC to FPGA data buses (16 x 4 LVDS channels). DONE
- Learning how to use the ARM processor in the FPGA to implement the Ethernet and USB interfaces. DOING

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