

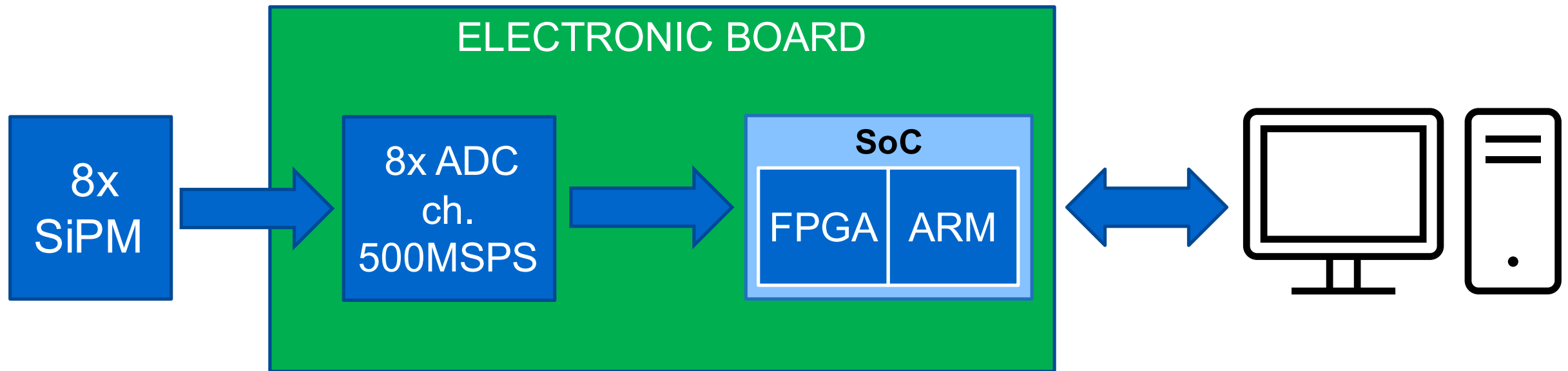
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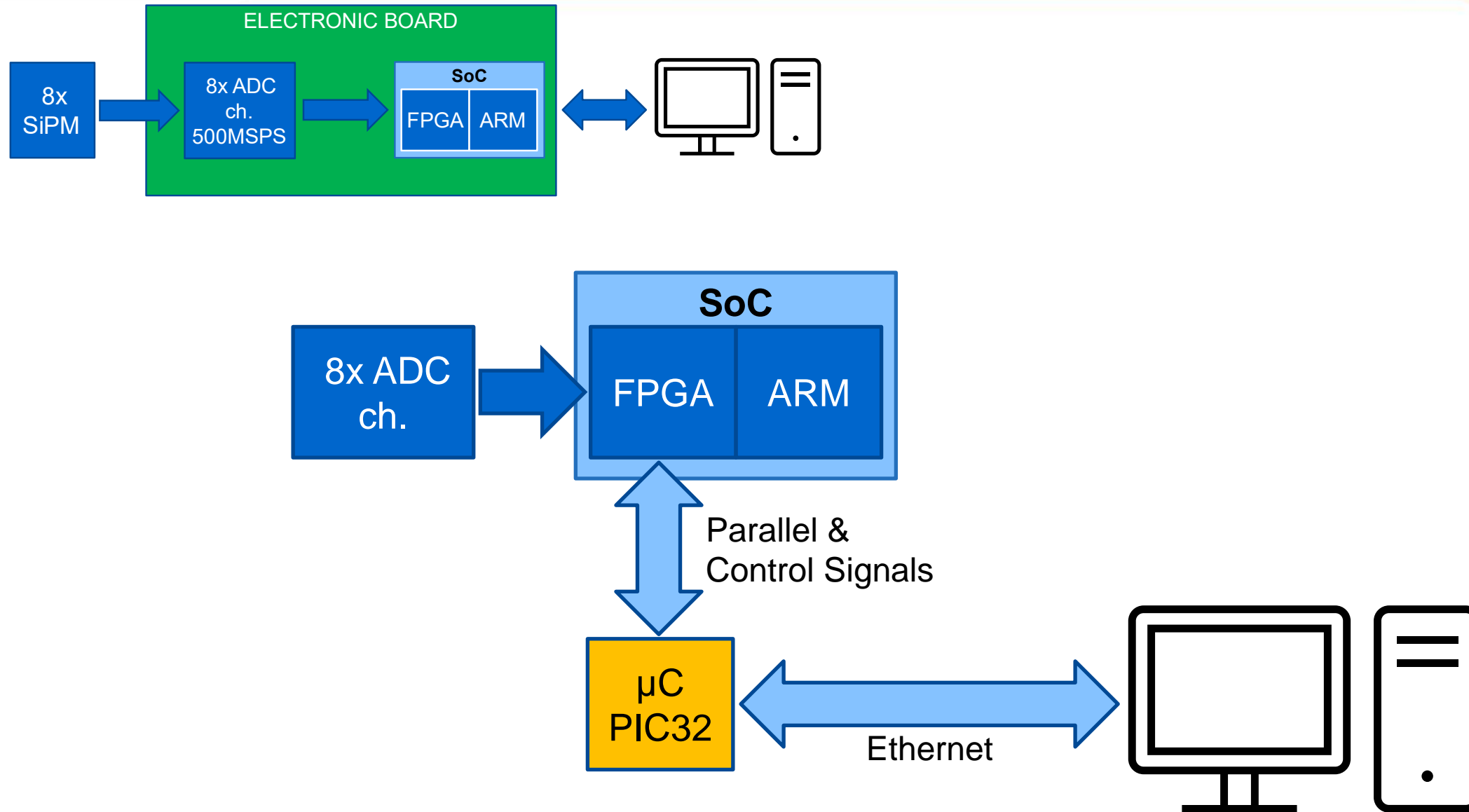
Photomultiplier DAQ development

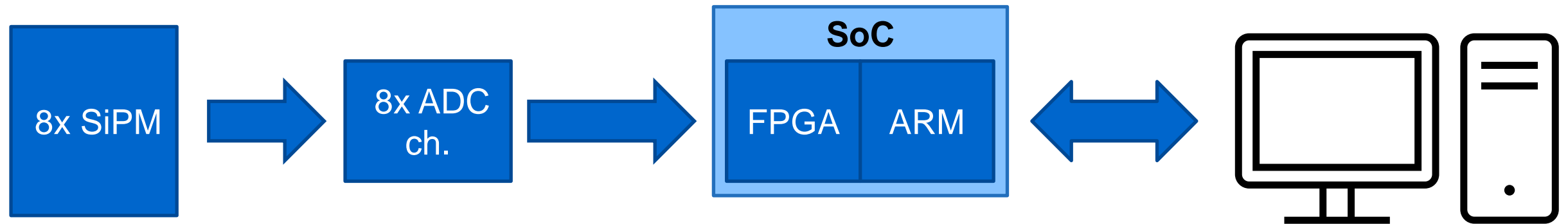
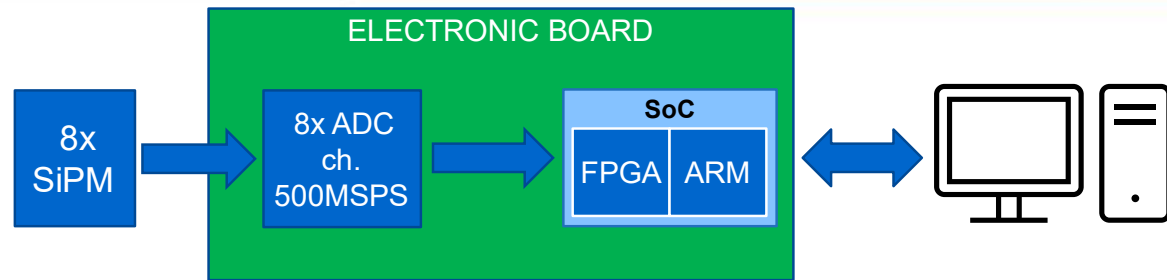
Herman Pessoa Lima Jr
Danilo dos Santos Cardoso

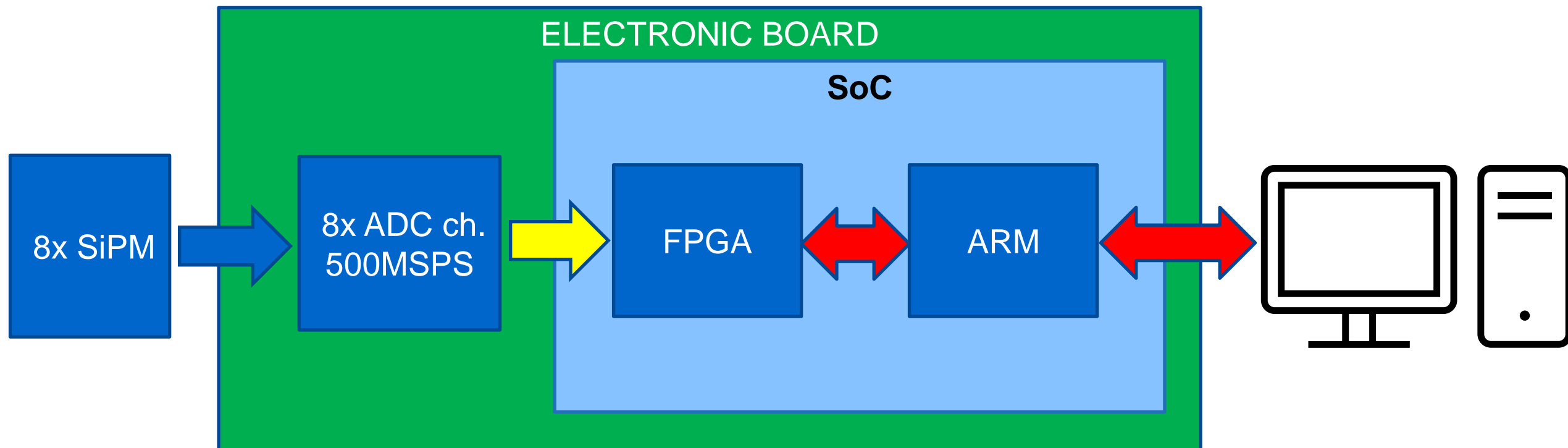
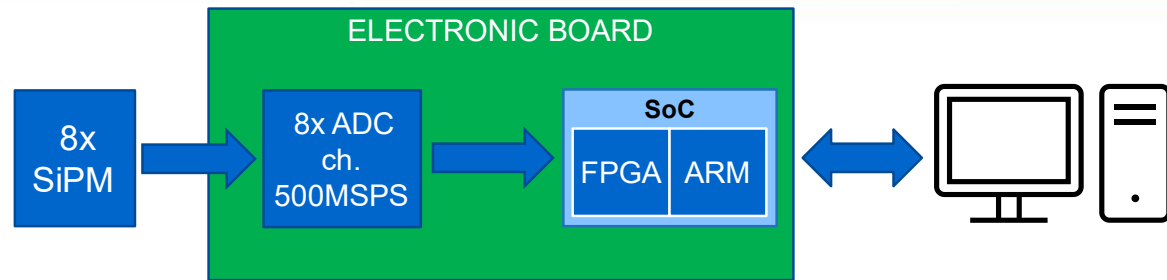
Dec 15, 2021

- ❑ The basic features of the DAQ Module;
- ❑ Brief presentation of the initial scope for the electronic board and what we have changed;
- ❑ The new and current project;
- ❑ Development kit;
- ❑ Embedded Linux and the other needs for using the ARM processor;
- ❑ Computer visualization of the acquired data;
- ❑ Current DAQ Module development overview.



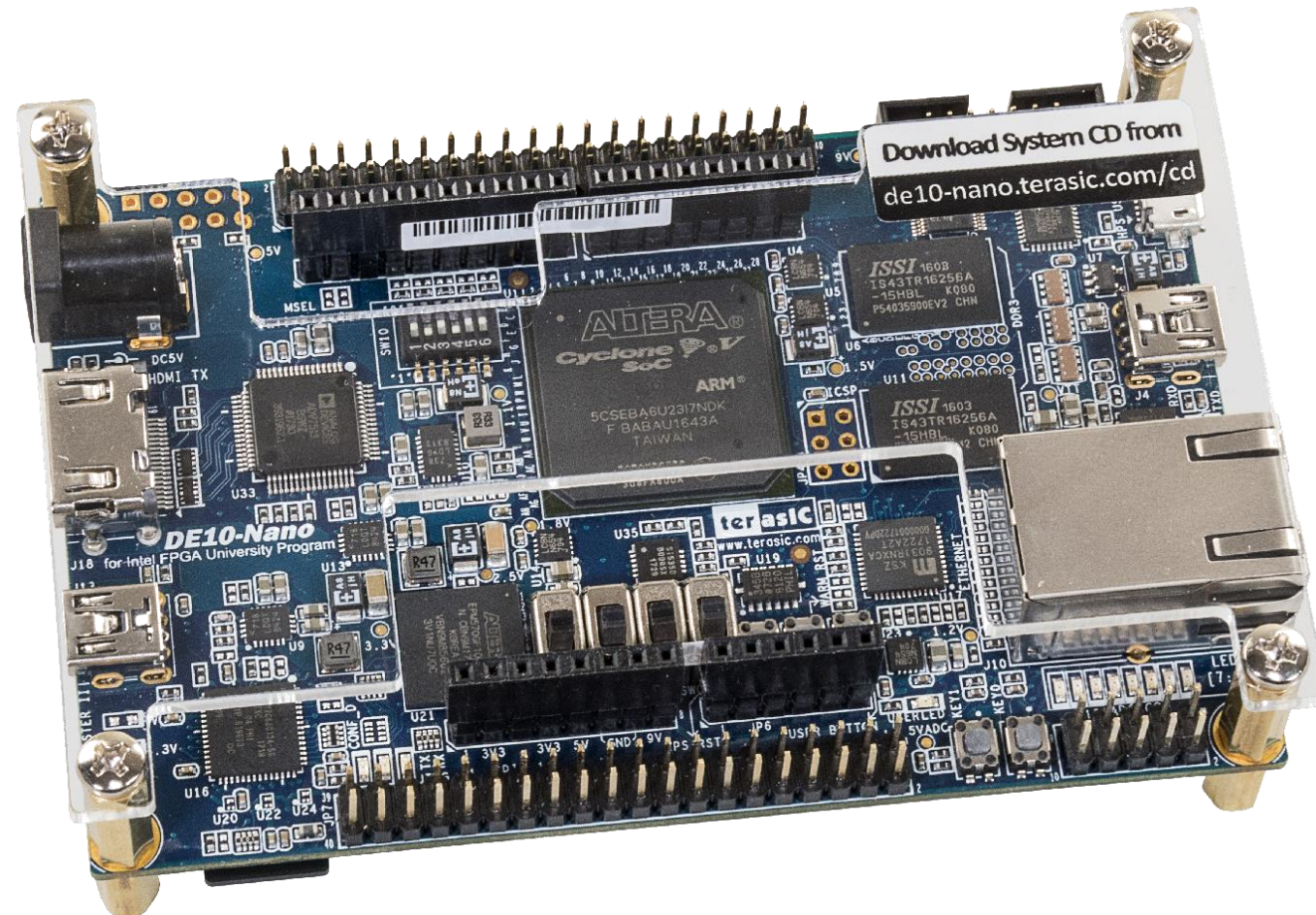






Development Kit: DE10-Nano from Terasic

- Based on the Cyclone V SoC, which pairs a Cyclone V FPGA with a dual-core ARM® Cortex®-A9 processor.
- The hard processor system includes a full set of peripherals and interfaces. It is equipped with 1 GB of DDR3, a microSD card socket, an ADC, gigabit ethernet, USB-Blaster II onboard for programming; JTAG Mode, USB OTG, UART to USB, and more.



- Use of embedded Linux distribution, called RSYocto*, from Yocto Project;
- Django Project for rapid web development;
- Visual Studio Code Insiders;
- Quartus Prime Lite;
- Altium Designer;
- Programming Languages: Python and Verilog.



Quartus
Prime

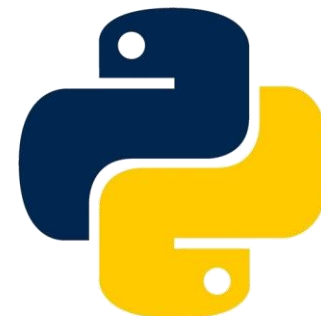
www.intel.com.br

yocto .
PROJECT
www.yoctoproject.org

Altium
Designer®

www.altium.com

django
www.djangoproject.com



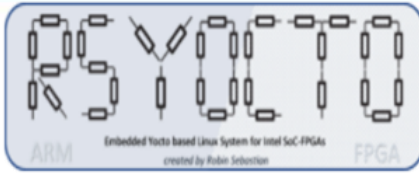
www.python.org



code.visualstudio.com/insiders

* <https://github.com/robseb/Django2FPGAdemo>

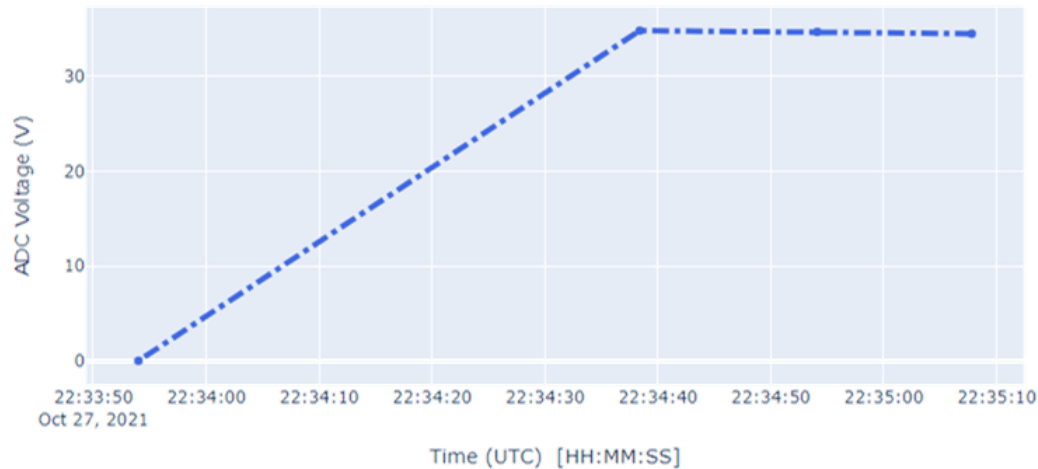
Software Tools for the current development



Simple Django demo application for using a web interface to control and access the FPGA fabric

FPGA IP data plot

Plot of recorded ADC data from a Soft IP-interface



Change the FPGA Configuration

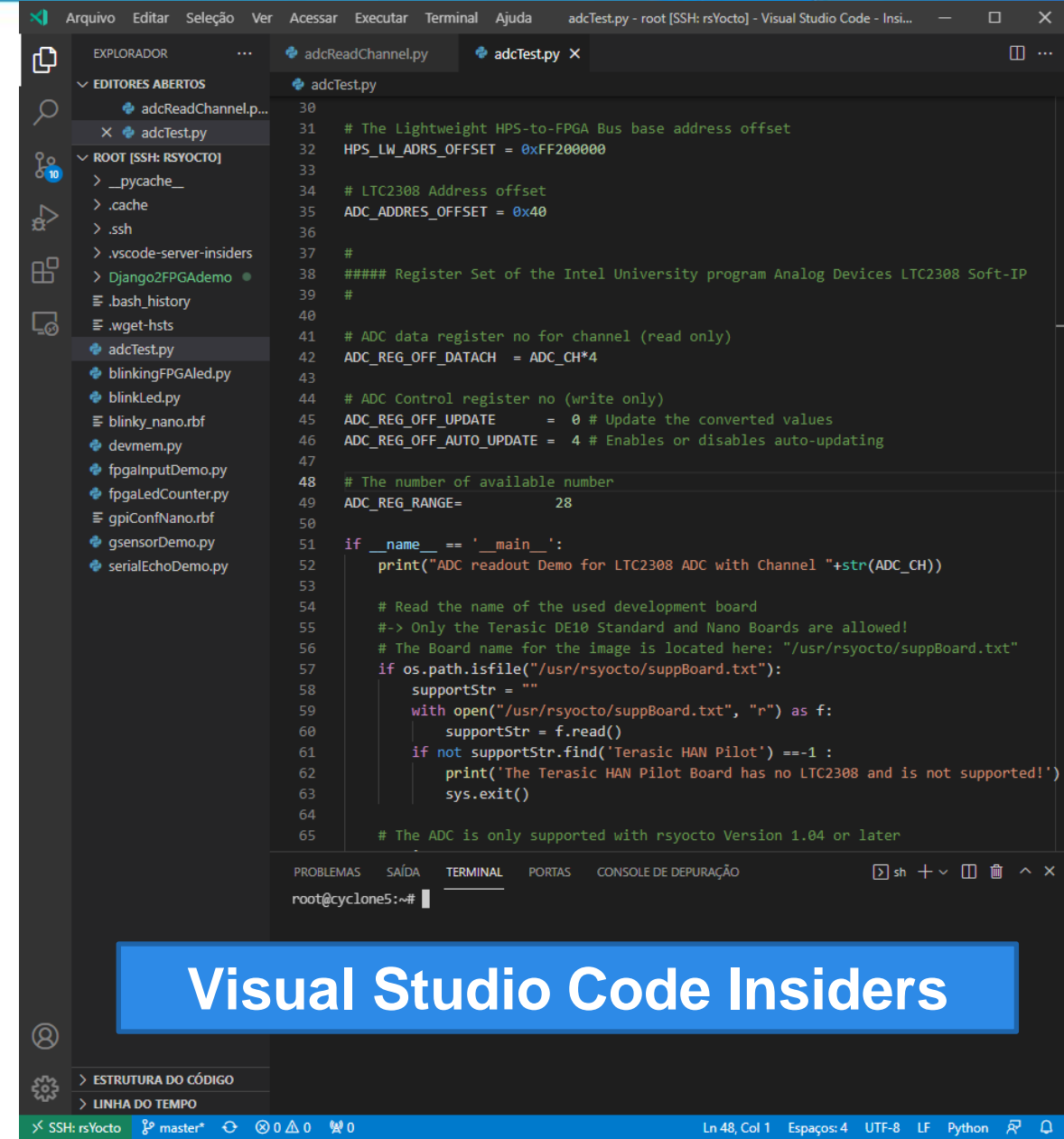
Select a ".rbf"- FPGA configuration file: Click Upload to save the file and configure the FPGA fabric

Escolher Arquivo Nenhum arquivo escolhido

Upload

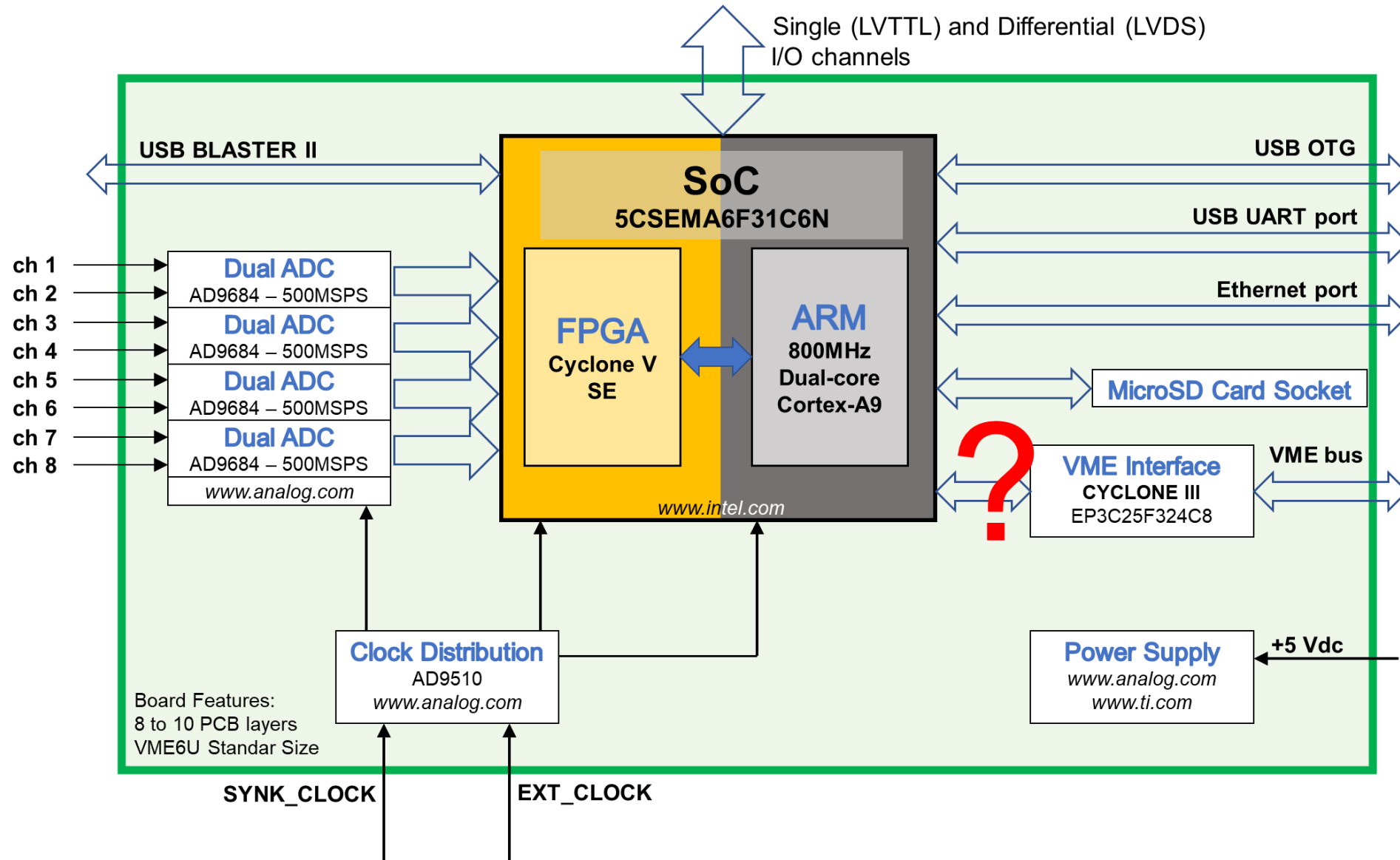
FPGA configuration manager

File Name	Upload Date	Load to the FPGA fabric
FPGAconfigDatabase/2021/10/27/output_file.rbf	Oct. 27, 2021, 10:38 p.m.	Configure FPGA
FPGAconfigDatabase/2021/10/28/output_file.rbf	Oct. 28, 2021, 12:06 a.m.	Configure FPGA
Bootloader FPGA Configuration	-	Roll back



The screenshot shows the Visual Studio Code Insiders interface. The Explorer sidebar on the left lists files in the 'ROOT [SSH: rsyocto]' directory, including 'adcTest.py'. The main editor area displays the code in 'adcTest.py', which is a Python script for interfacing with an ADC. The code includes comments for register offsets and control registers, and a main function that reads the board name from a file and prints the ADC readout. The terminal window at the bottom shows the command prompt 'root@cyclone5:~#'.

Visual Studio Code Insiders



- ❑ Survey and selection of technologies/devices: ADC, FPGA, μ C. **DONE**
- ❑ Drawing electrical schematics: analog input circuit, ADC connections, microcontroller circuit. **DONE**
- ❑ Survey of other FPGA due to software licence issue (Quartus Prime). New FPGA family selected: **Cyclone V**. **DONE**
- ❑ Second ADC option selected due to transceiver speed limitation in Cyclone V. **DONE**
- ❑ Drawing electrical schematics: FPGA circuit. **DOING**
- ❑ Defining and drawing ADC to FPGA data buses (16 x 4 LVDS channels). **DONE**
- ❑ Learning how to use the ARM processor in the FPGA to implement the Ethernet and USB interfaces. **DOING**

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