Report on Updates in GTK Read Out Firmware

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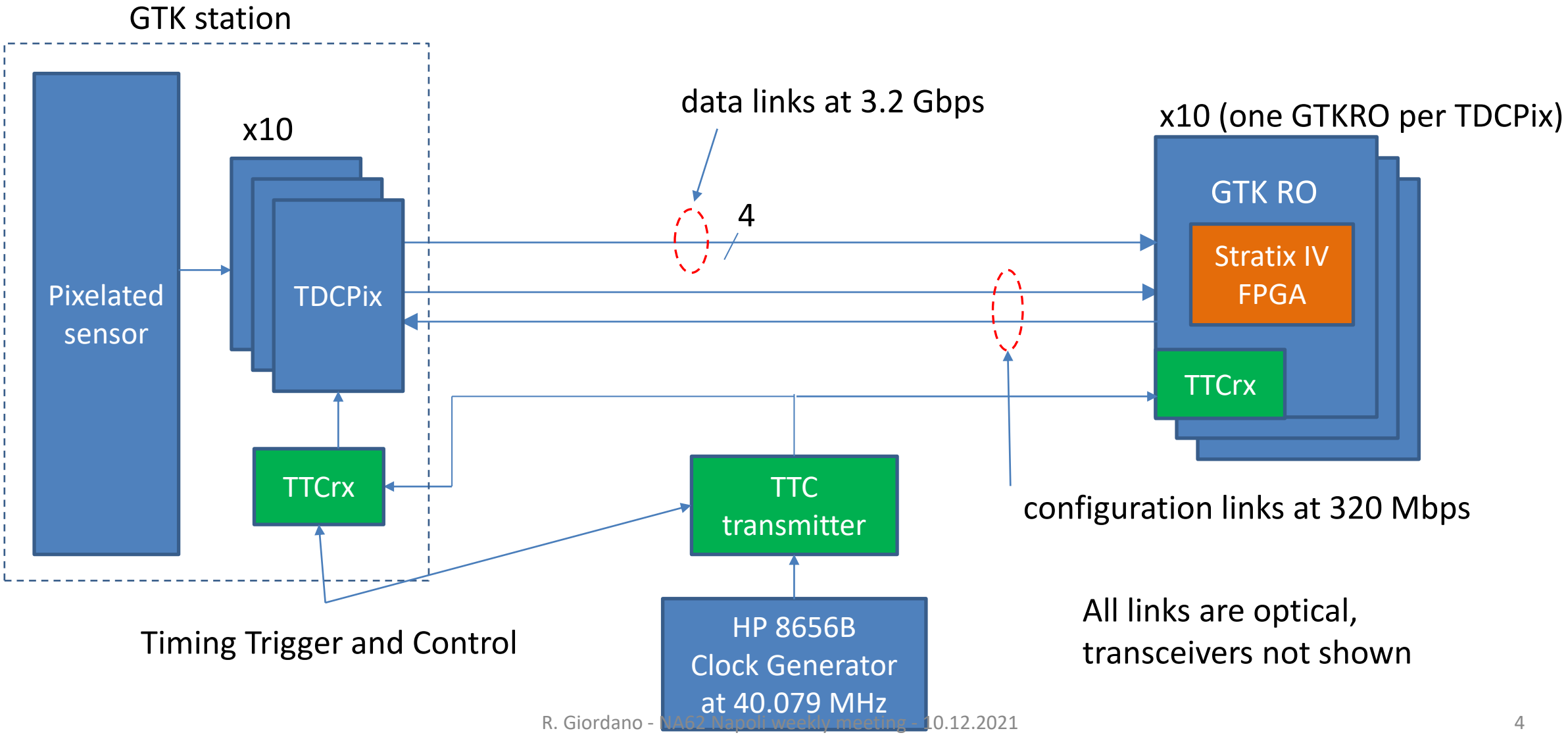
Activity at CERN

- At CERN from Nov. 23 to 28 with A. Cotta Ramusino (INFN FE)
- Welcoming and friendly environment
- Briefing on present firmware organization
  - TDCPix readout and configuration
- GTK-RO is based on Altera Stratix IV
- Firmware is designed by means of Quartus 13.1
  - stuck to this very old version due to IP and licensing issues

Configuration Issues

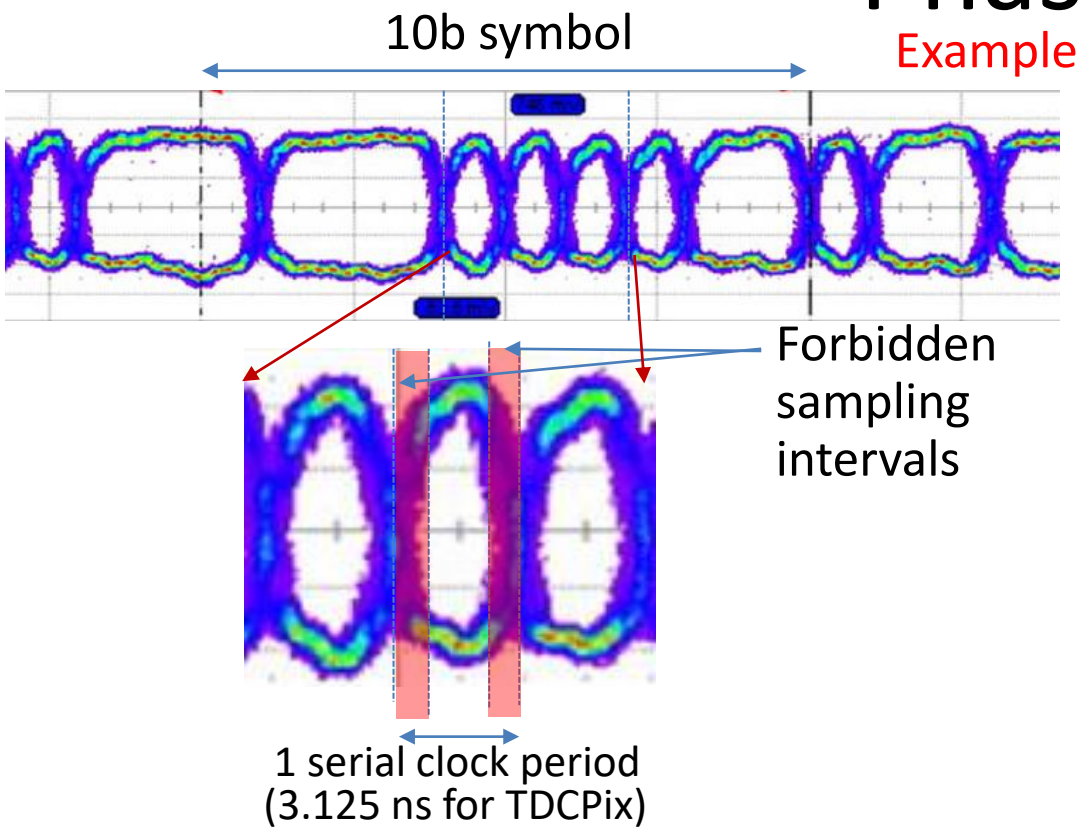
- One of the problems reported during NA62 operation is the loss of lock on configuration links to/from TDCPix chips
- This causes loss of entire bursts => inefficiency
- Allegedly it is related to improper or marginal phases for serial communication from the chips (RX) and to the chips (TX)

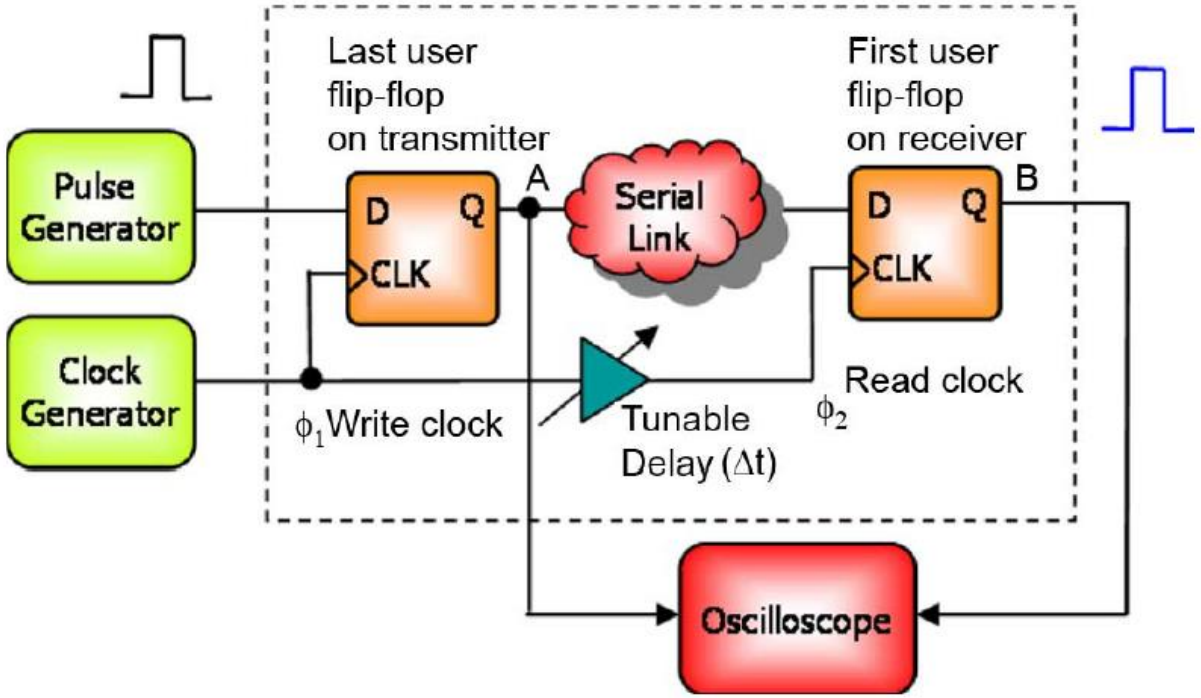
TDCPix Links: Simplified Block Diagram



Phase Issues

Example of 8b10b stream





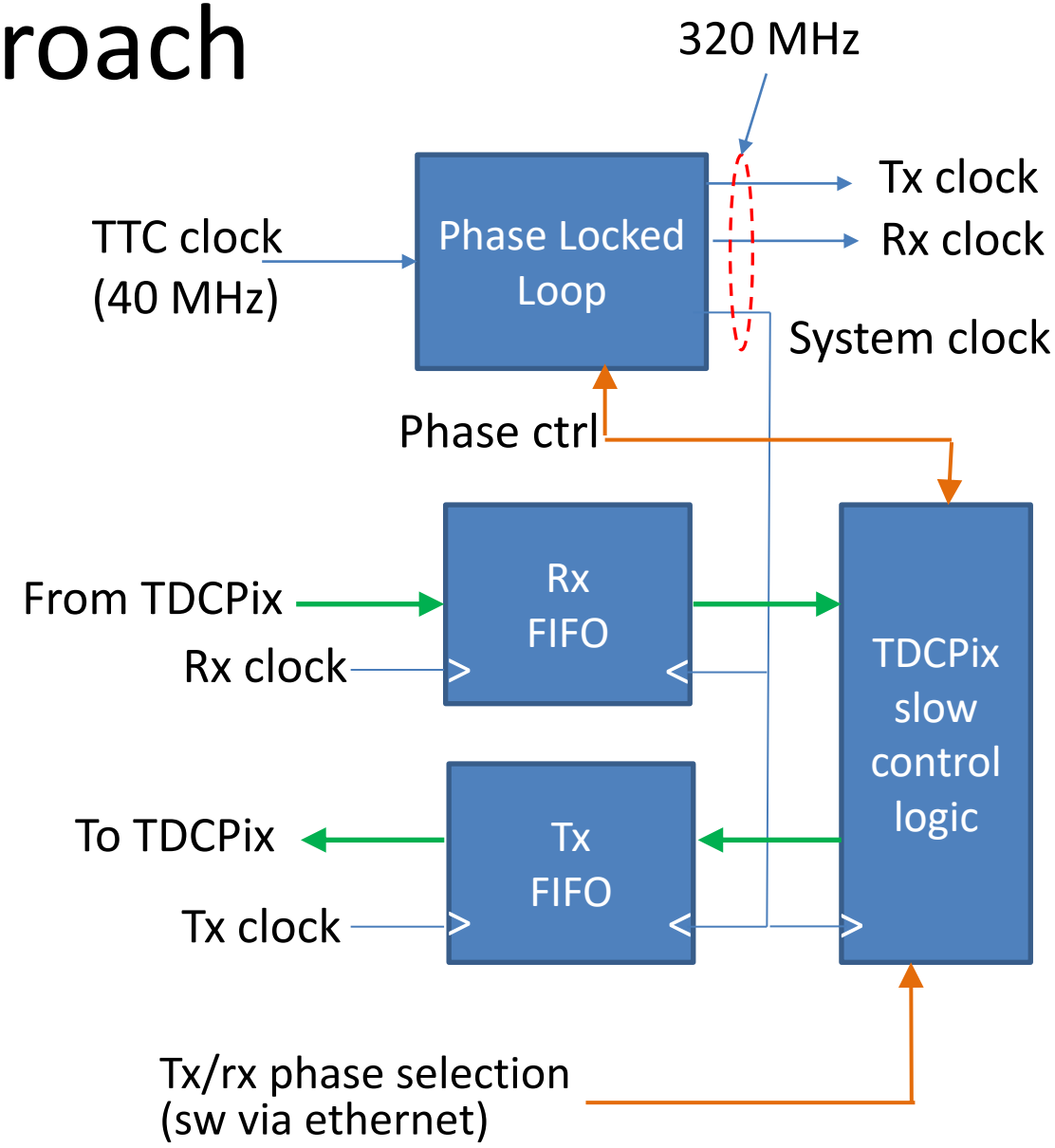
- Serial stream configuration links 8b10b encoded, received by GTK RO with an unpredictable phase
  - recovery of embedded clock is not possible, stream is routed to regular IO pins
- TDCPix expects data with a phase compatible with it is internal clock at 320 MHz (TTC 40MHz x 8)

Phase Issues (2)

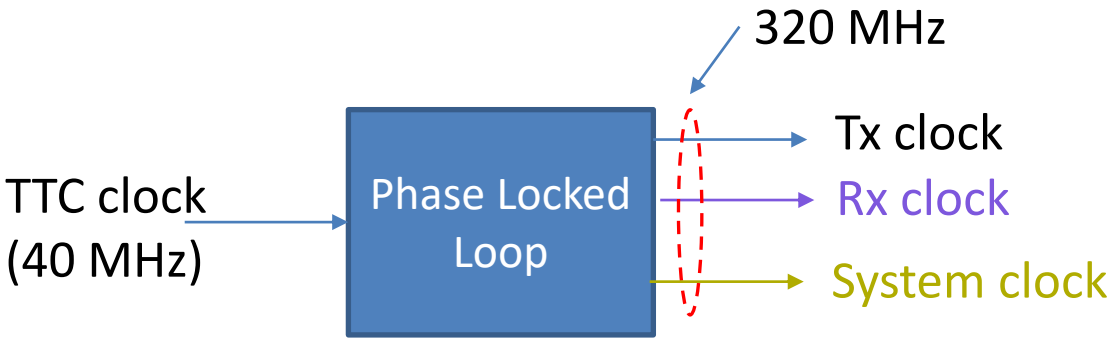
- Previously, the problem was addressed in GTK RO firmware by
  - Running the transmitter and receiver on a 320-MHz system clock derived by the TTC clock at 40 MHz (Phase Locked Loop in Stratix IV)
  - Shifting the system clock among 4 possible equally-spaced phases (781ps) to transmit to the TDCPix
  - Sampling the data from TDCPix on rising and falling edges of the system clock and choosing one of the two according to data integrity (equivalent to two opposite phases)
- Limitations
  - System was modifying its own clock phase, potential timing violations
  - Modifying transmission phase impacted also reception phase

New Approach

- Decouple transmission and reception clocks
  - System clock, transmission clock and reception clocks (all at 320 MHz)
- finer-grade phasing, 24 possible independent phases for Tx and Rx clocks
- tiny FIFO buffers (8 words depth) to cross clock domains from system to transmission/reception

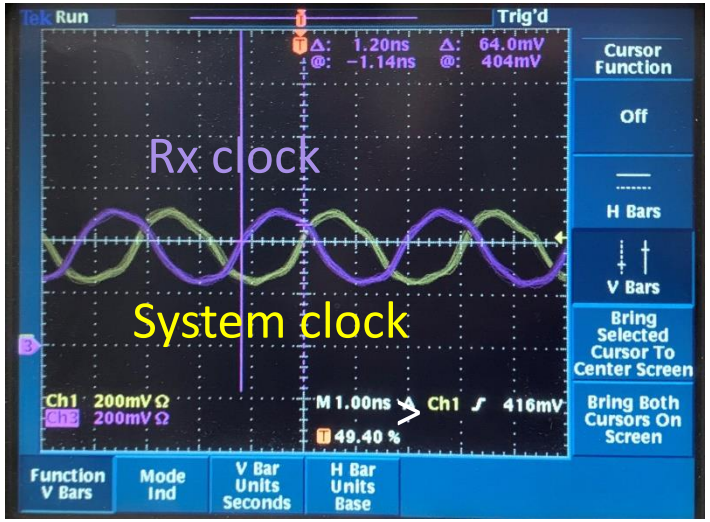


Hardware Verification of Phase Shift

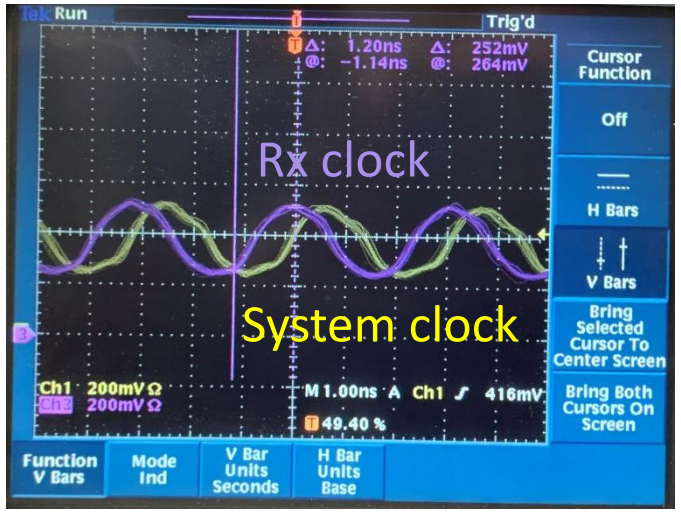


- Phase shift logic has been verified in hardware on a GTK-RO board in the PC farm room
- Board equipped with coax cables and SMA connectors
- Available scope (Tektronix TDS 3054C) limited at 500 MHz bandwidth

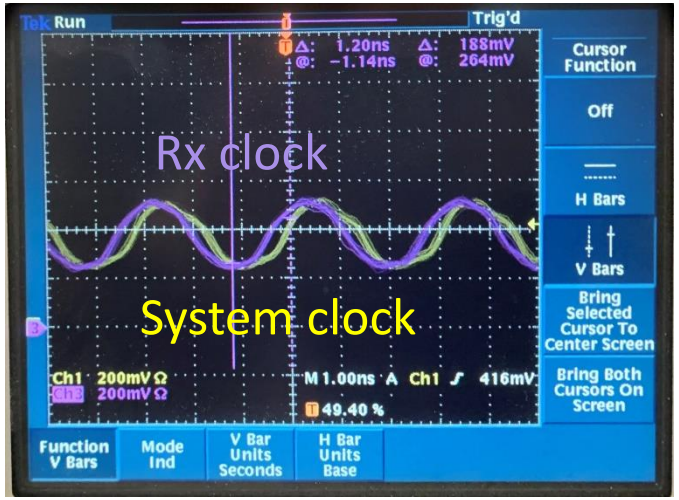
Phase 0



Phase 2 (+260ps)



Phase 4 (+520ps)



Configuration Link Lock Tests

- A. Cotta Ramusino has implemented phase control in software and he is running tests since November 29
- In each test
  - reset the TDCPix forcing it to a initial state in which it sends a predictable serial stream (K28.1)
  - scan the possible 24 rx phases and flag those which allow to lock on comma characters embedded in K28.1 symbols
  - For each suitable rx phase, scan the 24 possible tx phases
- System is working, but some issues remain
  - Isolated good (bad) phases breaking a sequence of bad (good) ones
  - Good rx phases seem to be fewer than expected
  - Could be related to signal integrity or logic issues in the lock logic

Test by A. Cotta Ramusino

RX phase	Result(1)	Result(2)
0	ok	
1	ok	
2	ok	
3	ok	
4	ok	
5	ok	
6	ok	
7	bad	
8	bad	
9	bad	
10	bad	
11	bad	
12	bad	
13	bad	bad
14	ok	ok
15	bad	bad
16	ok	
17	ok	
18	ok	
19	ok	
20	ok	
21	ok	
23	bad	

Configuration Link Lock Tests (2)

- Tx and Rx phase scan
  - 0 no rx lock
  - 1 rx only
  - 2 rx & tx
- PLL lock in TDCPix is not checked yet

Test by A. Cotta Ramusino

```
RXPhase_test_index: 0: [ 2 2 2 2 2 2 2 2 2 2 2 1 2 1 2 2 2 2 2 2 2 2 2 2 2 2 ]
RXPhase_test_index: 1: [ 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 ]
RXPhase_test_index: 2: [ 2 2 2 2 2 2 2 2 2 2 2 2 2 1 2 1 2 2 2 2 2 2 2 2 2 2 ]
RXPhase_test_index: 3: [ 2 2 2 2 2 2 2 2 2 2 2 2 2 2 1 2 2 2 2 2 2 2 2 2 2 2 ]
RXPhase_test_index: 4: [ 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 1 2 1 2 2 2 2 2 2 2 2 ]
RXPhase_test_index: 5: [ 2 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 1 2 2 2 2 2 2 2 2 2 ]
RXPhase_test_index: 6: [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
RXPhase_test_index: 7: [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
RXPhase_test_index: 8: [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
RXPhase_test_index: 9: [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
RXPhase_test_index: 10: [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
RXPhase_test_index: 11: [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
RXPhase_test_index: 12: [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
RXPhase_test_index: 13: [ 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 1 ]
RXPhase_test_index: 14: [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
RXPhase_test_index: 15: [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
RXPhase_test_index: 16: [ 2 2 2 2 2 2 2 2 2 2 2 1 2 1 2 2 2 2 2 2 2 2 2 2 2 2 ]
RXPhase_test_index: 17: [ 2 2 2 2 2 2 2 2 2 2 2 2 1 2 2 2 2 2 2 2 2 2 2 2 2 2 ]
RXPhase_test_index: 18: [ 2 2 2 2 2 2 2 2 2 2 2 2 2 1 2 2 2 2 2 2 2 2 2 2 2 2 ]
RXPhase_test_index: 19: [ 2 2 2 2 2 2 2 2 2 2 2 2 2 2 1 2 1 2 2 2 2 2 2 2 2 2 ]
RXPhase_test_index: 20: [ 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 1 2 2 2 2 2 2 2 2 2 2 ]
RXPhase_test_index: 21: [ 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 1 2 2 2 2 2 2 ]
RXPhase_test_index: 22: [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
RXPhase_test_index: 23: [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
Configuration links test finished, proceeding initialization
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Conclusions and Outlook

- Implemented finer grade phasing will make it possible to fix configuration link issues if they were related to marginal phase selection only
  - From NA62 operation it has been reported that an initially good phase can become a bad one
  - TDCPix reset and phase change? Radiation-induced? SEUs?
- Currently firmware development is bound to a Virtual Machine with the development system provided by Angelo
  - Need to coordinate firmware development efforts
  - use a version control system (git/hog)
  - get a license for Quartus/Modelsim at NA
- Constant contact with Angelo for link testing which is ongoing