

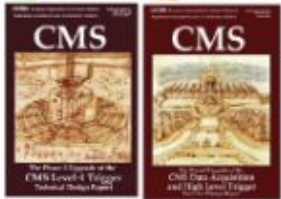


CMS PD

hardware activities

riunione Gr1
14.12.2021

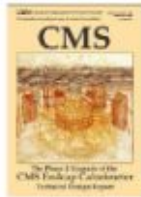
CMS Phase2



L1-Trigger HLT/DAQ

<https://cds.cern.ch/record/2714892>
<https://cds.cern.ch/record/2759072>

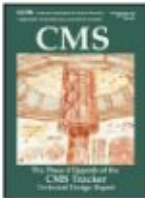
- Tracks in L1-Trigger at 40 MHz
- PFlow selection 750 kHz L1 output
- HLT output 7.5 kHz
- 40 MHz data scouting



Calorimeter Endcap

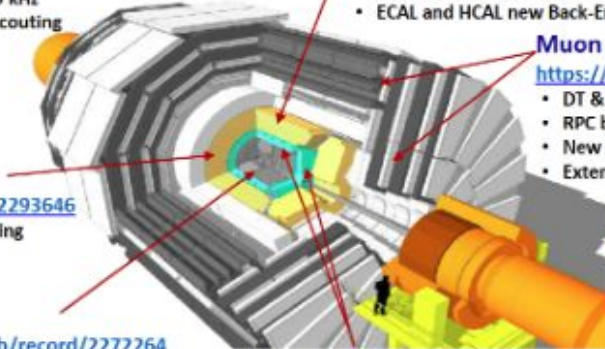
<https://cds.cern.ch/record/2293646>

- 3D showers and precise timing
- Si, Scint+SiPM in Pb/W-SS



Tracker <https://cds.cern.ch/record/2272264>

- Si-Strip and Pixels increased granularity
- Design for tracking in L1-Trigger
- Extended coverage to $\eta \approx 3.8$



Barrel Calorimeters

<https://cds.cern.ch/record/2283187>

- ECAL crystal granularity readout at 40 MHz with precise timing for e/ γ at 30 GeV
- ECAL and HCAL new Back-End boards

Muon systems

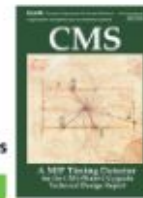
<https://cds.cern.ch/record/2283189>

- DT & CSC new FE/BE readout
- RPC back-end electronics
- New GEM/RPC $1.6 < \eta < 2.4$
- Extended coverage to $\eta \approx 3$

Beam Radiation Instr. and Luminosity

<http://cds.cern.ch/record/2759074>

- Bunch-by-bunch luminosity measurement: 1% offline, 2% online

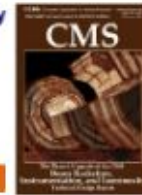


MIP Timing Detector

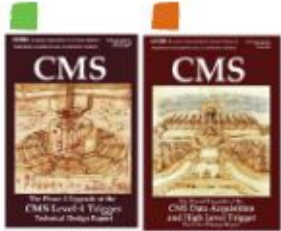
<https://cds.cern.ch/record/2667167>

Precision timing with:

- Barrel layer: Crystals + SiPMs
- Endcap layer: Low Gain Avalanche Diodes



CMS Phase2 : PADOVA

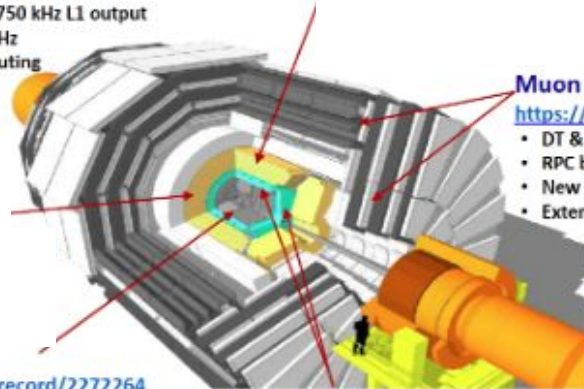


L1-Trigger HLT/DAQ

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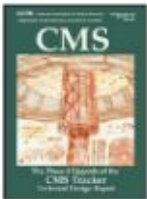
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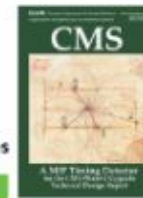
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MIP Timing Detector

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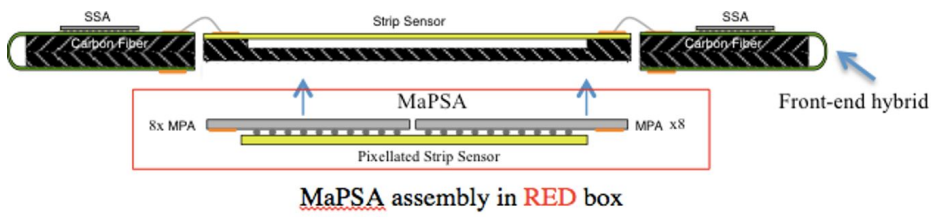
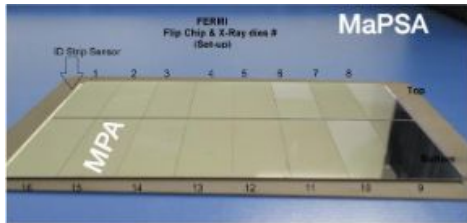
Precision timing with:

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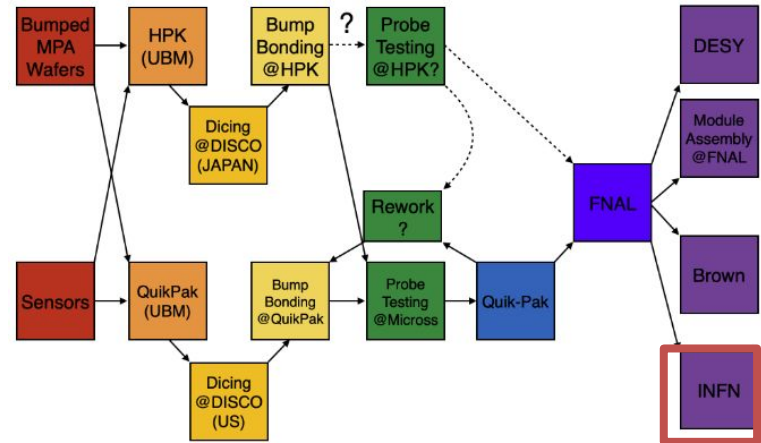
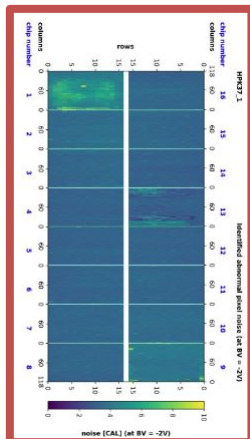
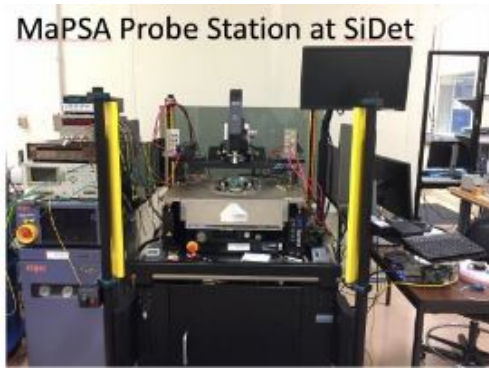


Tracker : MaPSA

- the MaPSA is the bump bonded assembly of the pixelated PS-p sensor and 16 MPAs (Macro Pixel ASICs)



- MaPSA probe testing (N. Bacchetta + D. Pantano) in camera pulita @PD
→ assegno di ricerca 2 anni (INFN)



DT : OBDT

@CERN DT slice test

One sector split and readout by phase-1 and phase-2 in parallel during LS2 / Run-3
(13 OBDT v1)



UXC split setup @CERN

In July, splitters were installed to bring signals from 2 FE cables of a DT chamber (YB+2 S1 MB4) to the racks on the balconies
Plan to use them to connect and test lpGBT OBDT (v2) prototypes before EYETS access

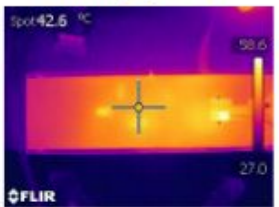


OBDT v2: 8 boards (pre production batch) tested in Padova



1. GBTx → lpGBT both for timing/slow control (lpGBT chip) and readout (lpGBT FPGA)
2. Safety subsystem is on-board **[TO]**
3. Clock distribution to logic different w.r.t. v1
4. SFP+/QSFP → VTRX+ (dual)

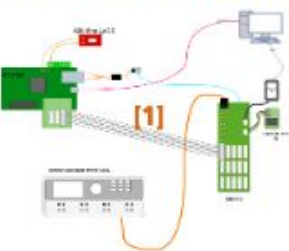
Thermal management (filler gap tests)



Liquid gap that turns solid after application and can be removed.

@SPE-PD

lpGBT clock & fast/slow controls



Basic functionalities:

1. lpGBT Tx/Rx (10gFEC5) link for lpGBT chip
2. lpGBT Rx (10gFEC5) for readout (test purpose)
3. Fast reset forwarded by the lpGBT - Elink0
4. "Emulated" F.E. pulses (16 channels) **[1]**

Irradiation @ TIFPA



Setup for OBDT v2 qualification prepared
TIFPA (TN) facility schedule still unstable, as of now beam time reserved in October

L1/DAQ : 40 MHz scouting

repliche a footprint ridotto ($\sim 0.5 \text{ m}^2$) delle DT @LAE in LNL

→ readout compatibile con Phase2 upgrade di CMS

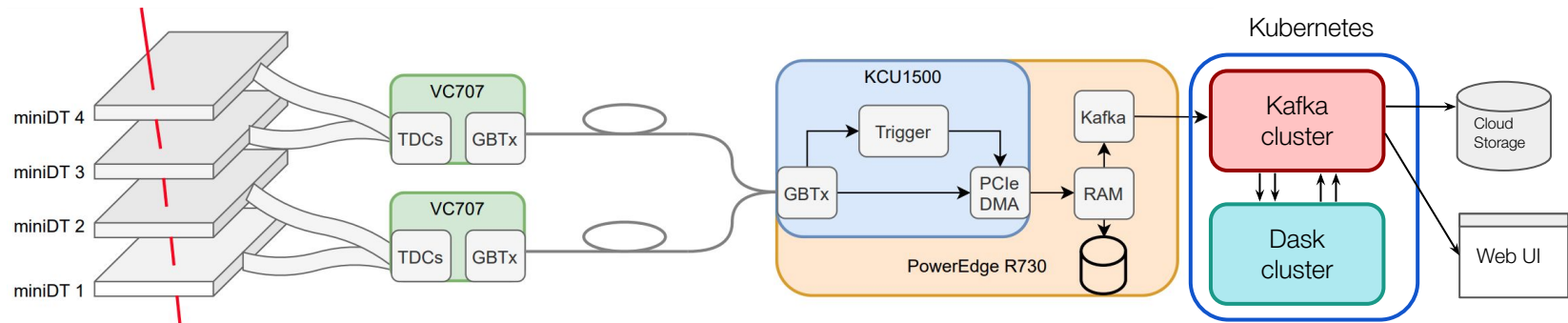
⇒ testbed per elettronica di Phase2 di CMS-DT (OBBDT)

→ sviluppo sistema DAQ "trigger-less" ed online processing

- readout di tutti gli hit prodotti dalle camere
- processing online usando risorse
 - *in-situ* : strumenti di calcolo distribuito (Apache Kafka, Apache Spark/Dask)
 - *off-site* : cloud (INFN Cloud e/o Cloud Veneto)
- sviluppo di architetture per il processing **scalabili** e facilmente **portabili** a molteplici use-cases [Kubernetes]

→ sviluppo di algoritmi di trigger basati su NN su FPGA

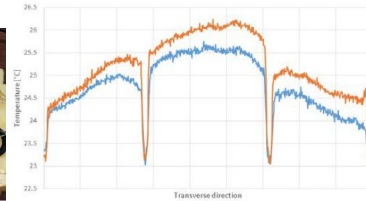
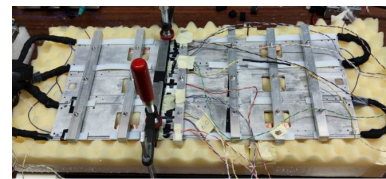
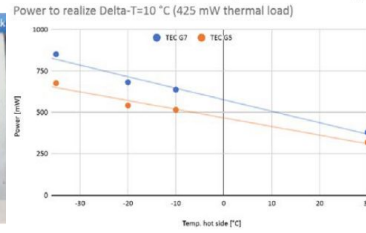
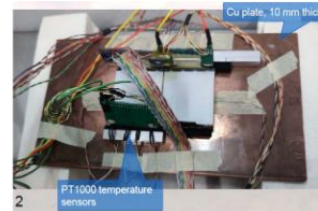
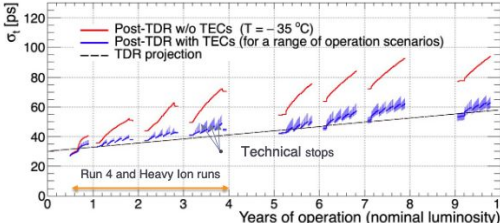
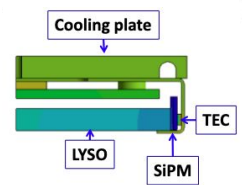
- ricostruzione veloce in FW di segmenti per il trigger locale delle DT ["alto" combinatorio]
 - tempi di inferenza della rete di $O(2)$ clock ($\rightarrow \sim 50 \text{ ns}$)
 - latenza fissa indipendentemente dalla complessità degli input
 - elasticità e portabilità potenzialmente vantaggiose anche per lo sviluppo di processing online per esperimenti locali e test beams



MTD : thermal tests timeline

Thermoelectric Coolers (TECs) integrated on SiPM array to further reduce the SiPM operating temperature [from -35°C to -45°C]

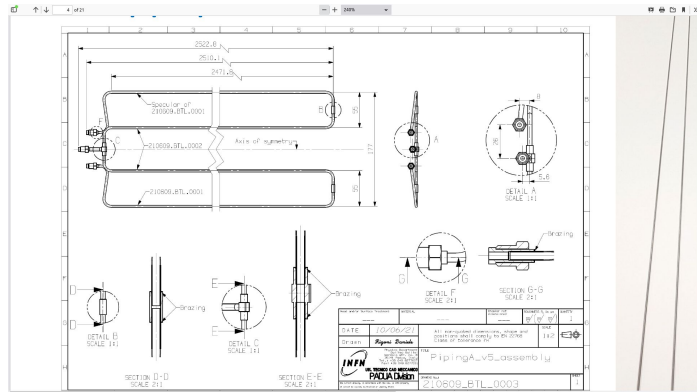
- test of the interface between TECS and copper housing
 - probably the most critical part of the interface
 - in progress in our Gr1 lab w/ different thermal coupling materials
 - need to converge in the first half of 2022
- test of the interface between CO2 cooling pipes and cold plates
 - test in our Gr1 lab w/ a cold plate and water cooling
 - detailed test of different grooves dimensions and thermal interfaces being performed in the heat transfer lab of the department of engineering in Vicenza
- test of a fully equipped readout unit (a cold plate w/ 12 readout modules) w/ glicole cooling at -35C in our specially equipped fridge in our Gr1 lab
 - system overhauled, expected in the first months of 2022
- other test planned in 2022
 - verify mechanical and thermal stability of thermal interfaces w/ radiation
 - verify mechanical stability of all interface w/ thermal cycles between -40C and +40C
 - plan to use the climate chamber in the electronics lab



needed for the SiPM annealing

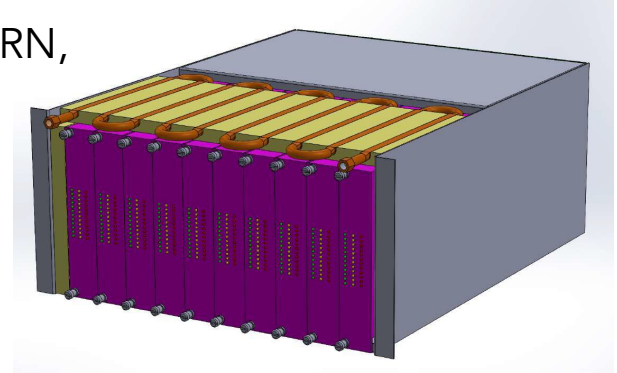
MTD : test of mechanics

- a full size “tray” designed by PD has been produced by a company in Italy and assembled at CERN
- cooling pipes manifold for the tray, also designed by PD, were electron-beam brazed at CERN and need to be tested at 150 bar for compliance with CO2 cooling
- full assembly will then be tested at CERN CMS TIF facility with dummy thermal loads
 - in the first months of 2022
 - to complement the test made in Padova of a fully equipped (not dummy) readout unit tested w/ liquid cooling



MTD : test TECs power supplies

- CMS is making a global tender for power supplies through CERN, for several sub-detectors upgrades
 - hostile environment (magnetic field, radiation)
- main version will be for MTD endcap (ETL) and barrel (BTL) LV, and for the endcap calorimeter (HGICAL)
- MTD will have two more versions, for the bias voltages and for the TECs
- Padova is expected to test the prototypes of the power supply for the TECs, coherently w/ the involvement on the TECs cooling interface
 - it is special as it needs to be able to invert the voltage, to use TECs as heater for the annealing
 - goal is to verify the compliance of the prototype w/ specs, not the functionality of the full production that will be tested by the company
 - expected to happen in the second part of 2022 in our Gr1 lab

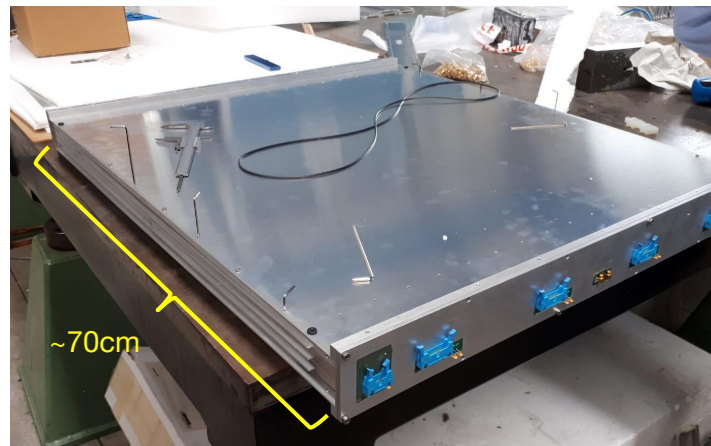


BACKUP



Camere a deriva (mini-DT)

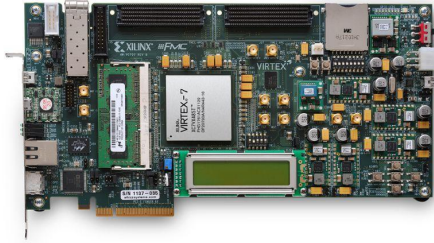
- Costruzione e operazione di camere a deriva presso il LAE di LNL
 - Repliche a footprint ridotto ($\sim 0.5 \text{ m}^2$) delle DT di CMS
 - Readout compatibile con Phase2 upgrade di CMS
- Utilizzate in diverse applicazioni:
 - Sviluppo sistema DAQ triggerless e online processing
 - Sviluppo di algoritmi di trigger basati su Reti Neurali su FPGA
 - Testbed per elettronica di Phase2 di CMS-DT (OBDT, in sviluppo a PD)
 - Muon-spectrometer per testbeam collaborazione LEMMA
 - Previsto il deployment nel corso della presa dati di MUTOMCA (muon tomography)
- 8 camere costruite
 - 4 (+1 spare) correntemente usate in uso in configurazione “telescopio” presso il LAE
 - 1 al CERN per test di integrazione dell’elettronica di readout e trigger di CMS on-site
 - 2 assemblate assieme a colleghi di INFN-BO, interessati a replicare un setup simile a BO



Camere a deriva (mini-DT)

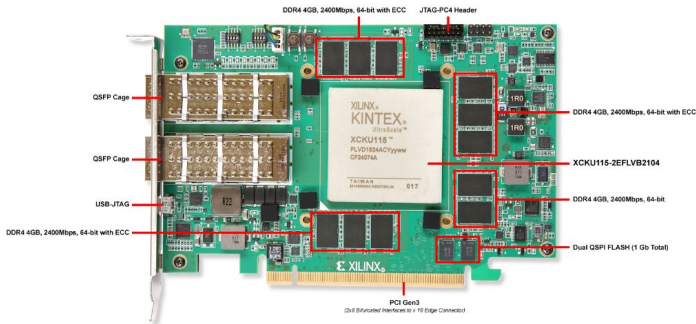
2x Xilinx VC707 ev. Boards

- TDCs in FW
- GBTx-FPGA protocol to 10Gbps SFP+ transceivers



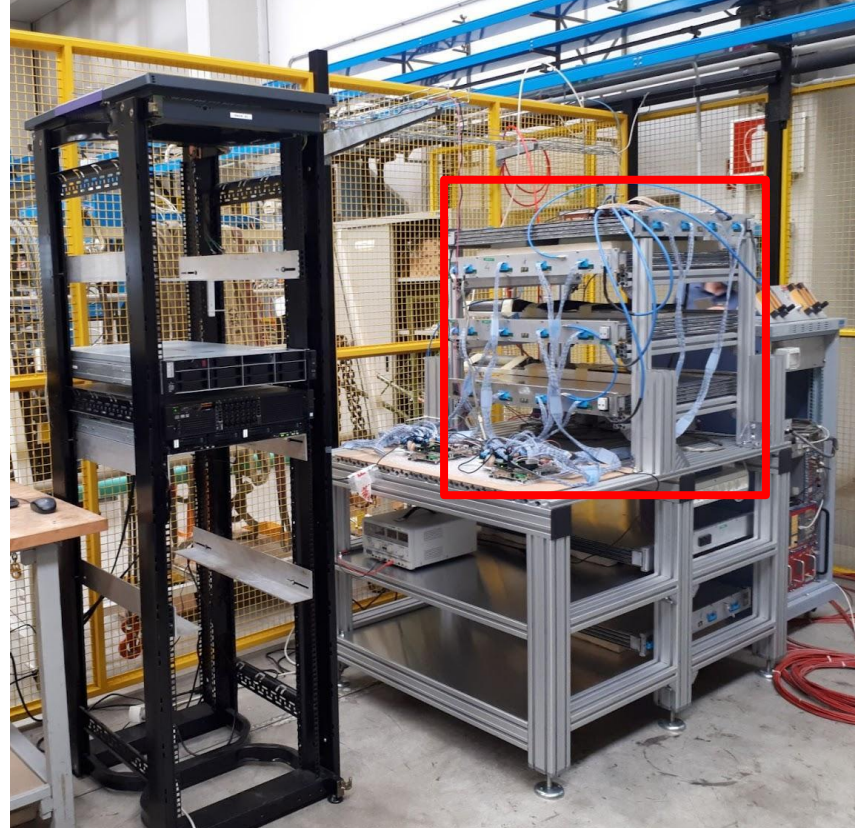
Xilinx KCU1500 ev. Boards

- Concentrator of up to 8 GBT links
- DMA data transfer over PCIe



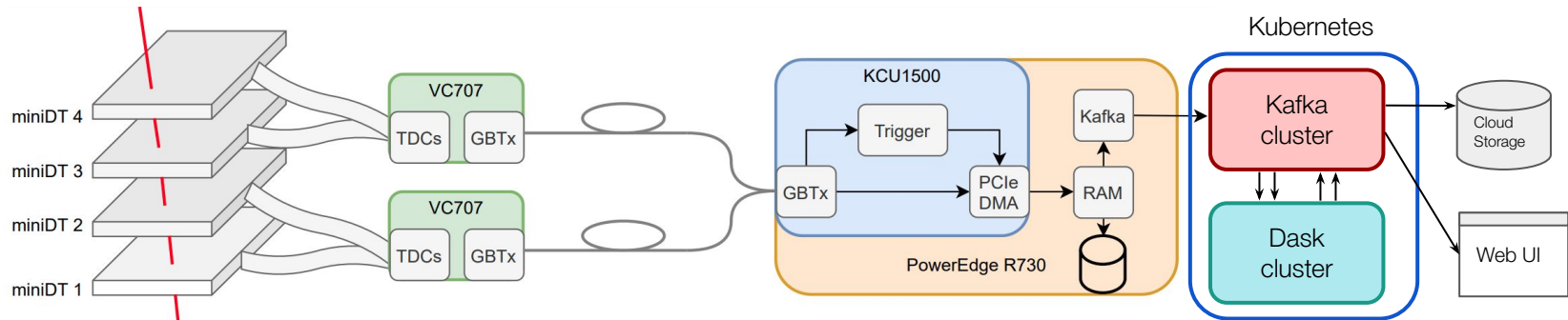
Rack slow-control e computing “on-site”

Experimental stand equipaggiato con 4 mini-DTs



Sviluppo di metodi di acquisizione e online-processing di stream di dati

- Mini-DT usate come testbed per lo studio e implementazioni di sistemi di acquisizione **Triggerless** e **Processing Online**
 - Acquisizione in trigger-less mode di tutte le hits prodotte dalle camere
 - Processing online del 100% delle hits prodotte usando strumenti di calcolo distribuito (Apache Kafka, Apache Spark/Dask)
 - Processing online svolto “off-site” su risorse cloud (INFN Cloud e/o Cloud Veneto)
 - Sviluppo di architetture per il processing **scalabili** e facilmente **portabili** a molteplici use-cases
 - Deployment containerizzato basato su Kubernetes
 - Elasticità e portabilità potenzialmente vantaggiose anche per lo sviluppo di processing online per esperimenti locali e test beams
 - Discussioni attualmente in corso per l’integrazione di questi sistemi con DAQ e DT di CMS



Sviluppo di trigger basati su reti neurali

- Sviluppo di algoritmi basati su reti neurali per la ricostruzione veloce in FW di segmenti per il trigger locale delle DT di CMS
 - Problema “semplice” ma caratterizzato da alto combinatorio (specialmente ad alto PU)
 - Reti neurali permettono di eliminare il combinatorio
 - Tempi di inferenza della rete di $O(2)$ clock ($\rightarrow \sim 50$ ns)
 - Latenza fissa indipendentemente dalla complessità degli input
 - Tuning importante per contenere l’utilizzo delle risorse:
 - Scelta architettura NN
 - Quantizzazione pesi
 - Pruning modello

