

PID meeting

- SCATS : design status and simulation results
- PIF : status
- Milestones

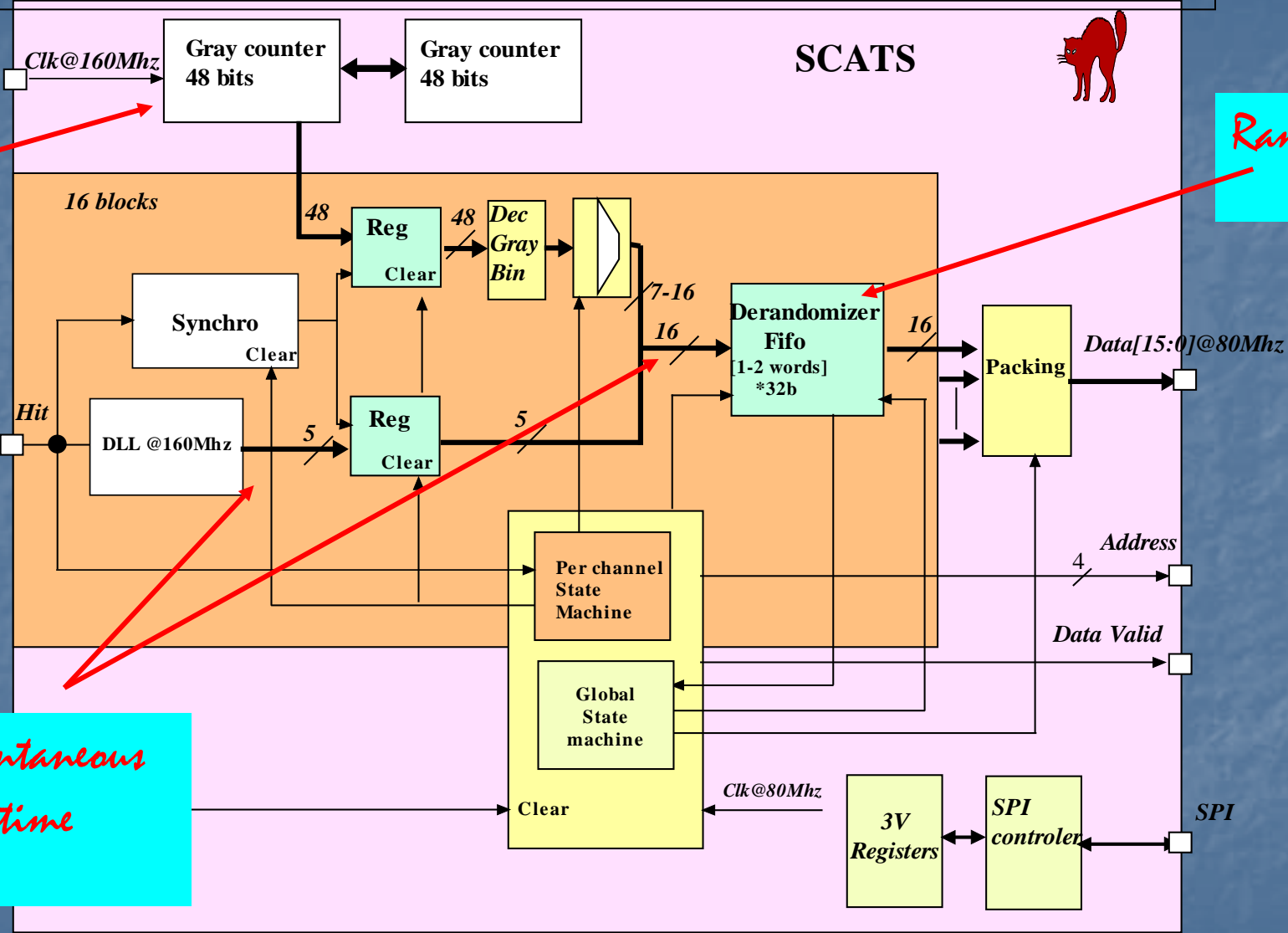
SCATS



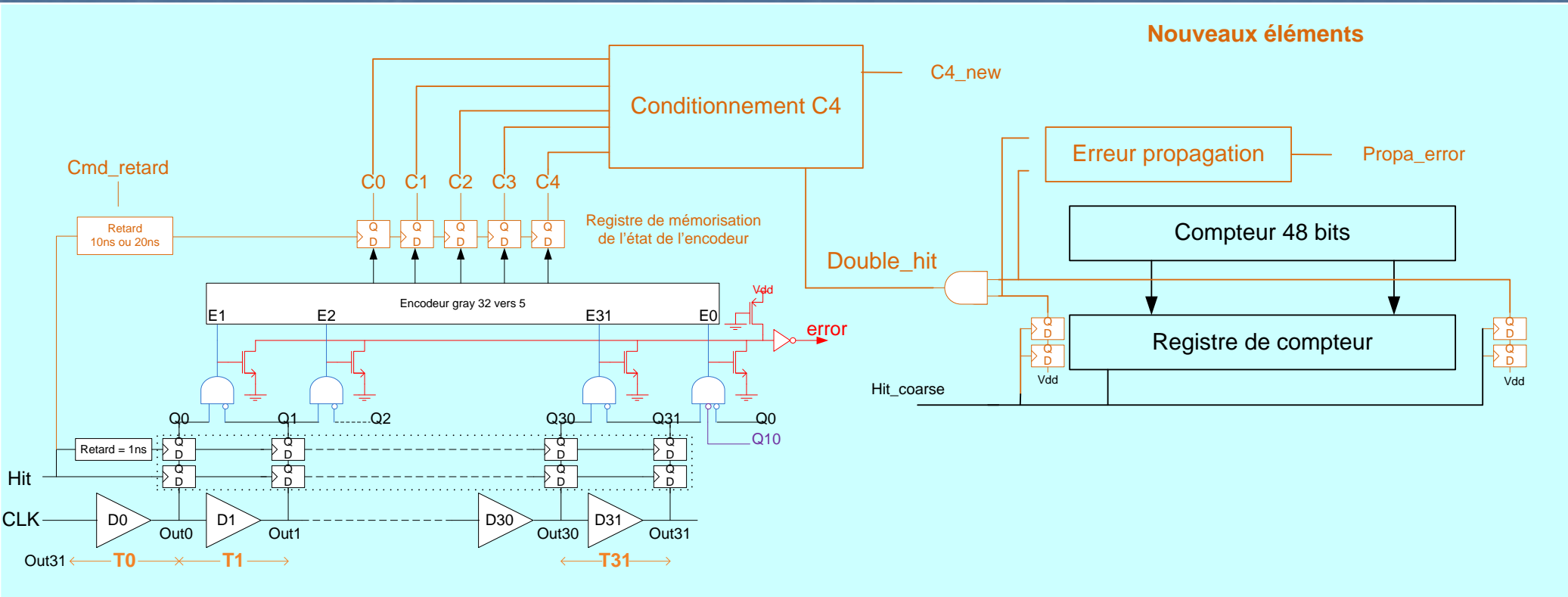
2 voting

Ram size

Instantaneous Dead time

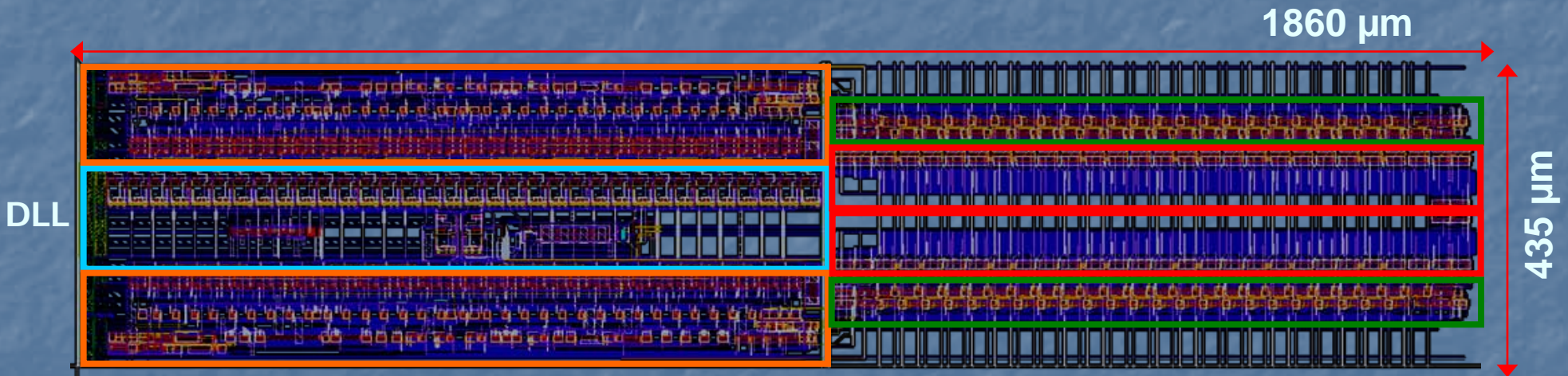
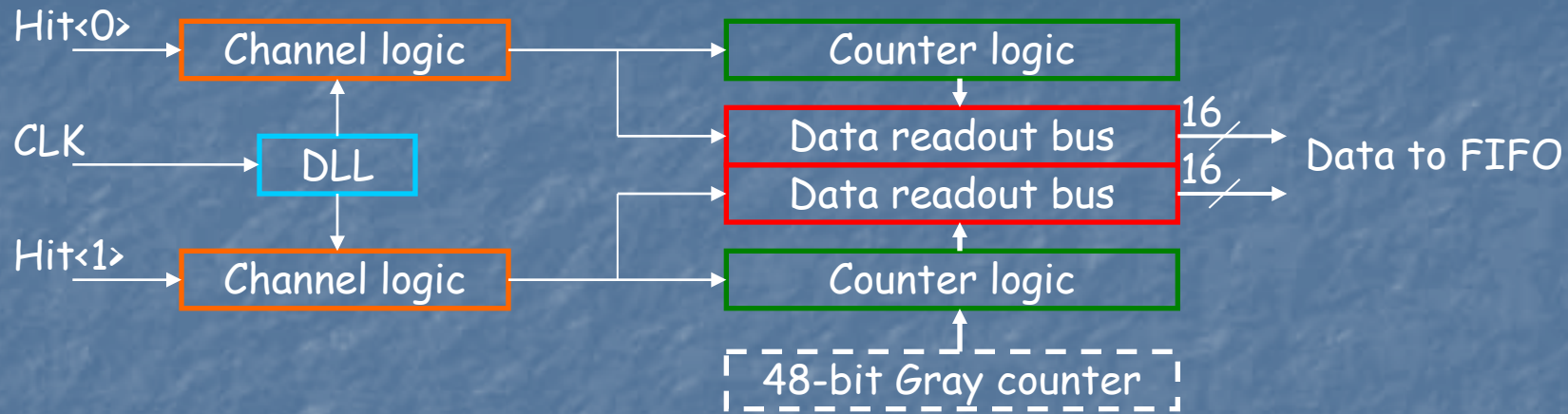


Front end Upgrade



Scheme, simulation & layout : done

2-channel block's layout



Synchronizer - 32-bit register
 Transitions detector - Binary encoder

48-bit register
 Gray to binary encoder
 4 x 16-bit multiplexed tristate bus

Front end Upgrade

LVDS receiver :

- Differential input stage (NMOS to PMOS)
 - ↳ *Scheme, simulation & Layout to be done*
- Redesign the hit output buffer :
 - ↳ *Buf15 from vendor library corelib3B (existing solution)*
- Power supplies have to be separated between hits et clk:
 - ↳ *Schemes, simulation & Layout to be done*
- Signal input polarity selection :
 - ↳ *Schemes, simulation & Layout to be done*

Front end Upgrade

Others :

- Inhibition of hits to avoid false triggering (edge trigger)
 - ↳ *Schemes, layout & simulation done*
- Suppression of the test channel
 - ↳ *Schemes done ; Layout to be done*
- More configuration bits needed for setup
 - ↳ *New setup registers*
Schemes, simulation & Layout to be done
- FIFO data bus (individual channel)
 - ↳ *Schemes, layout & simulation done*

Front end Upgrade

others :

- More robust connection between the counter and DLL
 - ↳ *Schemes, layout & simulation done*
- Design more robust to the clock duty cycle variations
 - ↳ *Schemes, layout & simulation done*
- Design error detection on the counter due SUE
 - ↳ *Schemes done ; Layout & simulation to be done*

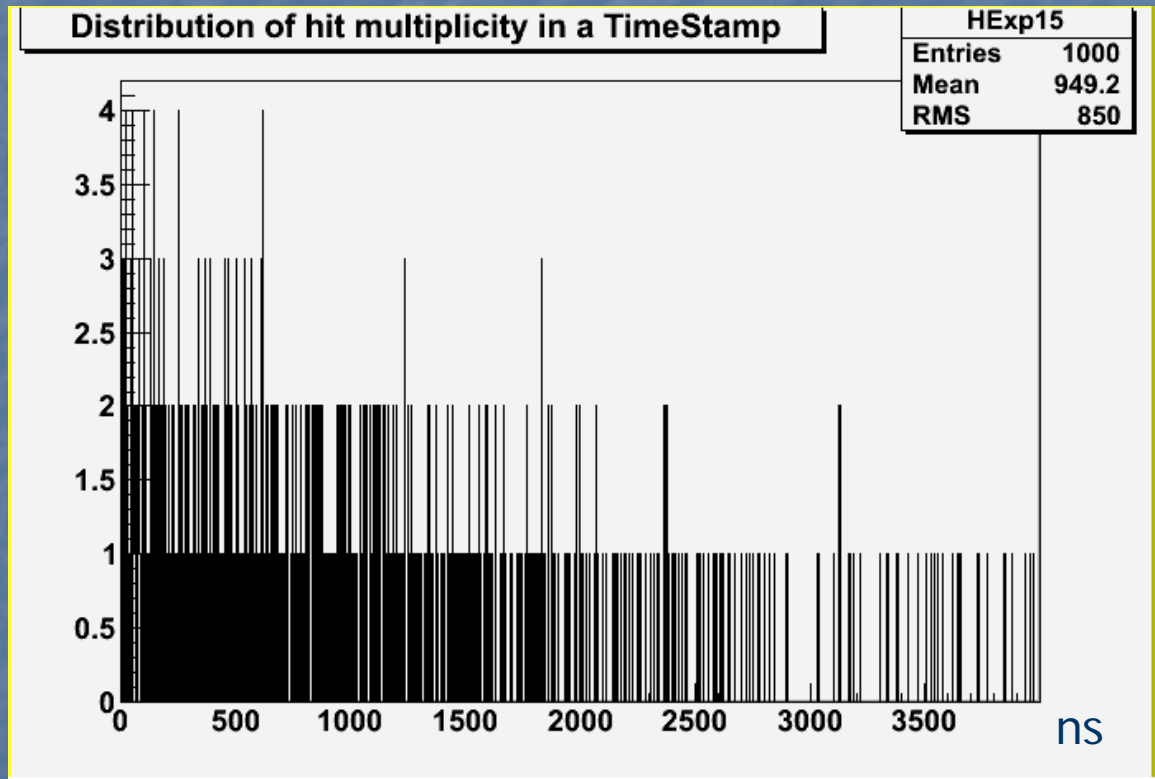
Readout Simulation

Design of the readout part is done in Verilog. Simulation performed with Modelsim

- Behavioral simulation (no delays)
- Code is targeted in a Actel family FPGA in order to have a post-synthesis evaluation of the performances closer to the reality
- Two designs tested: 16-bit x 32-word and 32-bit x 16-word RAM .

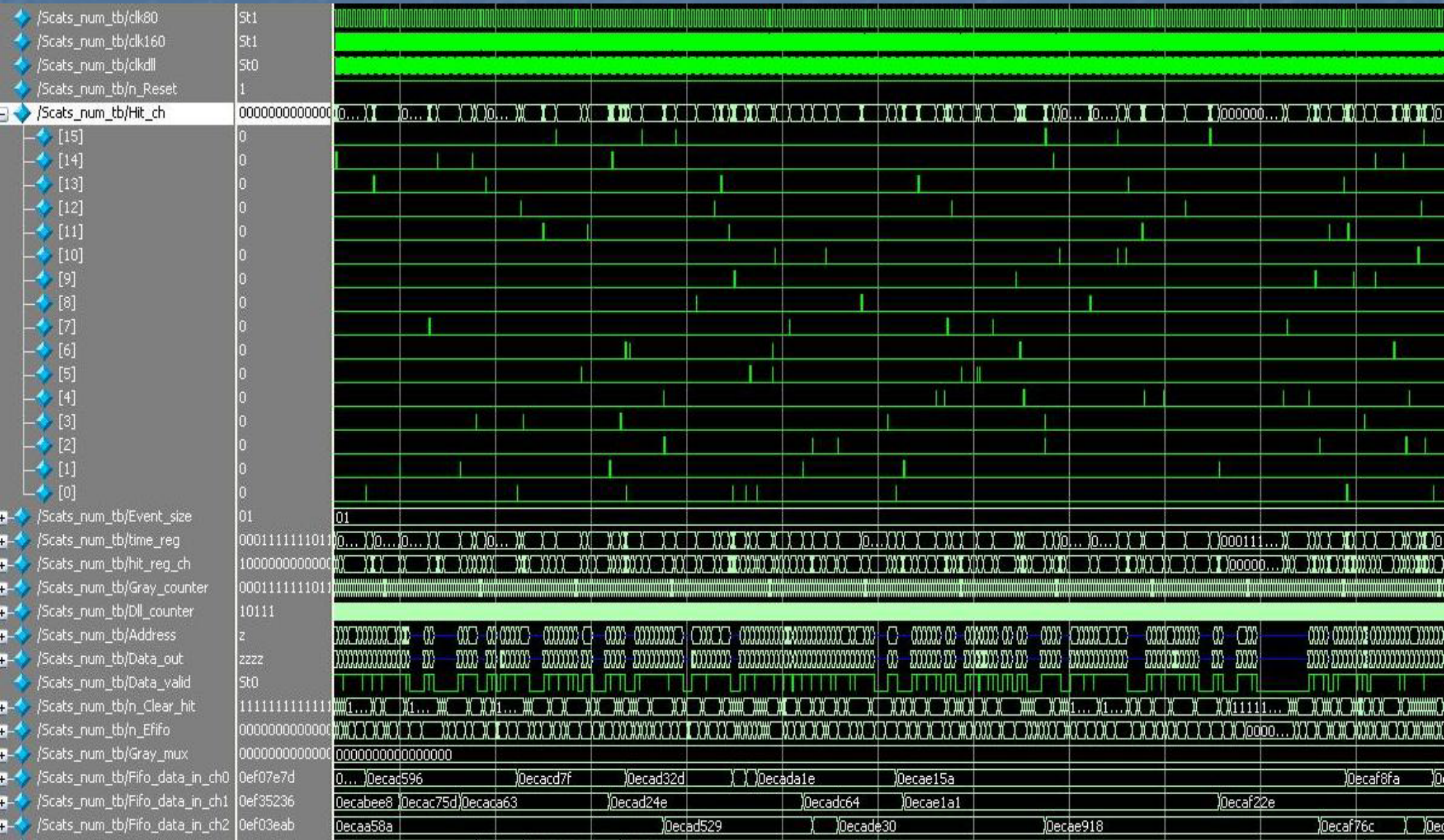
Simulation model

Exponential distribution model of delta time between hits used for simulation
- Mean rate \sim 1MHz



Hits input: timing distribution

250 ns



Readout simulation : results

Nb Of Input Hits channel 0 :	1001,	Accepted Hits :	971,	Rate :	97.00	Max Nb Of words in fifo:	2
Nb Of Input Hits channel 1 :	1001,	Accepted Hits :	961,	Rate :	96.00	Max Nb Of words in fifo:	3
Nb Of Input Hits channel 2 :	1001,	Accepted Hits :	978,	Rate :	97.70	Max Nb Of words in fifo:	4
Nb Of Input Hits channel 3 :	1001,	Accepted Hits :	964,	Rate :	96.30	Max Nb Of words in fifo:	3
Nb Of Input Hits channel 4 :	1001,	Accepted Hits :	968,	Rate :	96.70	Max Nb Of words in fifo:	3
Nb Of Input Hits channel 5 :	1001,	Accepted Hits :	971,	Rate :	97.00	Max Nb Of words in fifo:	3
Nb Of Input Hits channel 6 :	1001,	Accepted Hits :	965,	Rate :	96.40	Max Nb Of words in fifo:	4
Nb Of Input Hits channel 7 :	1001,	Accepted Hits :	977,	Rate :	97.60	Max Nb Of words in fifo:	5
Nb Of Input Hits channel 8 :	1001,	Accepted Hits :	972,	Rate :	97.10	Max Nb Of words in fifo:	4
Nb Of Input Hits channel 9 :	1001,	Accepted Hits :	969,	Rate :	96.80	Max Nb Of words in fifo:	4
Nb Of Input Hits channel10 :	1001,	Accepted Hits :	970,	Rate :	96.90	Max Nb Of words in fifo:	3
Nb Of Input Hits channel11 :	1001,	Accepted Hits :	971,	Rate :	97.00	Max Nb Of words in fifo:	4
Nb Of Input Hits channel12 :	1001,	Accepted Hits :	968,	Rate :	96.70	Max Nb Of words in fifo:	5
Nb Of Input Hits channel13 :	1001,	Accepted Hits :	968,	Rate :	96.70	Max Nb Of words in fifo:	4
Nb Of Input Hits channel14 :	1001,	Accepted Hits :	972,	Rate :	97.10	Max Nb Of words in fifo:	4
Nb Of Input Hits channel15 :	1001,	Accepted Hits :	977,	Rate :	97.60	Max Nb Of words in fifo:	4

Readout simulation : results

Fifo 0	Fifo 1	Fifo 2	Fifo 3	Fifo 4	Fifo 5	Fifo 6	Fifo 7	Fifo 8	Fifo 9	Fifo10	Fifo11	Fifo12	Fifo13	Fifo14	Fifo15
Nb Of words= 1:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words= 2:	970	959	973	961	965	966	952	970	960	956	954	956	946	949	946
Nb Of words= 3:	0	1	1	1	1	3	4	1	5	6	9	4	7	7	13
Nb Of words= 4:	0	0	1	0	0	0	1	1	1	1	0	3	4	4	8
Nb Of words= 5:	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0
Nb Of words= 6:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words= 7:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words= 8:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words= 9:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words=10:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words=11:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words=12:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words=13:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words=14:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words=15:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words=16:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words=17:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words=18:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words=19:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Nb Of words=20:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Performances : 16-bit input Ram

1MHz Hit rate per channel

One word :

Average Nb of hits accepted : ~98%

Maximum number of words in fifo (average on the 16 channels) : 1,5

Two words:

Average Nb of hits accepted : ~ 97%

Number of words in fifo : 2-5 max (3,5 in average)

Three words :

Average Nb of hits accepted : ~ 95-96%

Number of words in fifo (average on the 16 channels) : 5-10 words

Four words :

Average Nb of hits accepted : 93-95%

Number of words in fifo (average on the 16 channels) : 8-20 words

Performances : 16 bit input Ram

2 MHz Hit rate per channel

One word :

Average Nb of hits accepted : ~ 95 %

Number of words in fifo (average on the 16 channels)

Two words :

Average Nb of hits accepted : ~ 93 %

Number of words in fifo (average on the 16 channels) :8-10 words

Three words :

Average Nb of hits accepted : FAIL ...

Number of words in fifo (average on the 16 channels) : more than 63

Performances 32 bit input Ram

1 MHz Hit rate per channel

One word :

Average Nb of hits accepted : ~ 94-96%

Number of words in fifo (average on the 16 channels)

Two words :

Average Nb of hits accepted : ~ **97,6%**

Number of words in fifo (average on the 16 channels) :3

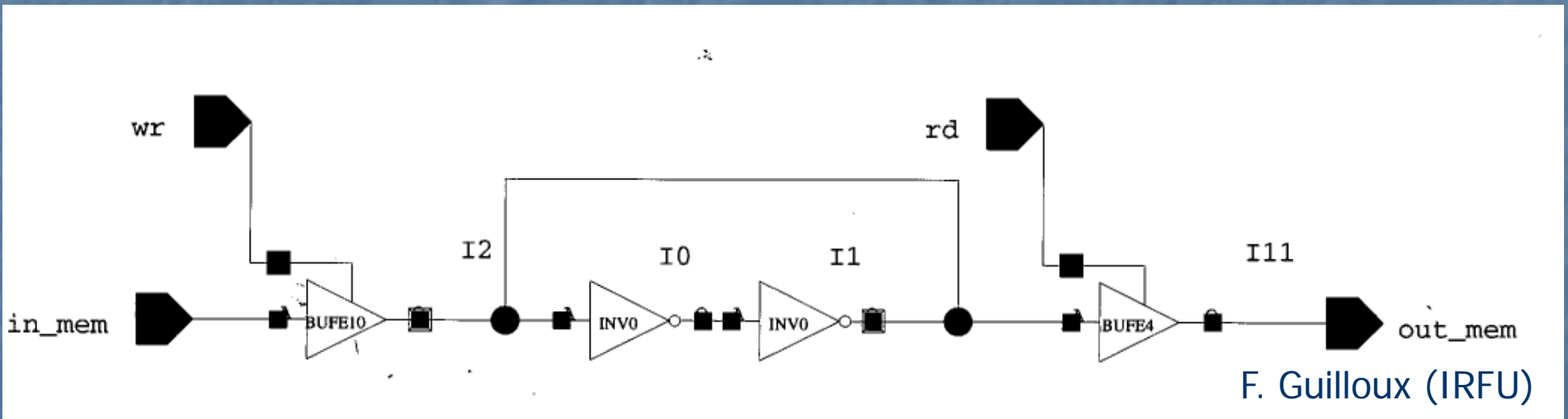
2 MHz Hit rate per channel

Two words :

Average Nb of hits accepted : 96 %

Number of words in fifo : 6 max

- RAM size : conclusions
 - AMS library :
 - 315u x 487u , 128 x 8 is the smallest for free
 - 6K Euros to buy a dedicated IP.
 - 32-bit input is obviously the best choice .
 - Trade-off between depth / hit rate performance to be found for cases with 3 and 4 words
 - > Consequences on size and cost
 - Design of the elementary cell has started .



- Test and simulation coming soon .
- Design will be more robust against latchup than AMS's.
 - Same design rules than for the Delay Chip (tested in radiation)

- Command and control
 - SPI control bus for writing and reading internal registers is implemented.
 - Triple voting registers : 6 setup registers and status moved into the digital part of the chip

Front end chip

- No relevant progress on PIF has been done since last meeting.
- From the simulation of the SCATS, the specs for the output design architecture and the synchronisation of the PIF can be studied more precisely :
 - FIFO in each channel (complexity)
 - Output mux or 16 outputs (pinout issue)
 - Synchronisation between TDC and PIF (handshake or adjustable timing setup)
 - ADC issue .

Conclusion

SCATS is well on tracks.

➤ Submission in May 2011 seems reasonable
1st prototype: around 3 months later

- PIF :
 - Need to finalise the complete architecture
 - Design of the CFD part will start very soon .
- One PM 8500 has been ordered to have a test setup @ LAL