



SuperB IFR electronics:
beam test of the prototype IFR detector at Fermilab

A. Cotta Ramusino on behalf of the Ferrara SuperB group

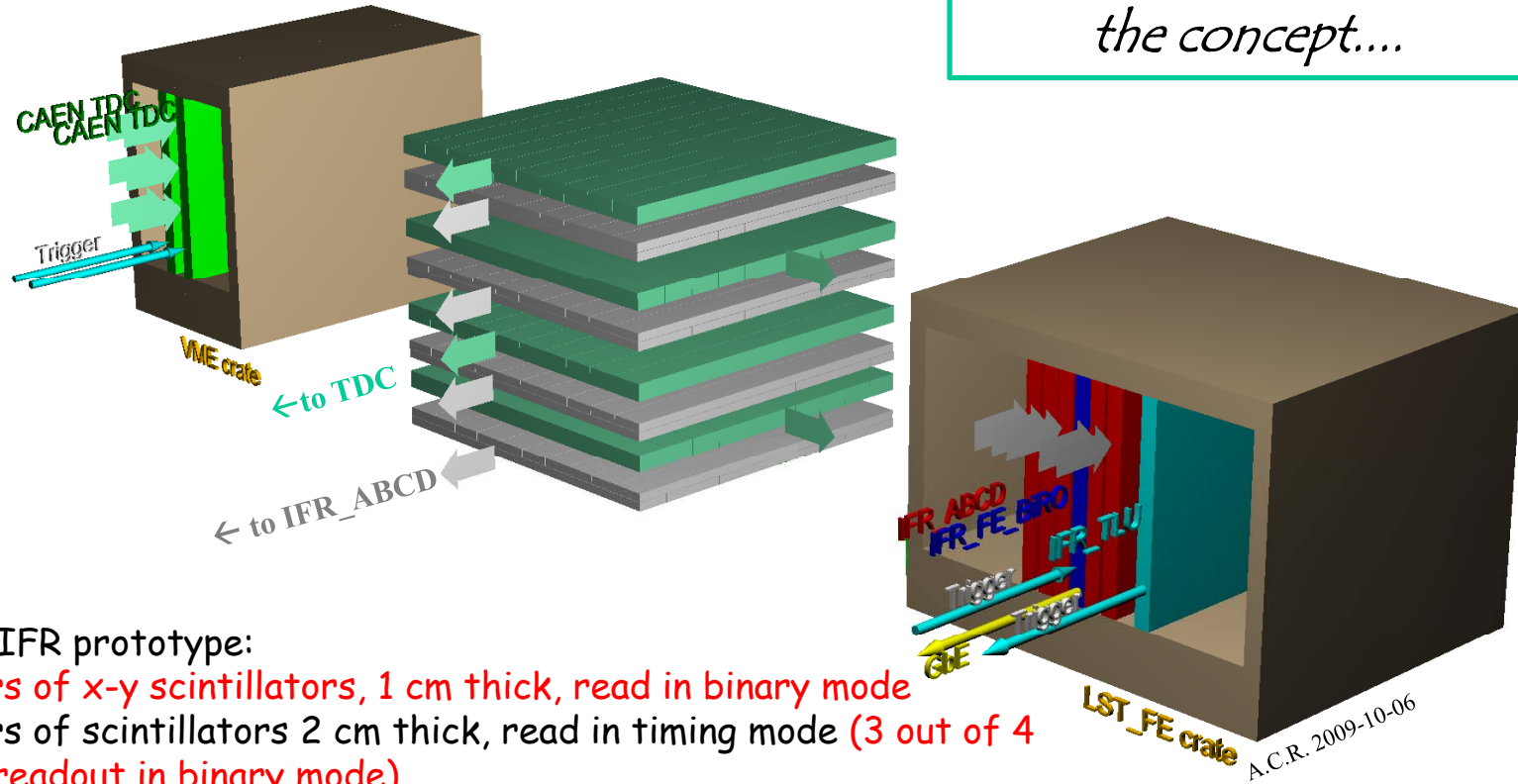
Outlook

- Beam test at Fermilab of the IFR prototype electronics and DAQ system

SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system



the concept....



SuperB IFR prototype:

- 5 layers of x-y scintillators, 1 cm thick, read in binary mode
- 4 layers of scintillators 2 cm thick, read in timing mode (3 out of 4 also readout in binary mode)

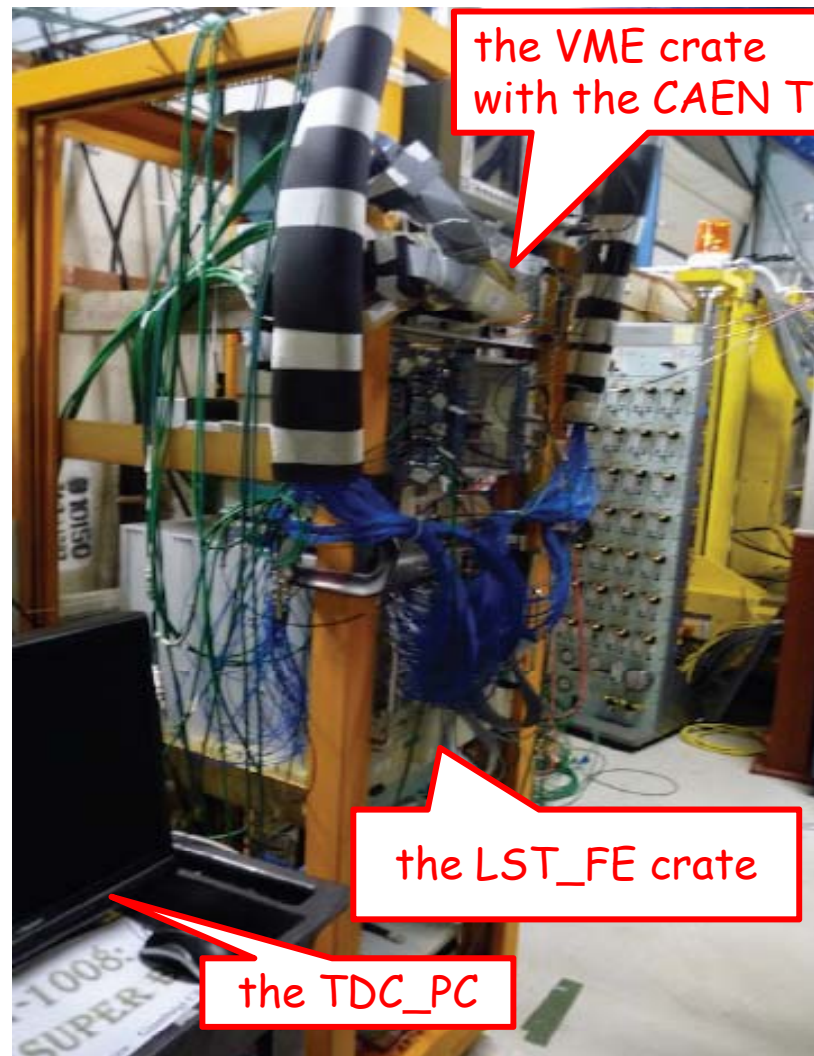
SuperB-IFR prototype readout electronics:

- "IFR_ABCD": sensor Amplification, Bias-conditioning, Comparators, Data processing: it samples the level of the comparators outputs @ $\geq 80\text{MHz}$ and stores it, pending the trigger request
- "CAEN_TDC": a multi-hit TDC design based on CERN HP-TDC; hosted in a VME crate and read out via a VME-PCI bridge to the DAQ PC
- "IFR_FE_BiRO": collects data from IFR_ABCD cards upon trigger request and sends it to DAQ PC (via GbE)
- "IFR_TLU": a module (Trigger Logic Unit) to generate a fixed latency trigger based on primitives from the IFR prototype itself or from external sources

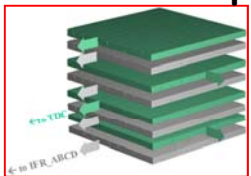
IFR_FE_BiRO + IFR_TLU are actually a single module

...and the real thing!

pictures from G. Cibinetto, "Some note on the beam test" presented at this meeting

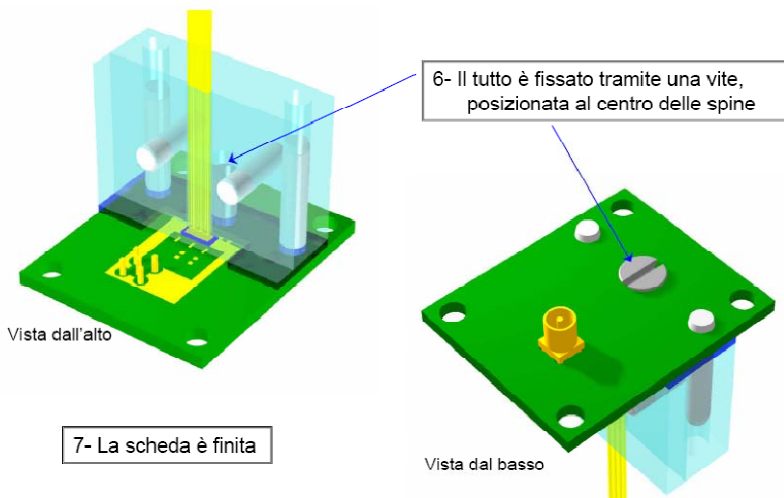


SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system SiPM carrier PCB



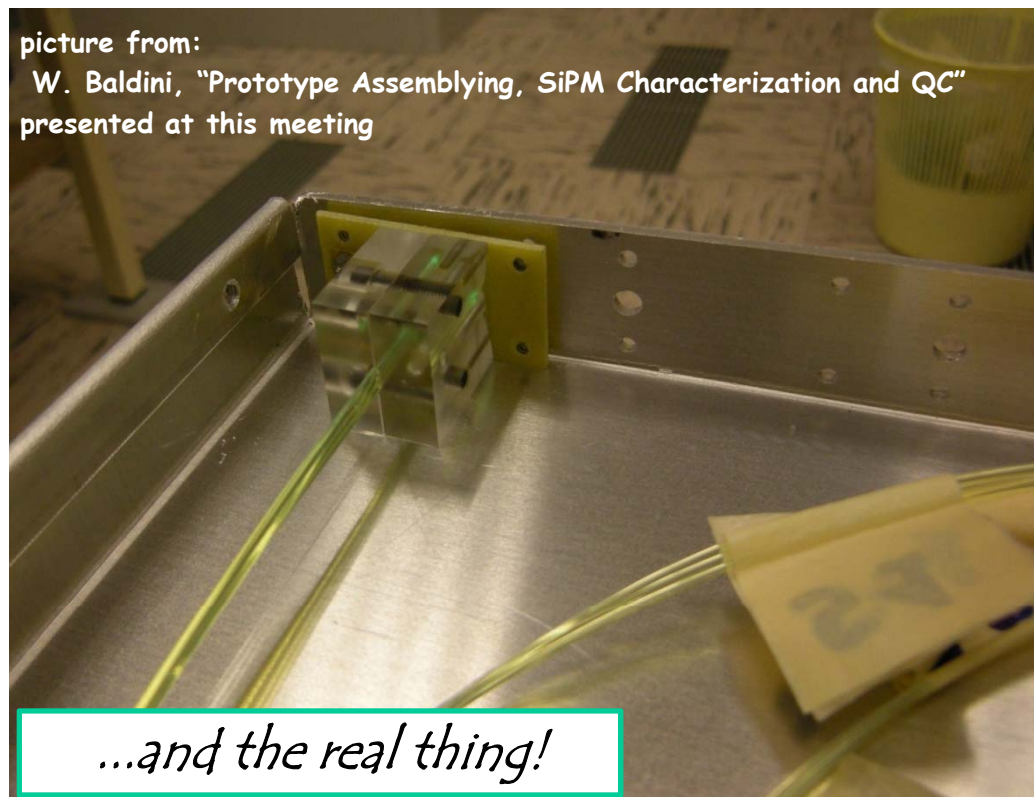
the concept...

Schema per l'assemblaggio



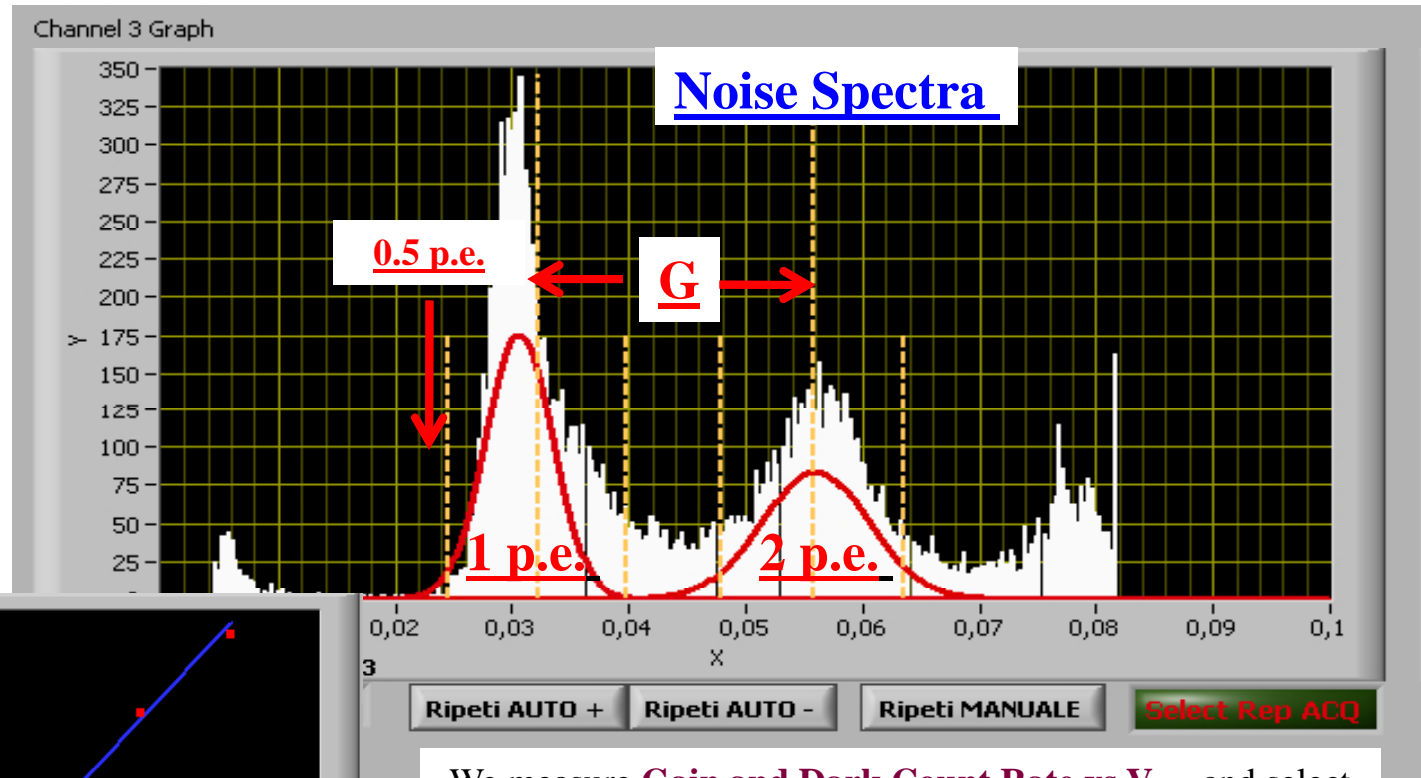
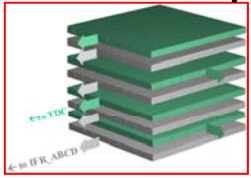
picture from:

W. Baldini, "Prototype Assembling, SiPM Characterization and QC"
presented at this meeting



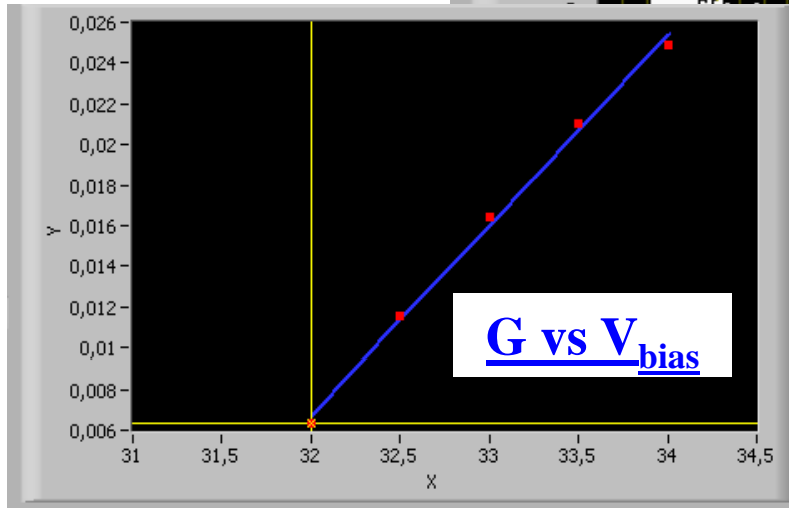
...and the real thing!

SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system
SiPM characterization



We measure **Gain and Dark Count Rate vs V_{bias}** and select the most homogeneous devices for each type

From: W. Baldini,
"Prototype Assembly, SiPM Characterization and QC"
presented at this meeting



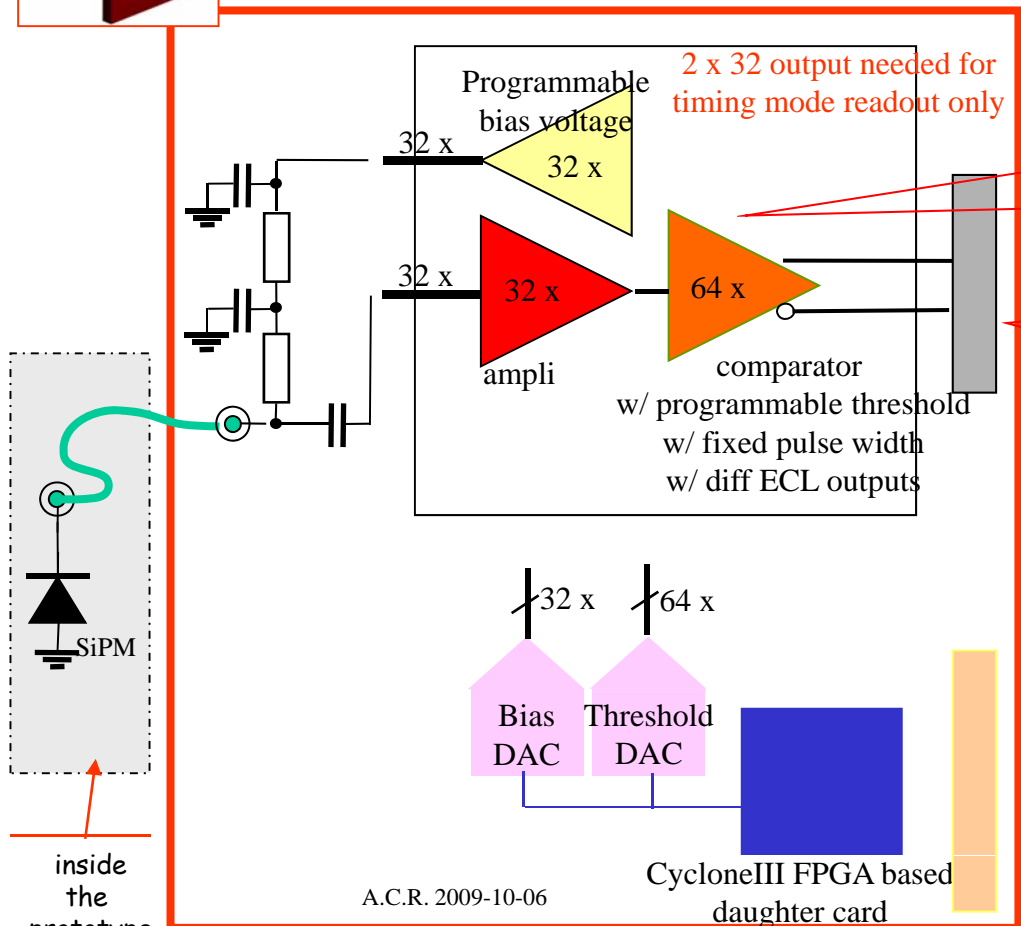
SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system



dimensions: VME 6U x 220mm

"IFR_ABCD" card features:

- ampli: two stage w/discrete components: BGA2748 + BGA2716
- discri: ADCMP563BRQ (ECL out, dual)



For the readout in timing mode of the SuperB IFR prototype it is foreseen to use two comparators at different thresholds for each sensor

signal connector compatible with BaBar IFR signal cables (re-usable): KEL 8831E-034-170LD

- DAC: LTC2625CGN#PBF (I²C, 12bit, octal)
- FPGA: Cyclone III ALTERA EP3C25Q240C8

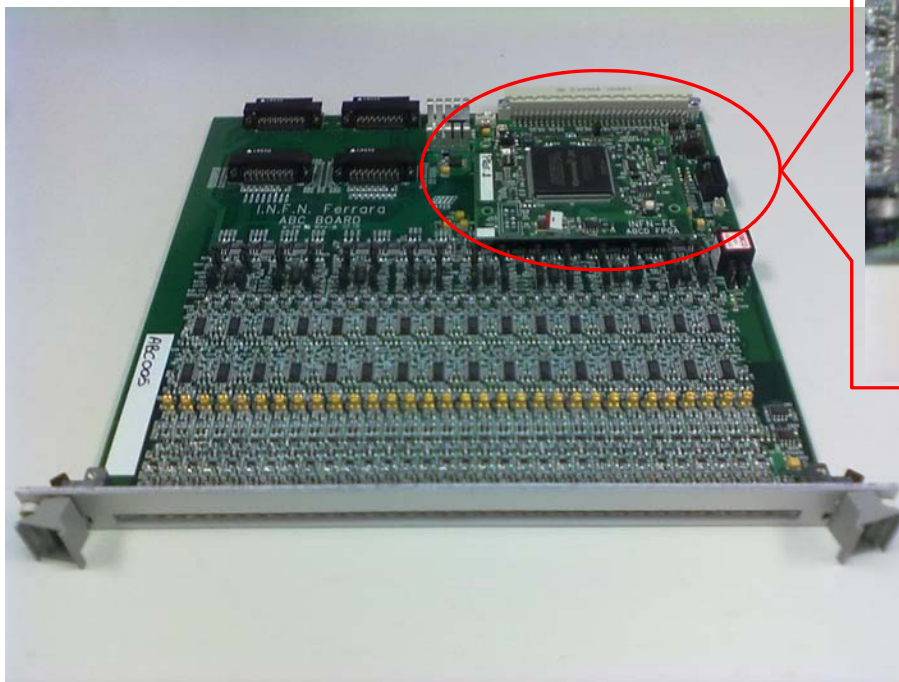
inside the prototype "pizza box"

Outline of the **"IFR_ABCD"** card
(Amplifier, Bias, Comparator, DataProcessing)

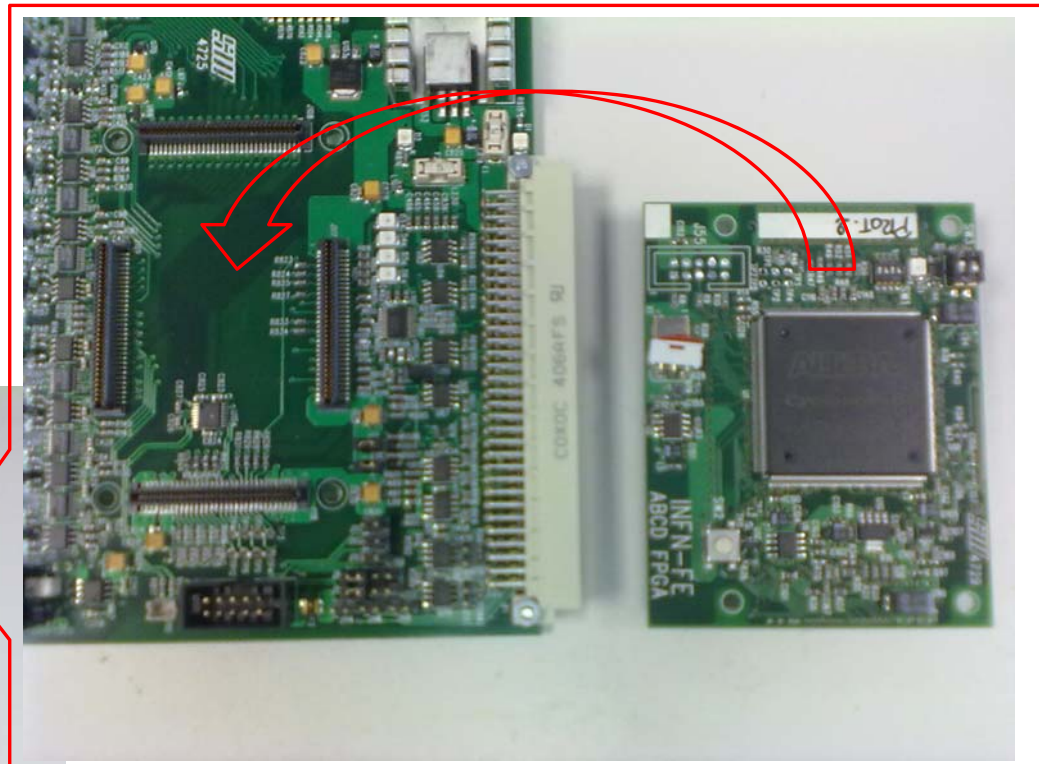
TOTAL "IFR_ABCD" cards produced: 12
To enable the reading of a 9th prototype layer

IFR_ABCD card: MMIC ampli design & test, schematics, and layout pre-placement by **R. Malaguti**, INFN-Ferrara

SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system

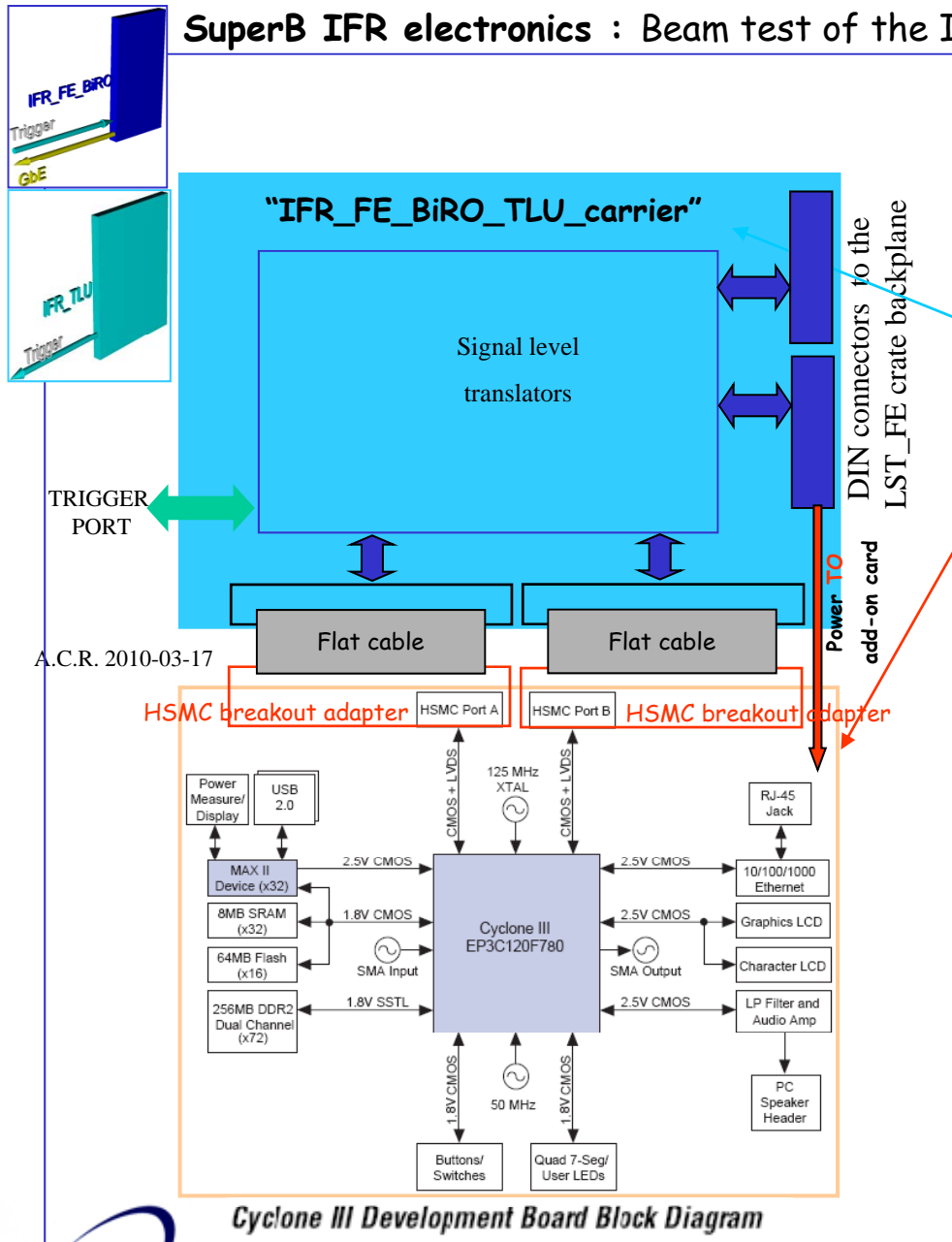


"IFR_ABCD" card



Detail of the digital "IFR_ABCD" daughter card

SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system



"IFR_FE_BiRO_TLU" module features:

The functions of the **IFR_FE_BiRO** and of the **IFR_FE_TLU** cards are combined into a single system made of

- a **carrier card** which fits in the "LST_FE" crate (6U x 220mm depth)
- an **add-on card** : it's simply the ALTERA Cyclone III development kit (DK-DEV-3C120N) equipped with breakout adapters for the kit's HSMC connectors

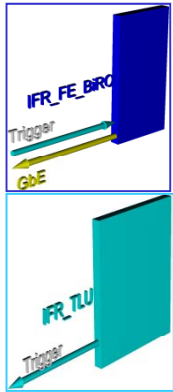
The **carrier card** hosts level adaptors and application specific I/O ports which allow the **add-on card** to:

- receive power
- receive the "fast OR" signals from the "ABCD" cards to generate triggers from
- generate and distribute triggers (also to the TDC system)
- generate and distribute clock and reset signals (also to the TDC system)
- poll data from the "ABCD" cards
- configure the programmable resources on the "ABCD" cards
- connect to the host PC running the DAQ software via ethernet (tcp/ip)

Total "**IFR_FE_BiRO_TLU**" needed for the prototype readout: **1**

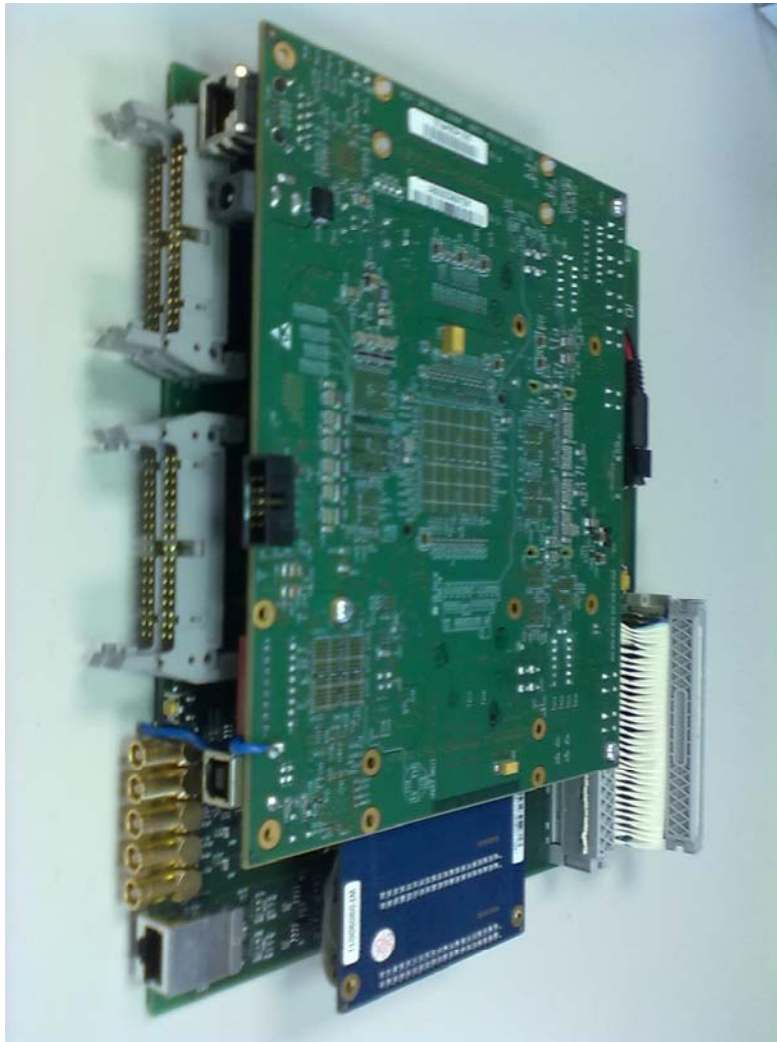
Cyclone III Development Board Block Diagram

Outline of the "IFR_FE_BiRO_TLU" module



SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system

"IFR_FE_BiRO_TLU" module features: (continues)



the "IFR_FE_BiRO_TLU" module

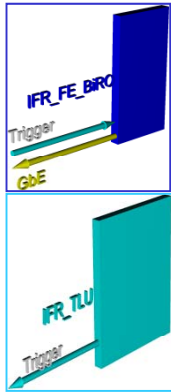
The FPGA on board the **add-on** card is connected to the RUN CONTROL/DAQ PC of the prototype test setup via an Ethernet port.

The FPGA features a NIOS-II microcontroller which implements the full TCP/IP stack.

The NIOS-II receives commands (i.e. START, STOP, INIT) from the RUN CONTROL/DAQ PC on a TCP server socket and sends data to a TCP server socket on the PC. Data is collected through the LST_FE backplane from the "ABCD" cards upon a trigger request. The data collection section of the FPGA is coded in VHDL.

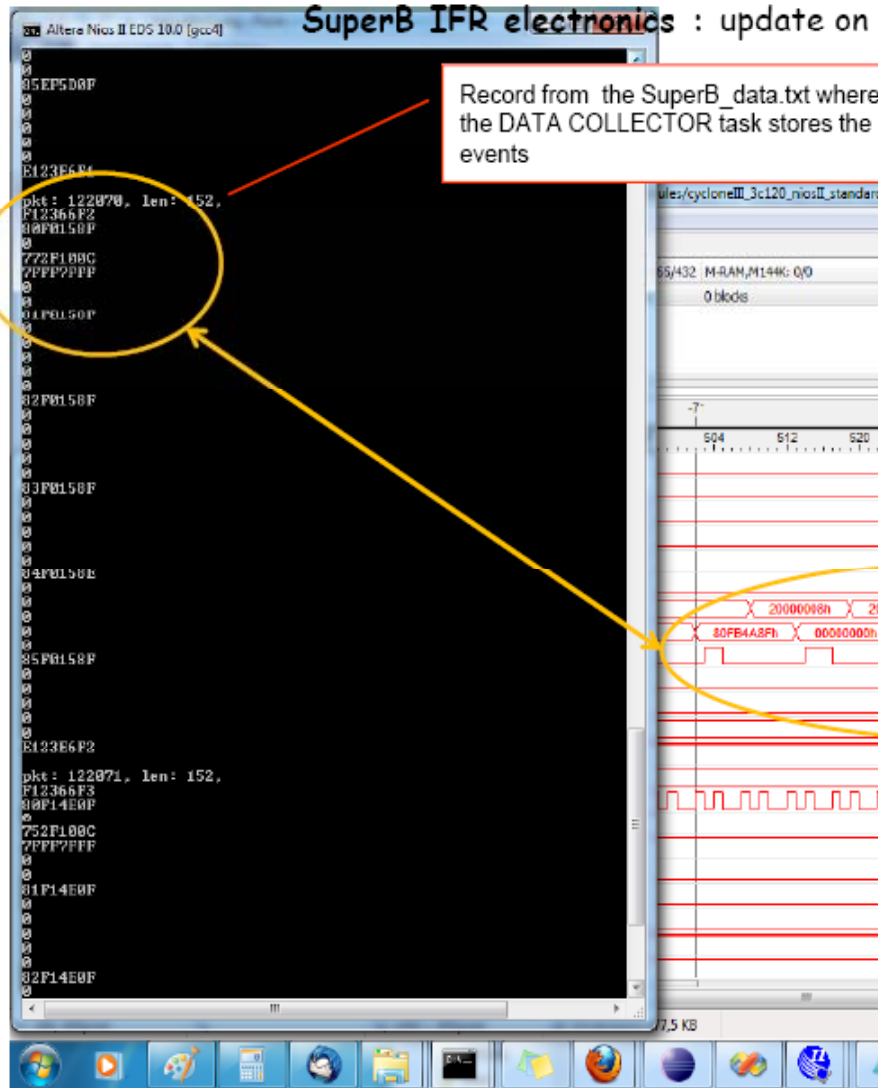
The FPGA of the add-on card generates the timing (clock and reset) for all the digitizers and handles the trigger distribution as well.

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SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system

"IFR_FE_BIRO_TLU" module features:
(continues)



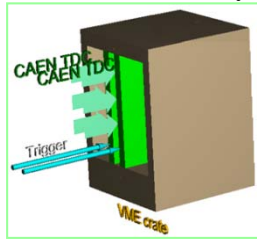
Record from the SuperB_data.txt where the DATA COLLECTOR task stores the events

One "Binary mode" event is the collection of 5 samples, taken 12.5ns apart, of the output of each of the 32 HIGH threshold discriminators, on each of the 8 "ABCD".

The samples from one card are preceded by a board header.

The "ABCD" internal pipeline is dimensioned so that the sample selected by a trigger is most likely the center sample in the group of 5.

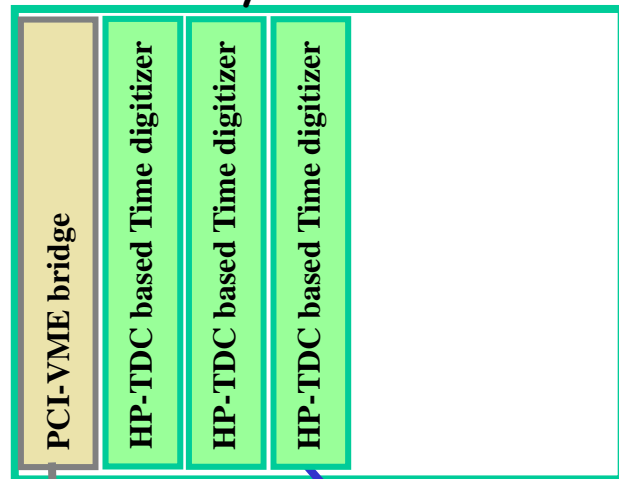
SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system



"TDC subsystem" features:

The **TDC subsystem** uses 3 commercial TDC modules based on CERN's HP-TDC to digitize the time of arrival of the pulses from the "ABCD" boards and from the detectors used in the beam test.

"TDC subsystem" VME crate

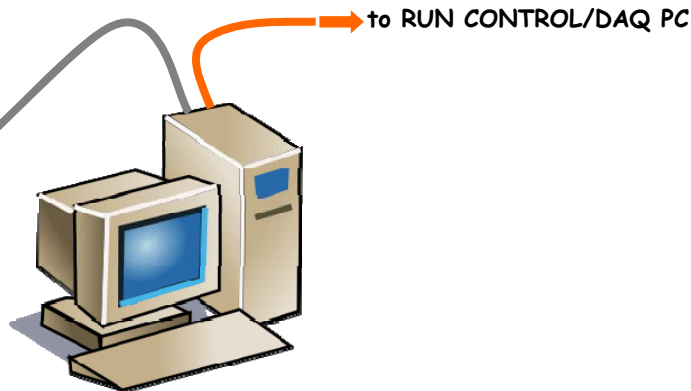


The "**IFR FE BiRO TLU**" provides the 40MHz reference clock to all the TDCs and receives the "Event Ready" ECL output signal from the last TDC in the readout chain.

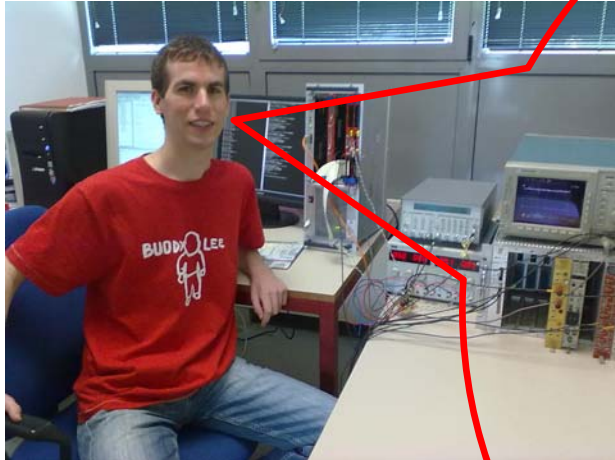
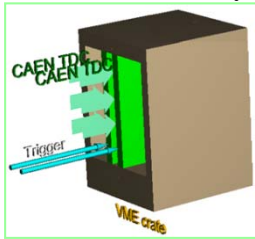
The "Event Ready" signal is released by the TDC module when the event selected by the trigger is read from its output FIFO.

Being the TDC readout slower than the BiRO readout, the detection of the falling edge of the "Event Ready" allows the "**IFR FE BiRO TLU**" to release the IFR_BUSY signal delivered to the beam test TRIGGER LOGIC

The **TDC subsystem** VME crate is controlled and read out by the "TDC-PC" via a PCI-VME bridge.



SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system

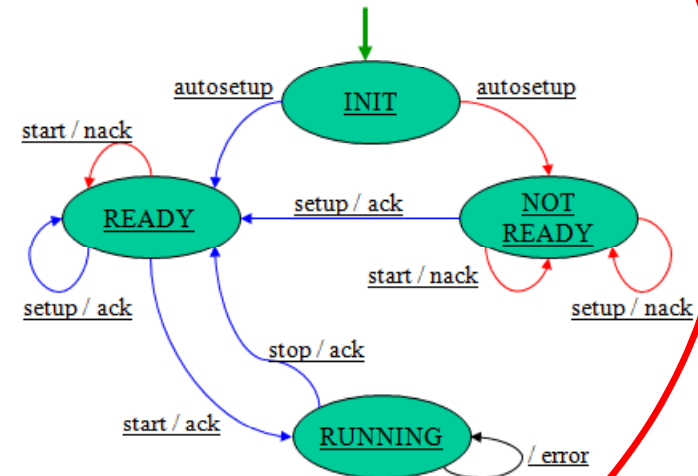


Behavior of the TDC PC

- The behavior of the data acquisition program is illustrated in the FSM bubble diagram. Blue lines mean the operation requested succeeds, otherwise a red line is used.

For each command received, an ack/nack message is sent.

- Running errors are signaled to the OCL via an error message and the running continue.
- INIT is the initial state: in this state a TDC setup is done and then the program waits for connection from the OCL.



XIV SuperB Meeting - LNF

Sept-28-2010

Nicola Dalpasso, Università Ferrara

The "TDC subsystem" control/readout software was part of the thesis work of Nicola Dalpasso (IT student at the University of Ferrara), who extended the basic implementation provided by Stefano Chiozzi of INFN-Ferrara.



XV SuperB Meeting – Caltech

Dec 16 2010

A.Cotta Ramusino, INFN Ferrara

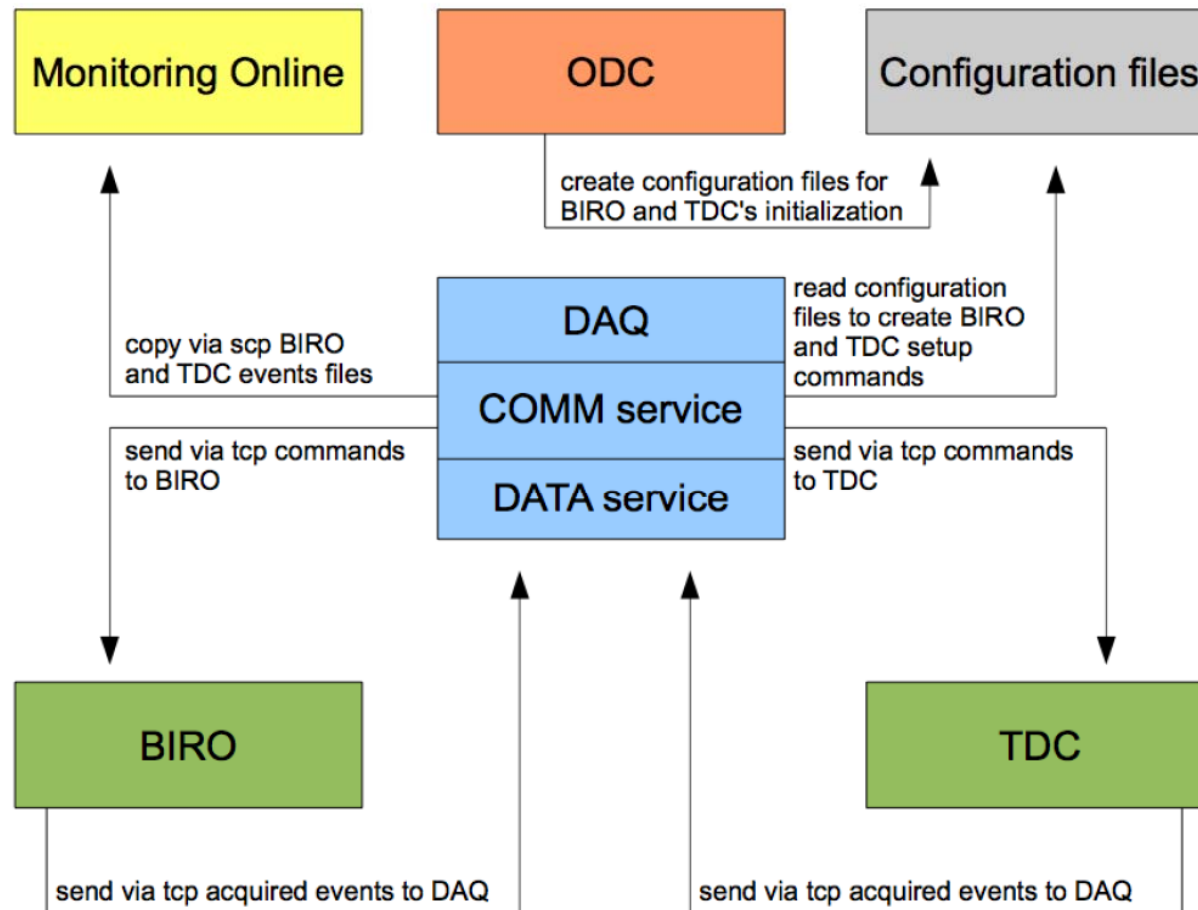


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SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system

Beam test "On Line" software features:

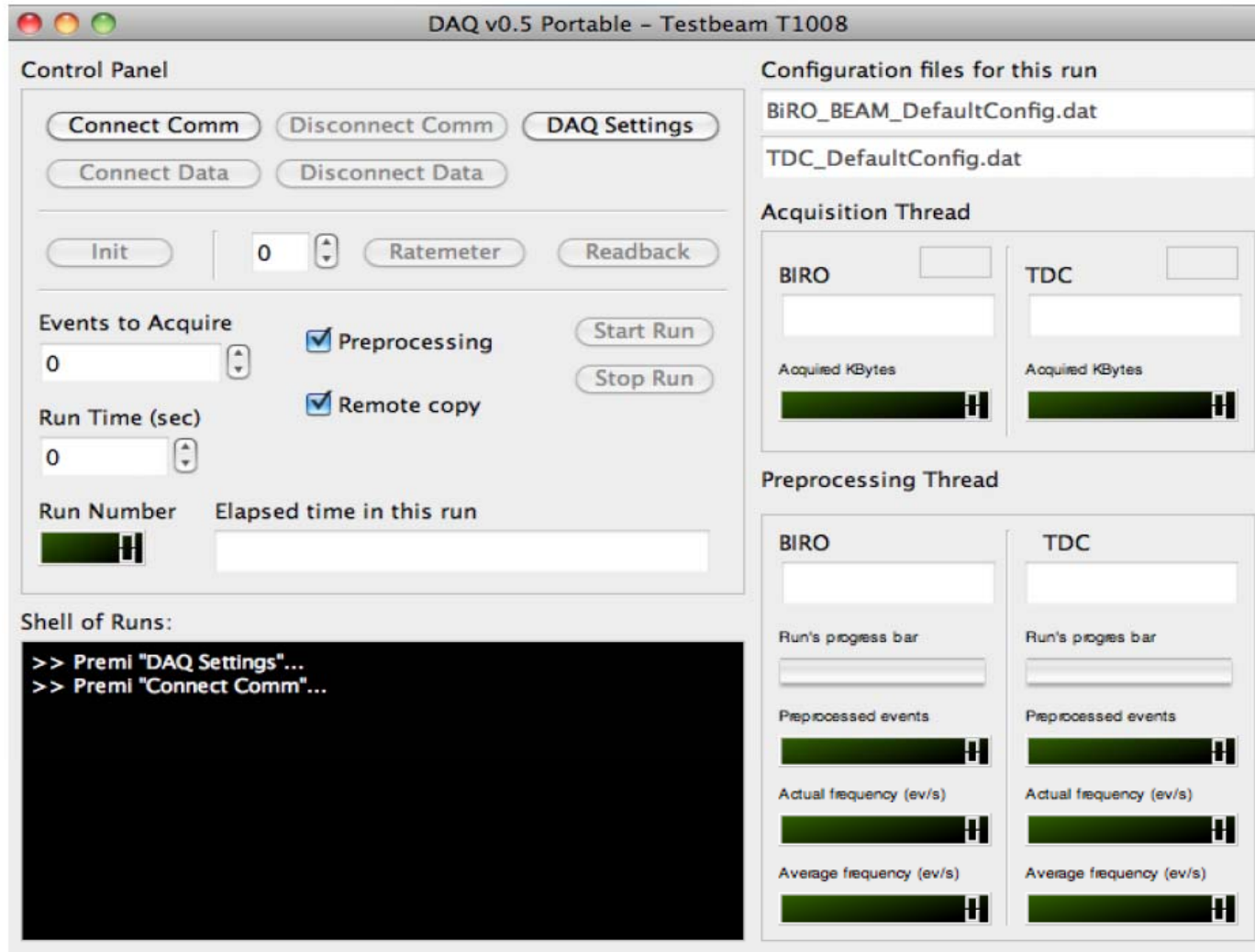
The diagram below, prepared by the main developer of the "On Line" engine, computer scientist Matteo Manzali, temporarily with INFN-Ferrara, shows how the IFR FE BiRO TLU and the TDC subsystem interact with the "On Line" system, which includes the DAQ, the ODC and the on-line monitoring modules.



SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system

Beam test "On Line" software features:

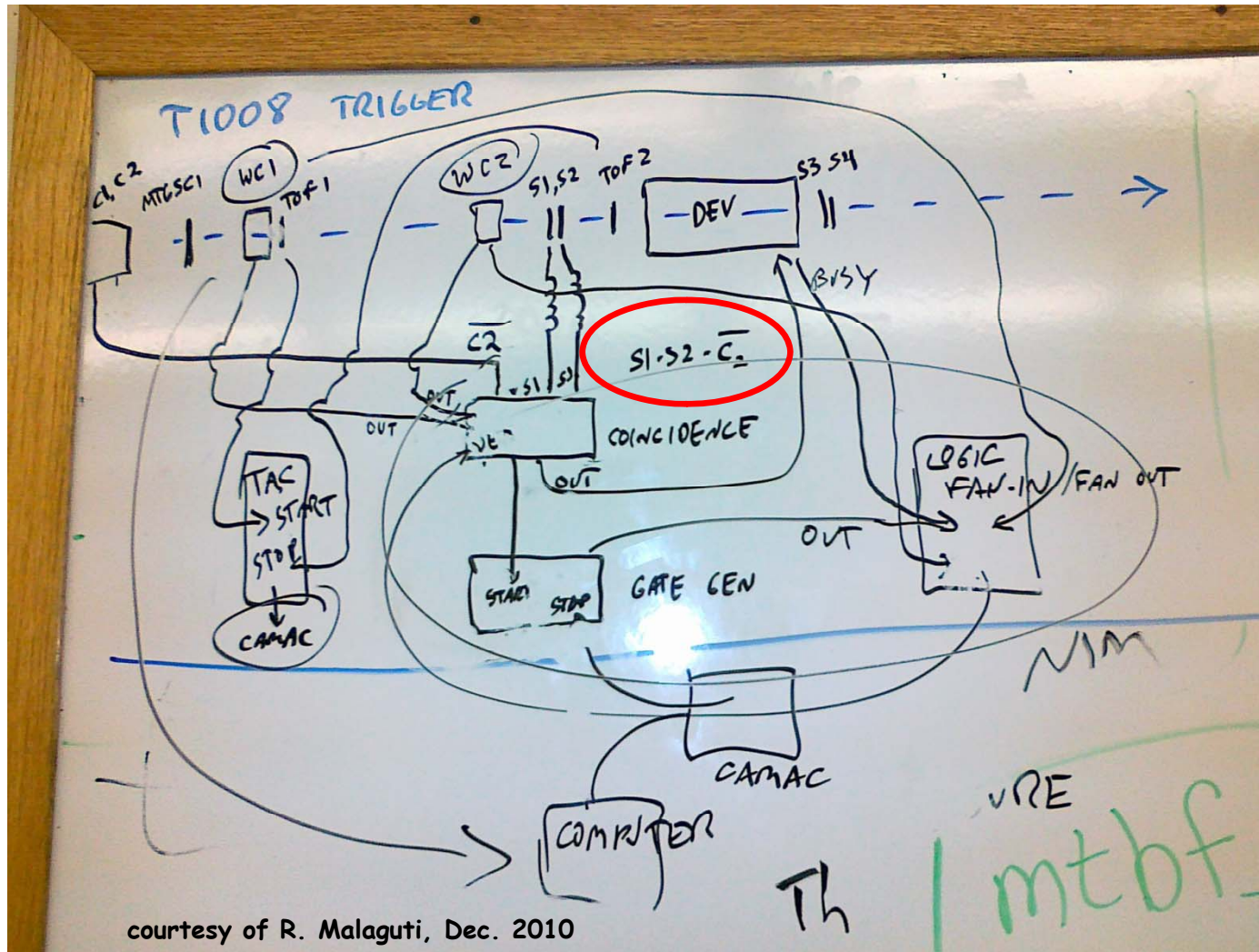
The QT based, graphical user interface of the "On Line" software engine



courtesy of M. Manzali, Dec. 2010

SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system

Beam test "On Line" software features: The beam test trigger logic:



Legenda:

C1, C2: signals from the differential Cherenkov detector.

C2 was used as an electron veto.

S1 through S4: trigger scintillators

TOF1, TOF2: time of flight detector

WC1, WC2: wire chambers

Circled in the picture is the basic trigger condition:

S1 & S2 & /C2

SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system
Preliminary beam test results

Reference talk:

FIRST RESULTS FROM BEAM TEST
G. Cibinetto, E. Feltresi, N. Gagliardi, M. Munerato

presented at this meeting by Mauro Munerato, University of Ferrara



SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system
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FIRST RESULTS FROM
BEAM TEST

G. Cibinetto, E. Feltresi, N. Gagliardi, M.M



XV SuperB General Meeting - Caltech

A reminder:

Layer 0 = the first one hit by beam particles

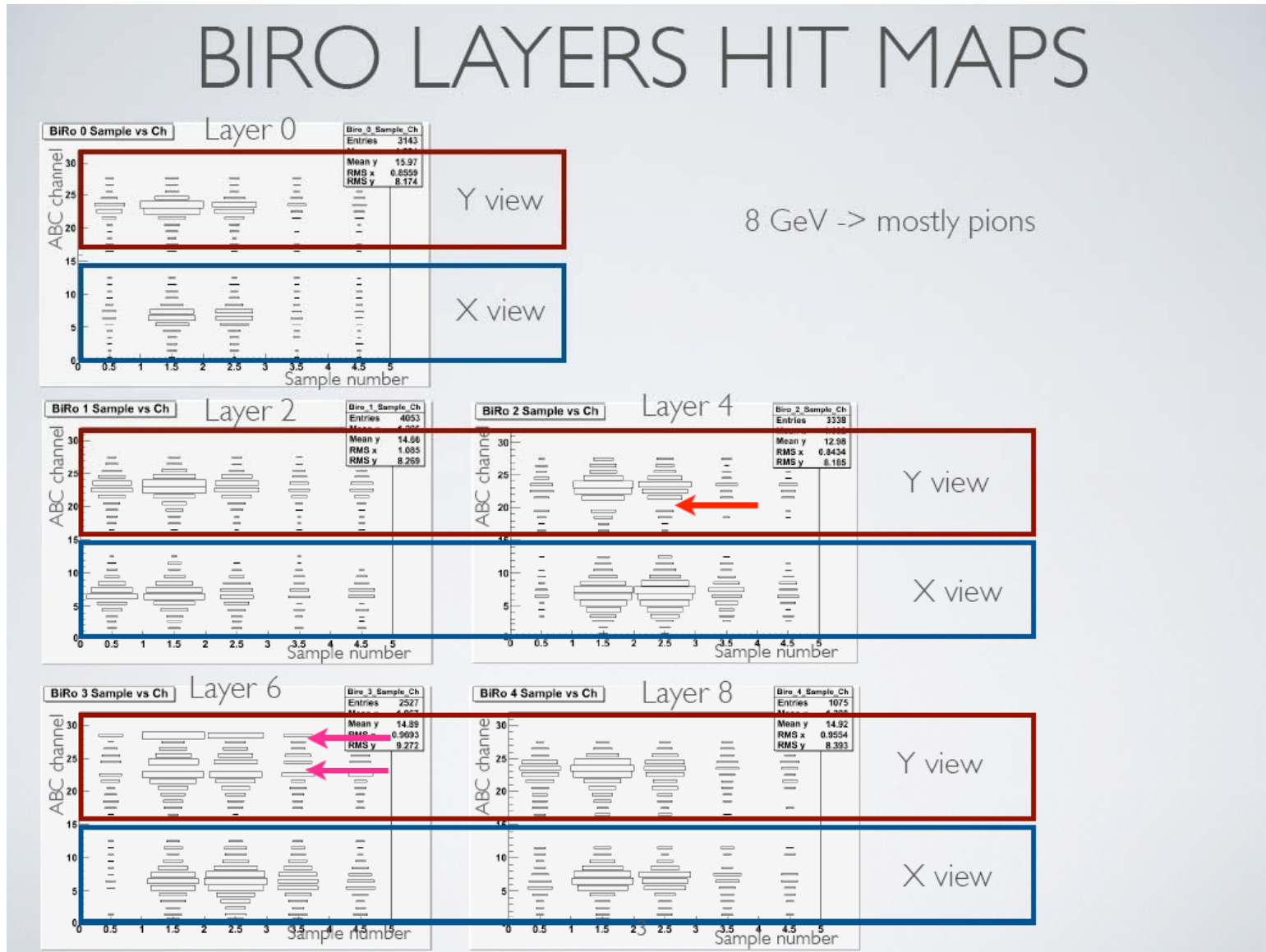
Layer 0, 2, 4, 6, 8 are equipped with double layered X-Y planes, each layer 1cm thick. Each bar in these layers is read only at one side.

These planes are only read out in "binary" mode

Layer 1,3, 5, 7 are equipped with single layer planes, 2 cm thick. For these layers all the bars are read from both sides

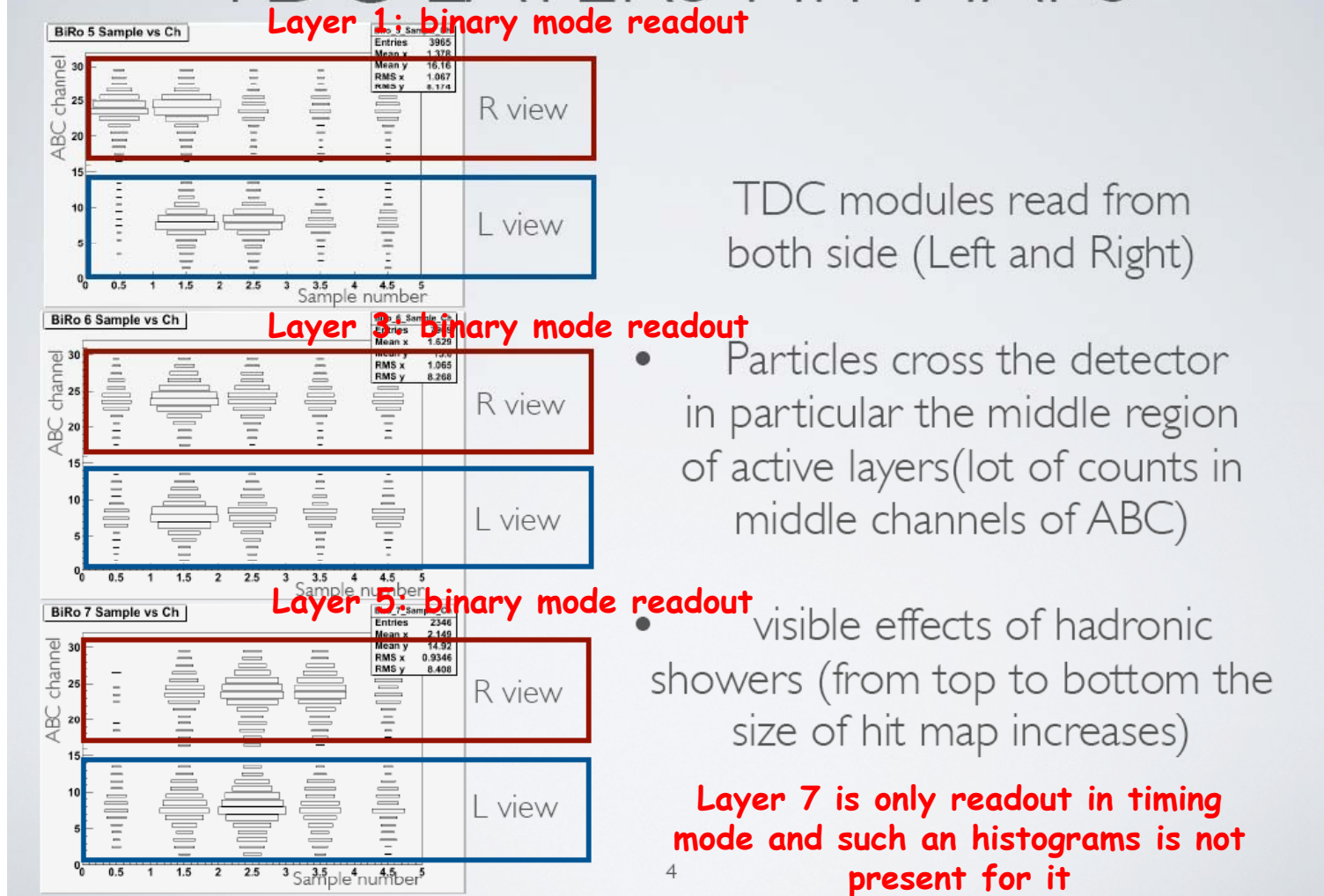
These planes are read out in "timing" mode and 3 out of 4 are also read out in "binary" mode

SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system
 Preliminary beam test results



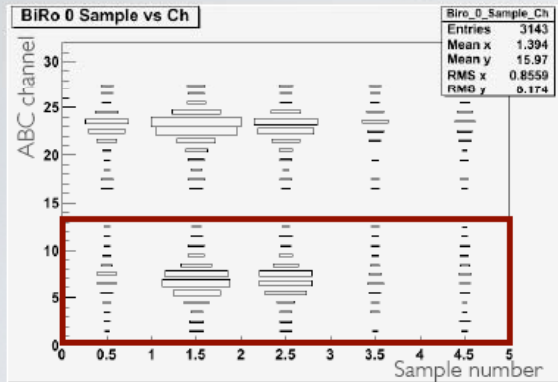
SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system
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TDC LAYERS HIT MAPS



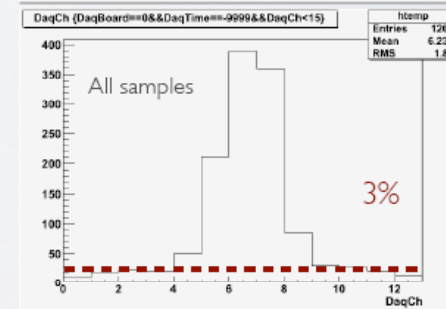
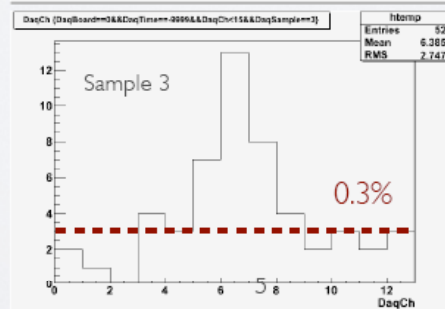
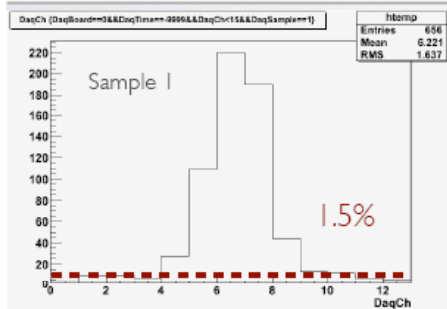
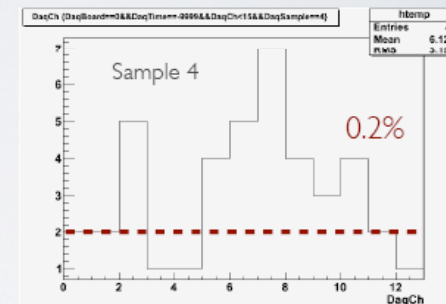
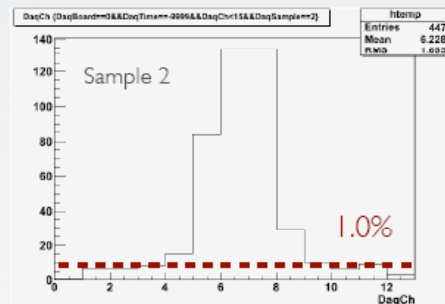
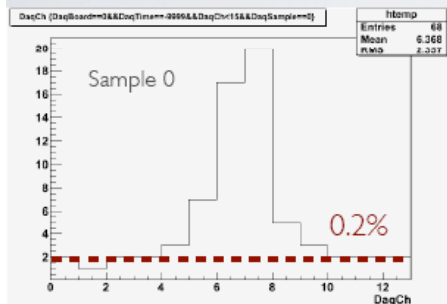
SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system
 Preliminary beam test results

OCCUPANCIES



Thr 8.5pe

Low occupancy for "out of time" time-slots \leftrightarrow low noise



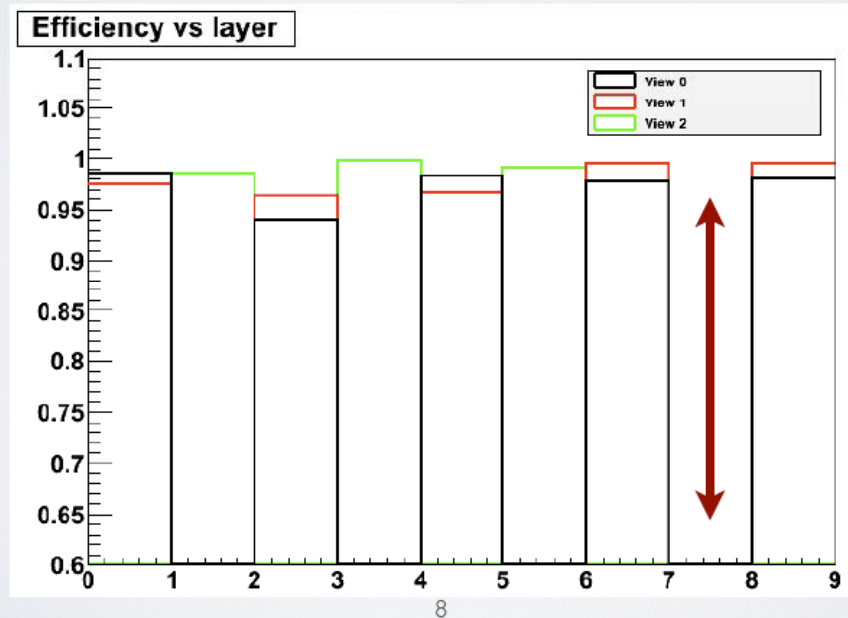
SuperB IFR electronics : Beam test of the IFR prototype electronics and DAQ system

Preliminary beam test results

Preliminary

EFFICIENCY

- Efficiencies can be calculated using muon events, pions events or mixed events, the results shouldn't change much.
- To calculate efficiency we require that the particle hit both the scintillators of the prototype.



Layer 0, 2, 4, 6, 8 are equipped with double layered X-Y planes, each layer 1cm thick.

Each bar in these layers is read only at one side.

These planes are only read out in "binary" mode

Layer 1,3, 5, 7 are equipped with single layer planes, 2 cm thick. For these layers all the bars are read from both sides

These planes are read out in "timing" mode

Layer 7 is only read out in "timing" mode and do not appear in this plot.

Efficiency is higher for thicker planes, as expected.