ETD session
SVT pixels electronics

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Summary

- New pixels triggered RO architecture
- DAQ trigger handling
- Simulations for pixel efficiency evaluation in triggered mode
- Bandwidth estimation in data-push and triggered mode
- Conclusions

Triggered Architecture

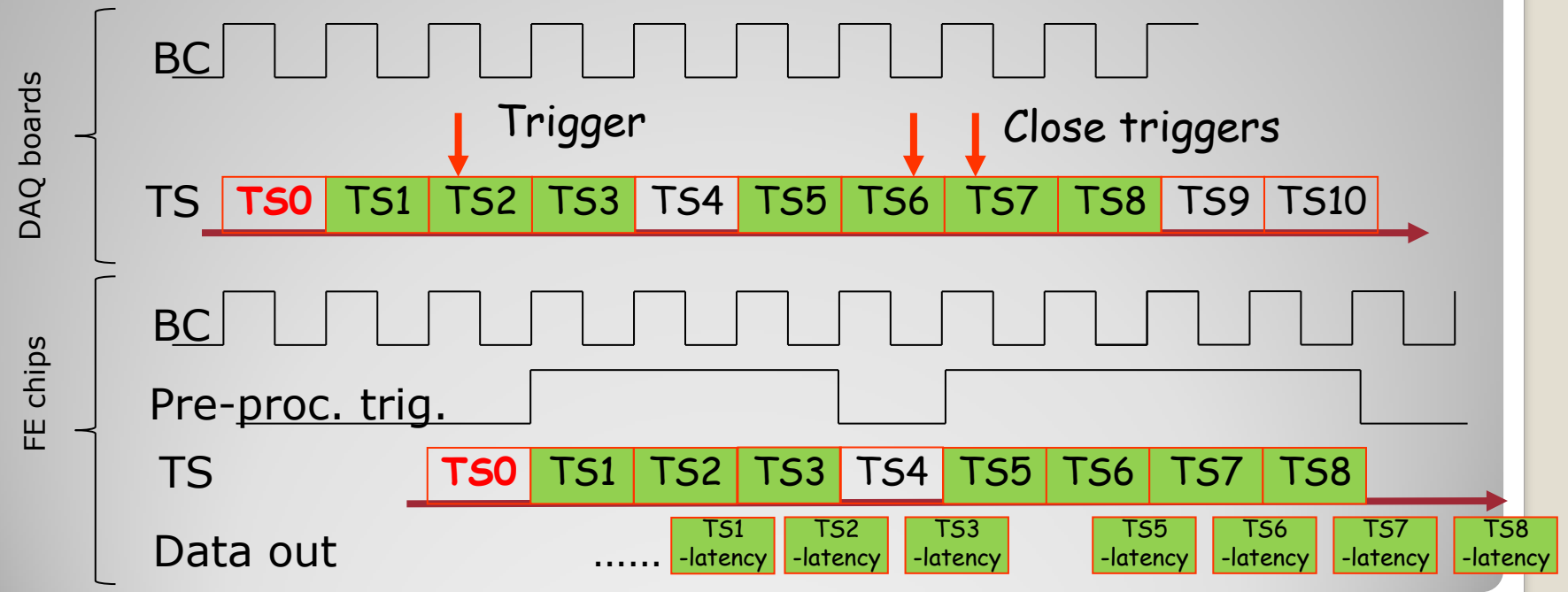
Data-push architecture for pixels on Layer0 requires a lot of output bandwidth. (100MHz/cm^2 x ~20bit = ~2 Gbps/cm^2)

Some modifications, involving the sweeper architecture only, make possible to exploit the **matrix itself as a hit buffer** for a triggered architecture.

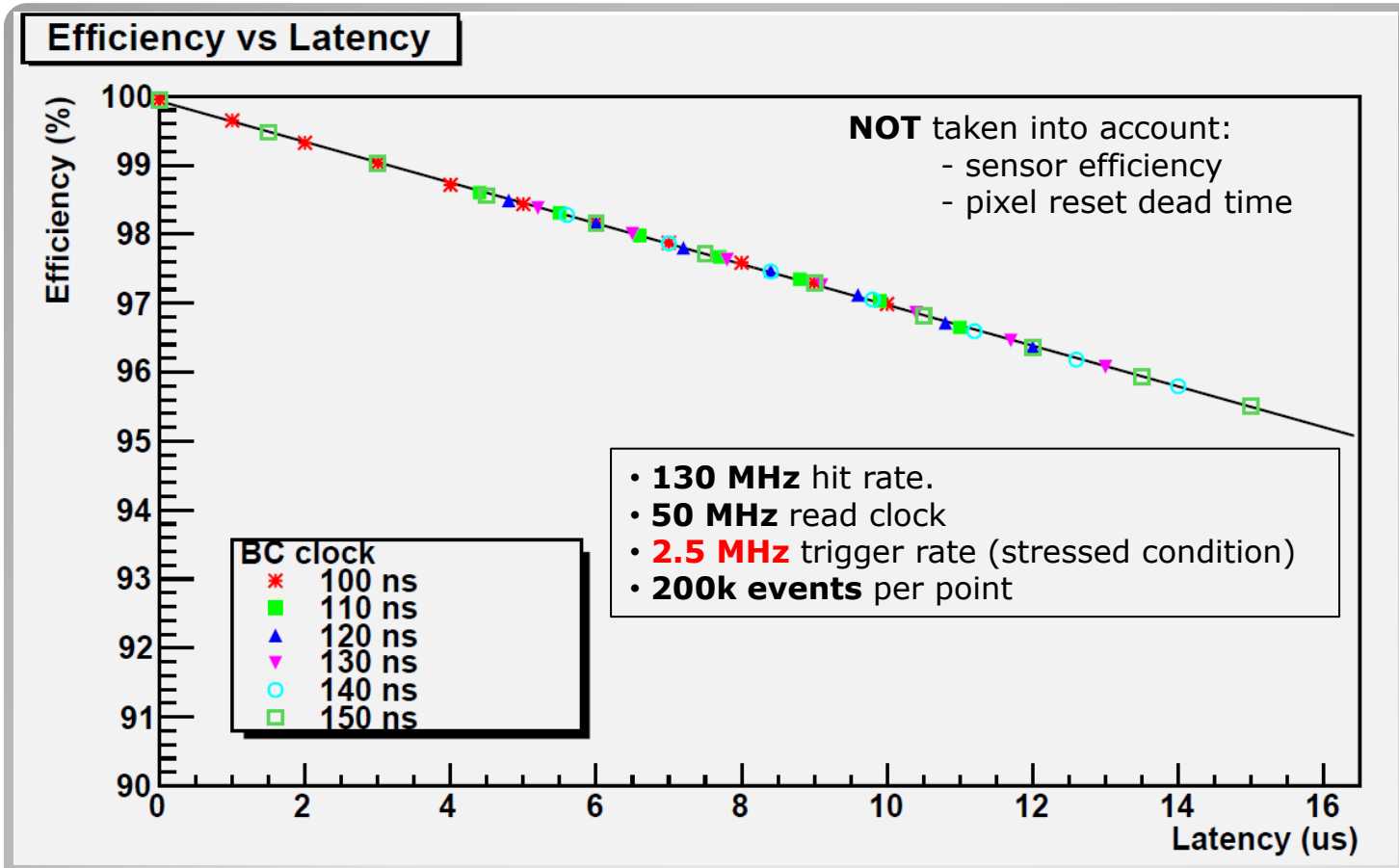
Since the pixel is the buffer element, **the longer the latency, the higher the occupancy** (→dead time).

We are evaluating **if this is solution is viable** taking into account the expected trigger latency (~6 μs) of SuperB.

- DAQ boards responsible for trigger handling
- Pre-processed trigger sent to Front-end electronics.
  - Simpler on-chip trigger logic
  - Re-configurable logic on DAQ boards
- One-wire trigger to FE chips.
- Trigger latency configured on FE chips at start-up.
- Chip trigger signal synchronous to BC clock.

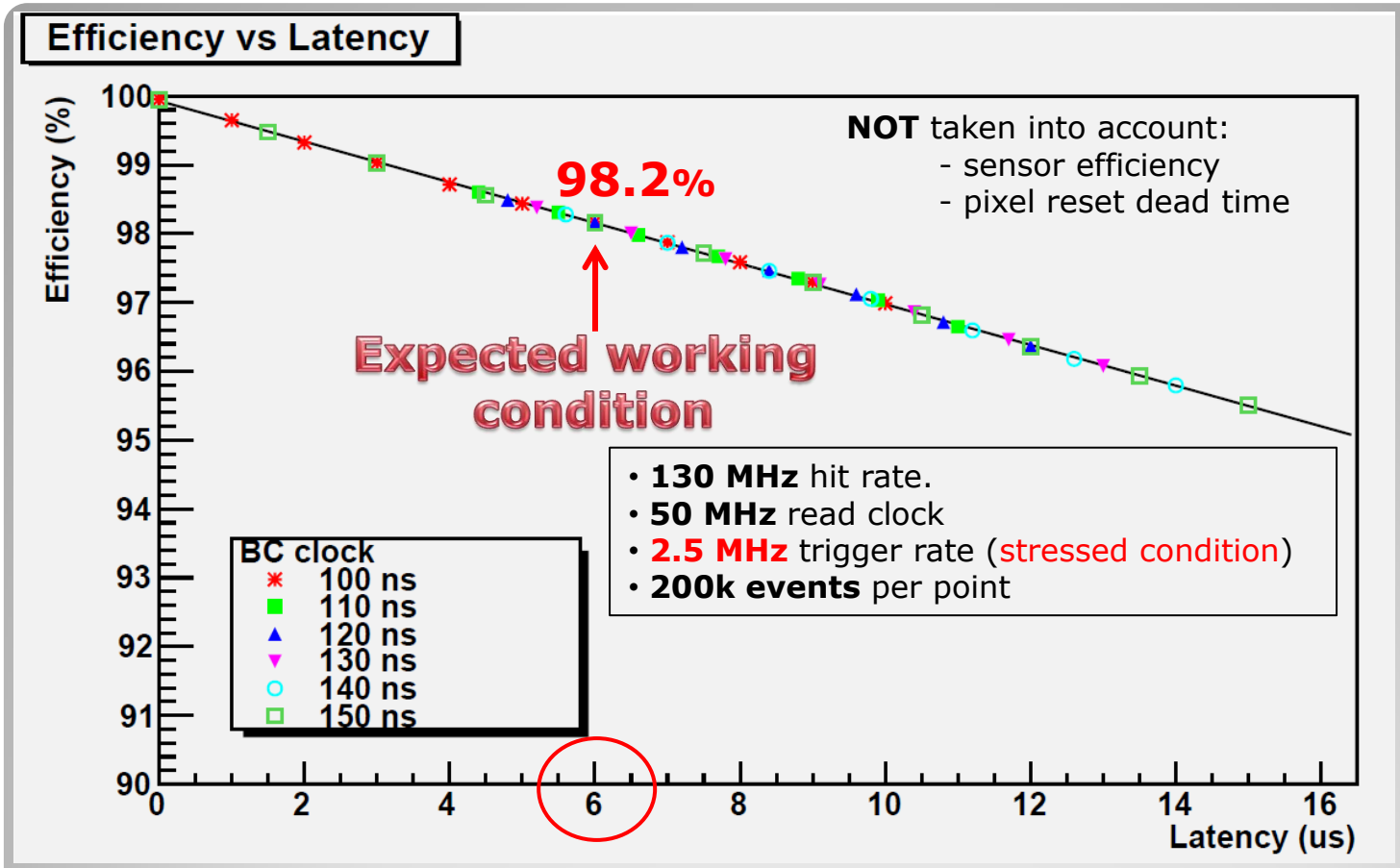


Trigger handling



- Smooth decrease of efficiency in function of trigger latency.
- Almost **no dependency** of efficiency **on BC period** (in this region)
- Linear fit slope: **-0.3 %/us**.

Simulation results: TRIGGERED



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Simulation results: BANDWIDTH

Bandwidth usage estimated by simulations

data bus: 20 bit @ 200 MHz bus → 4 Gbps max throughput.

- ***Data push mode***
  - BC = 100 ns (10 MHz)
  - Rate = 100 MHz/cm^2

mean bandwidth usage of **2.6 Gbps**

~22% bandwidth saving thanks to zone clusterization algorithm and time bundling of hits. (respect to standard *xyt* hit word encoding, taking into account cluster spread distribution from physics simulations (by R.Cenci)).

- ***Triggered mode***
  - BC = 100 ns (10 MHz)
  - Rate = 100 MHz/cm^2
  - Trigger Rate = 2.5 MHz (largely overestimated, 1 trig. every 4 BCs)

mean bandwidth usage of **650 Mbps**

(corresponding to ~40 Mbps for a standard 150 kHz trigger rate).

Conclusions

- Pixel triggered architecture designed and simulated.
- Trigger for pixel detectors must be pre-processed by the acquisition boards
- 98.2 % readout efficiency evaluated by simulations at 6 us of trigger latency.
- Bandwidth estimated about 40 Mbps at 150 kHz of trigger rate.