

# *DCH FEE STATUS*

*Level 1 Triggered Data Flow FEE Implementation*

*&*

*28 chs chamber prototype FEE for CC study*

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- *DCH TRIGGERED DATA FLOW – STANDARD RO (NO – CC)*
  - *Trigger & OL Specs (reminds)*
  - *ADB main blocks & data frame (remind)*
  - *FE readout architecture*
  - *Single channel multi-events and single event readout simulation*
- *Cluster Counting with the local derivative method*
  - *Circuit block diagram & digitized output samples*
- *Chamber prototype front-end for Cluster Counting & standard RO*
- *Conclusions*



## Specs

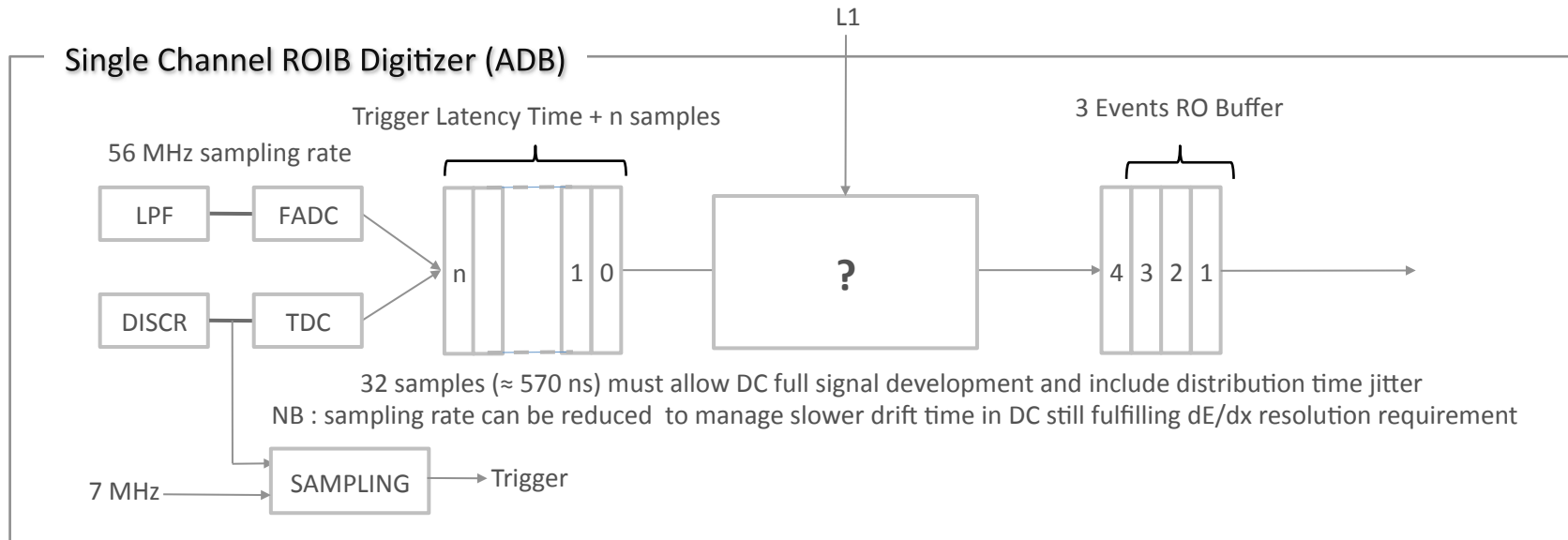
### System

- Trigger rate (average): **150 kHz**
- Trigger (fixed) latency :  $\approx 6 \mu s$
- Data OL BW : **16 OL @ 2 Gbits/sec**
- ECS OL BW : **16 OL @ 2 Gbits/sec**
- Trigger OL BW : **64 OL @ 1.2 Gbit/sec**
- Trigger spacing (min) > **36 ns** (*sampling frequency = 56 MHz*)
- *Trigger burst : 4 events (check other sub-detector ..)*

### Detector

- Number of cells (guess):  $\approx 9216$
- Chamber occupancy : **15%** (Inner layers)
- Chamber gain :  $5 \cdot 10^4 - 1 \cdot 10^5$
- Sense wire parasitic ( $C_D$ )  $\approx 25 pF$

# ADB main blocks & data frame (remind)

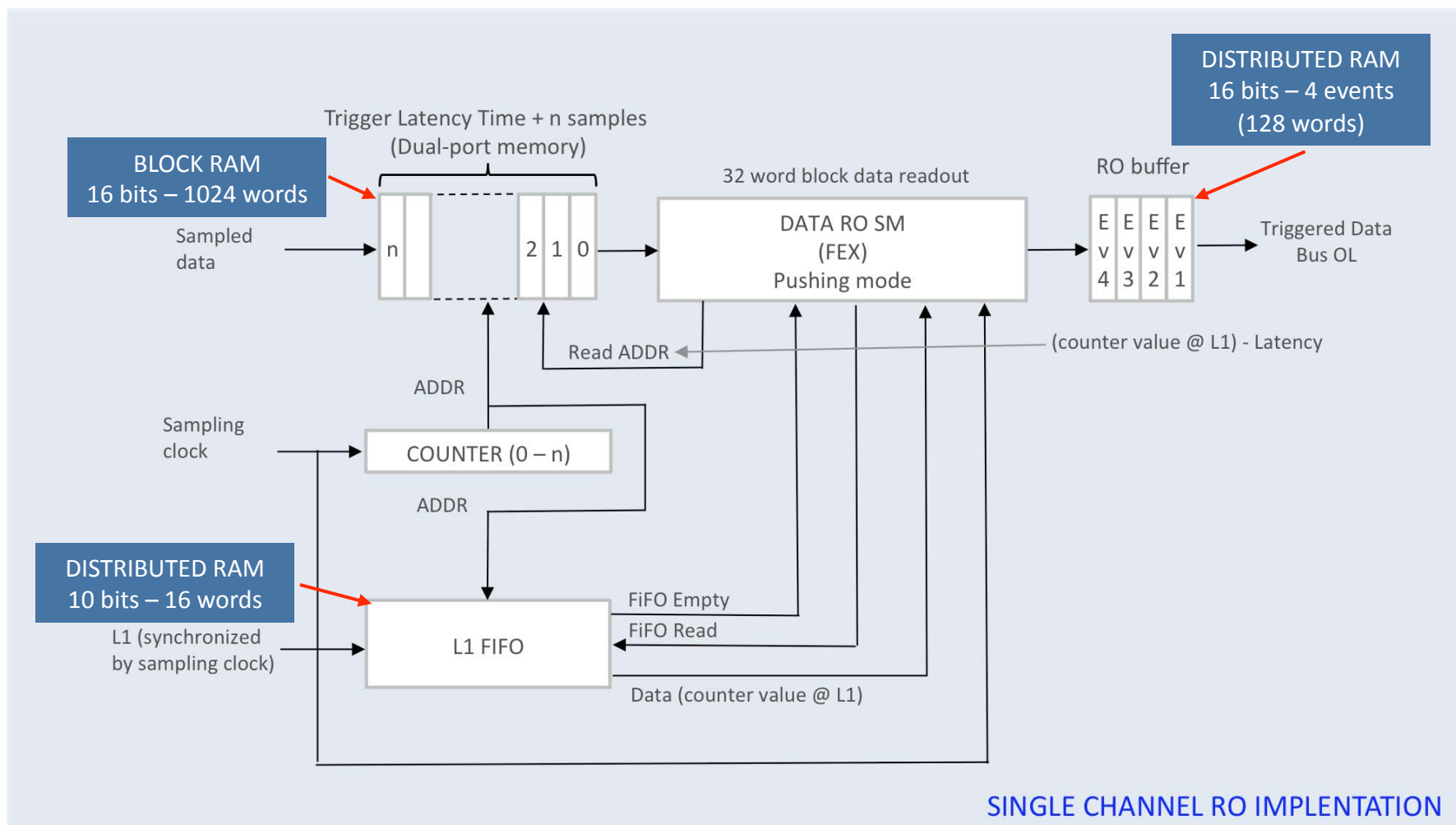


## Digitized Data Frame Example

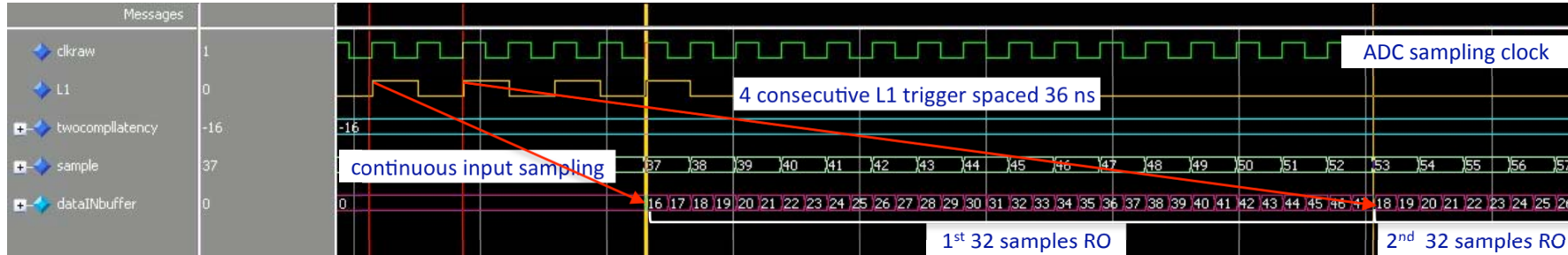
A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	T	A	A	A	T	A	A	A	A	A	A	
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	
C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	
#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	#	
3	3	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	#	#	#	#	#	#	#	#	#	#	#	
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	2	9	8	7	1	5	4	3	2	1	0

Position inside the frame  $\rightarrow$  coarse time measurement (5 bits)  
 Content  $\rightarrow$  fine time measurement (6 bits)

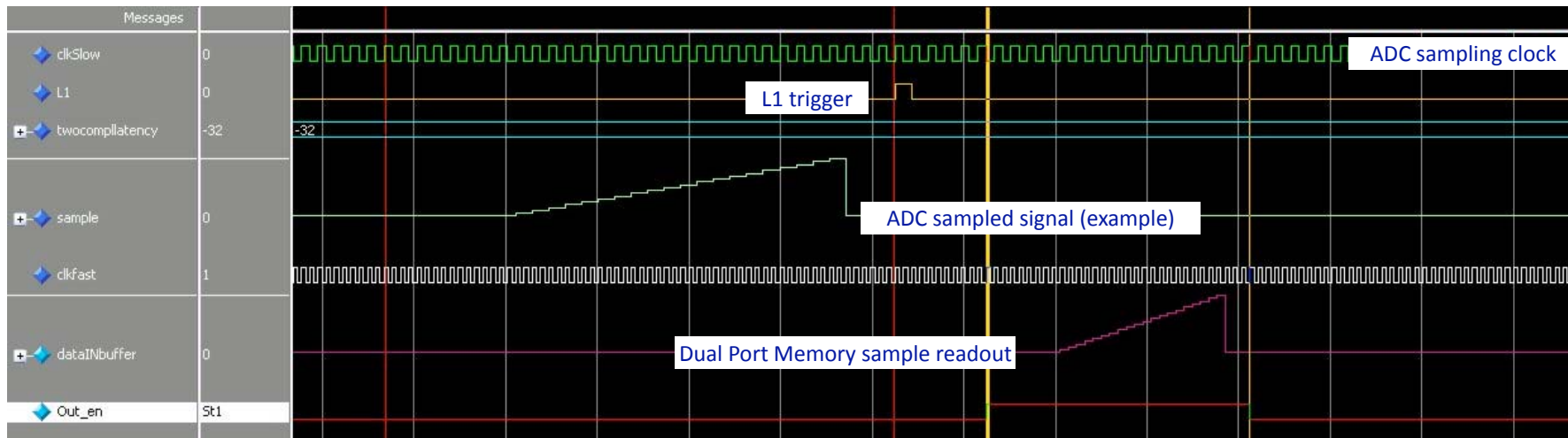
→ implemented and simulated on a SPARTAN 6 device (XC6SLX150T-FGG900) ←



➔ 4 L1 events spaced 36 ns (sampling CLK = 58 MHz – Memory RO CLK = 116 MHz) ←

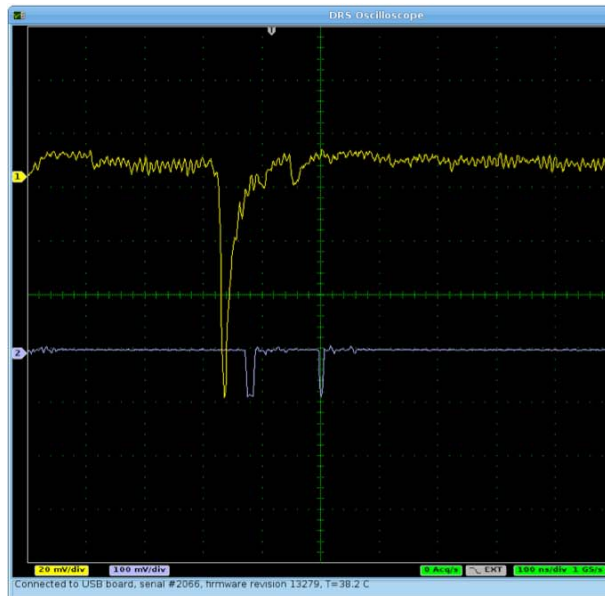
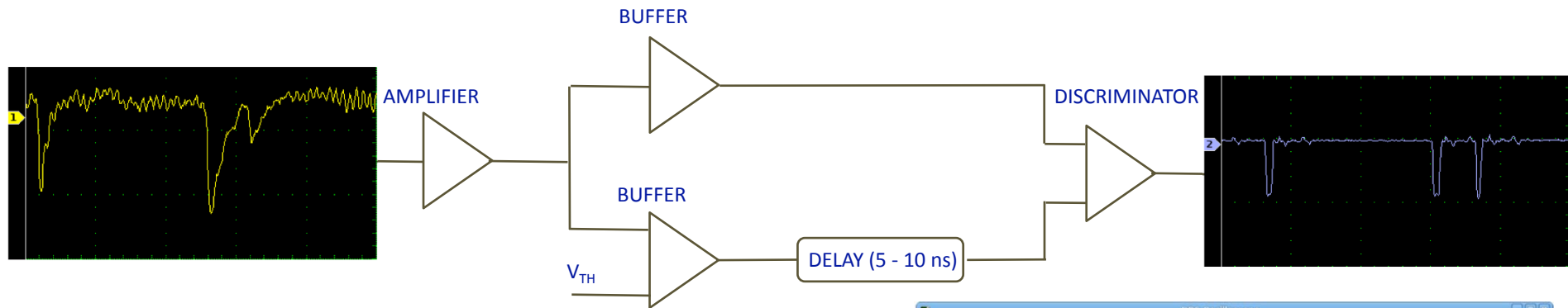


➔ Single event acquired @ 58 MHz and read @ 116 MHz ←

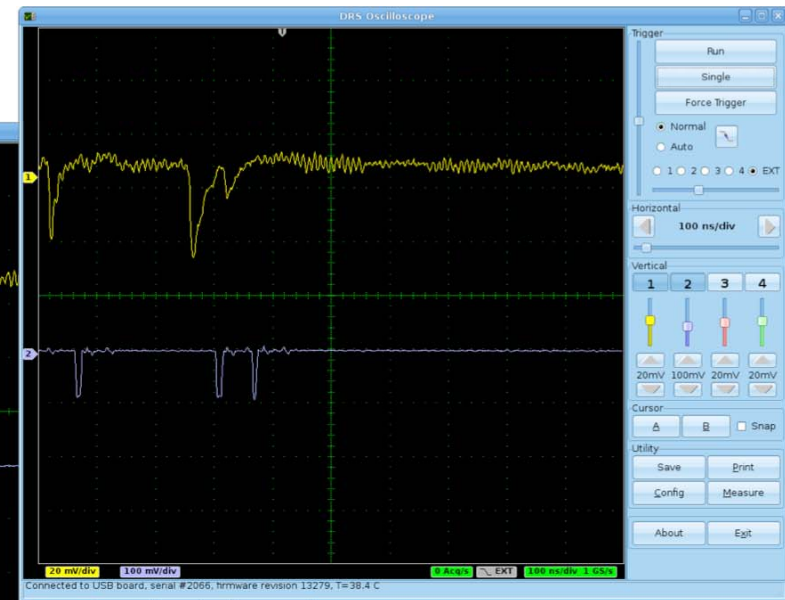




## *Cluster Counting with the local derivative method*



V<sub>TH</sub> close to the system noise limit



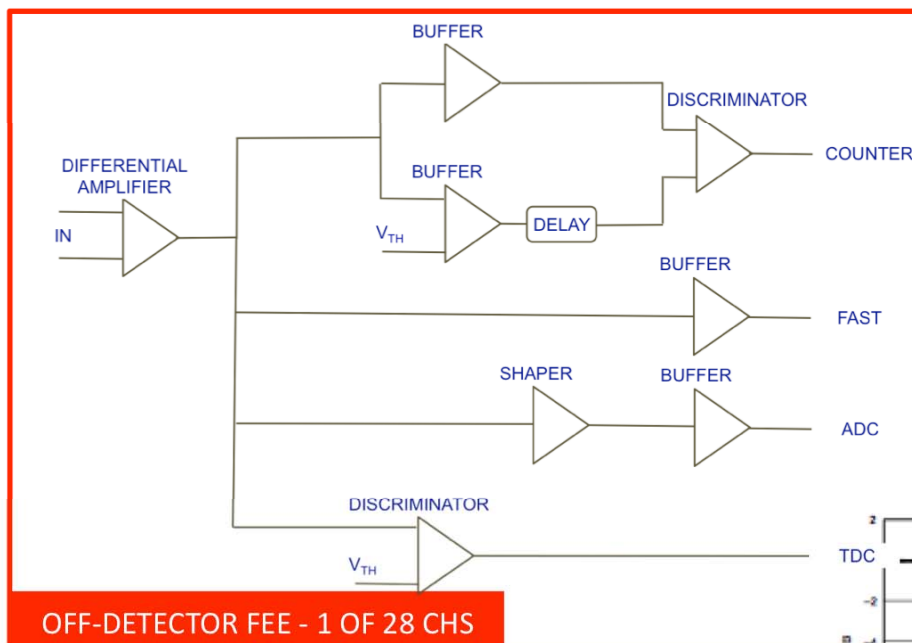
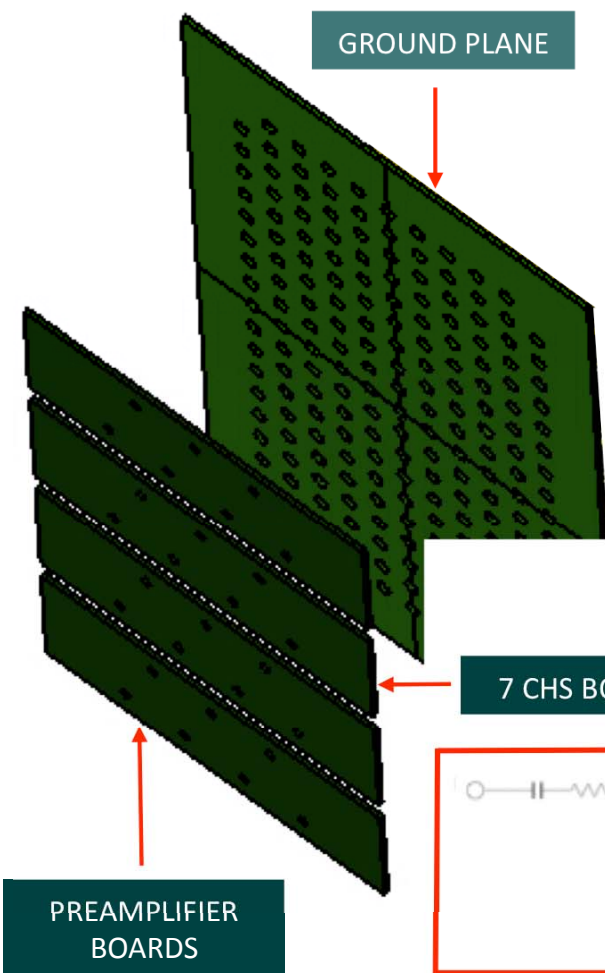
COLLATED IRON SOURCE



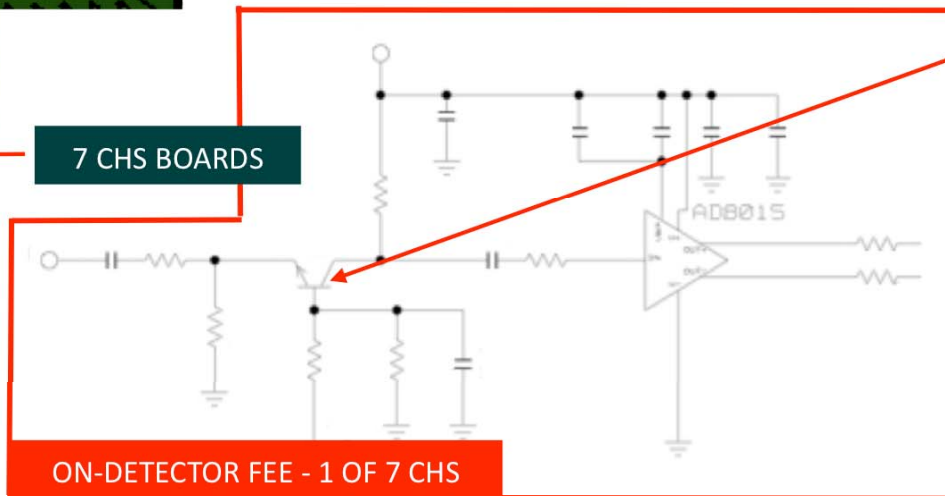


*Chamber prototype front-end for Cluster Counting  
& standard RO*

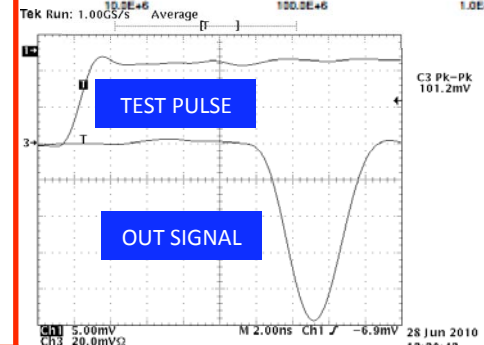
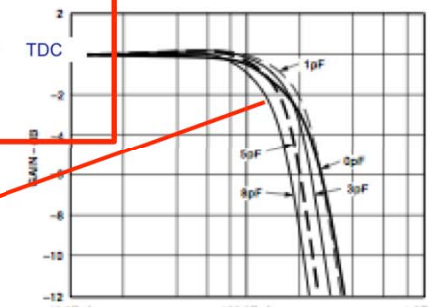
28 chs chamber proto - ON & OFF detector electronics



OFF-DETECTOR FEE - 1 OF 28 CHS



ON-DETECTOR FEE - 1 OF 7 CHS





- We have started FE readout architecture simulation (as planned in the previous WS). A single readout channel has been implemented on a SPARTAN 6 device and fully simulated for consecutive triggers spaced 36 ns (up to 4 triggers). An example of (a very simple) reconstructed waveform has been also shown.

### SIMULATION NEXT STEP

- FEX implementation for a single channel
  - Two continuous cathode single channel detectors (.4 and 2.7 mt length) instrumented with local derivative method have been set up and preliminary results (for the 2.7 mt detector) have been shown.
  - 28 chs chamber prototype front-end design has been started. Front-end will be split in two sections. The first one (on-detector) will be based on a wide band transimpedance preamplifier, while the second one (off-detector electronics) will include local derivative circuit and outputs for ADC/TDC and as well.