ALCOR for EIC

some background information
and feedback from user perspective

P. Antonioli, D. Falchieri, R. Preghenella
INFN - Bologna

Introduction

put together designers & users given:

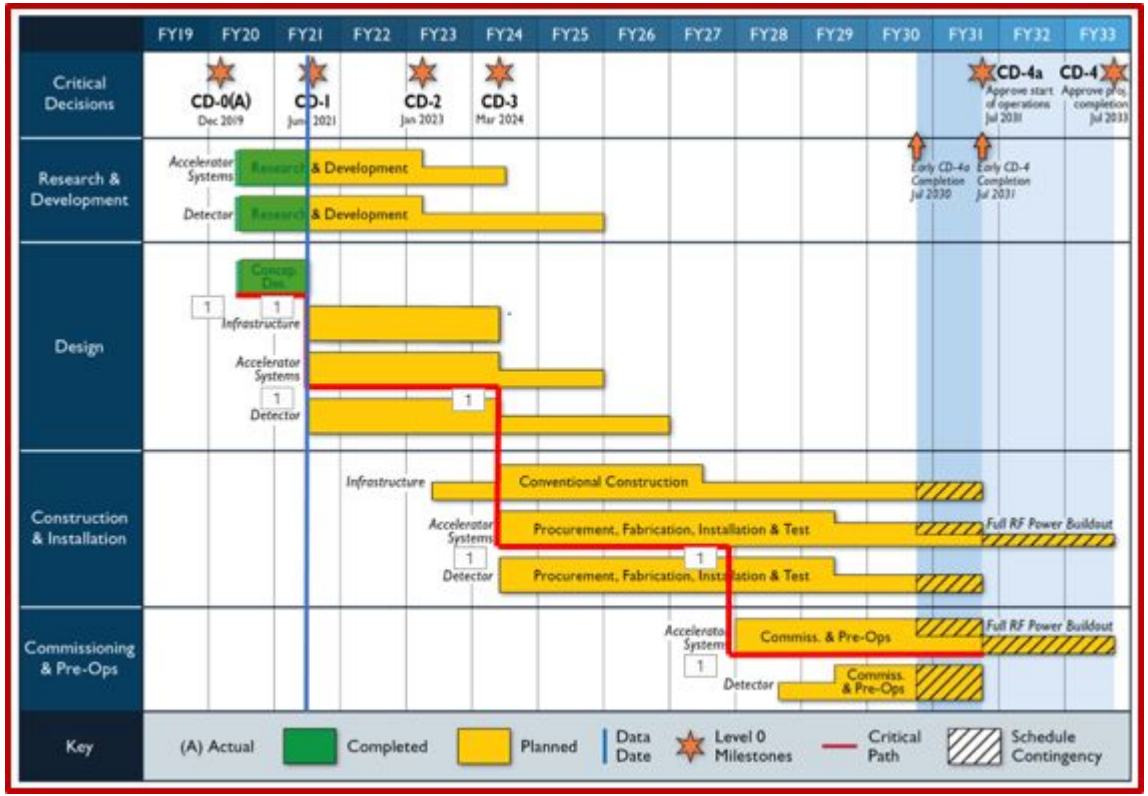
- last 18 months collaborative work (ALCOR on beams, ALCOR to characterize SiPM in the lab)
- “users” feedback toward ALCOR 4 EIC requirements/wishlist
- more info on EIC schedule → share timeline info
- share ideas on potential final setup
- be realistic on what we can achieve, but formulate “ask”

Status of project / timeline

R&D 2022-2024 but with some “space” in 2025/2026

construction to be completed by end of 2029

“detector in” (dRICH) Q1 2030



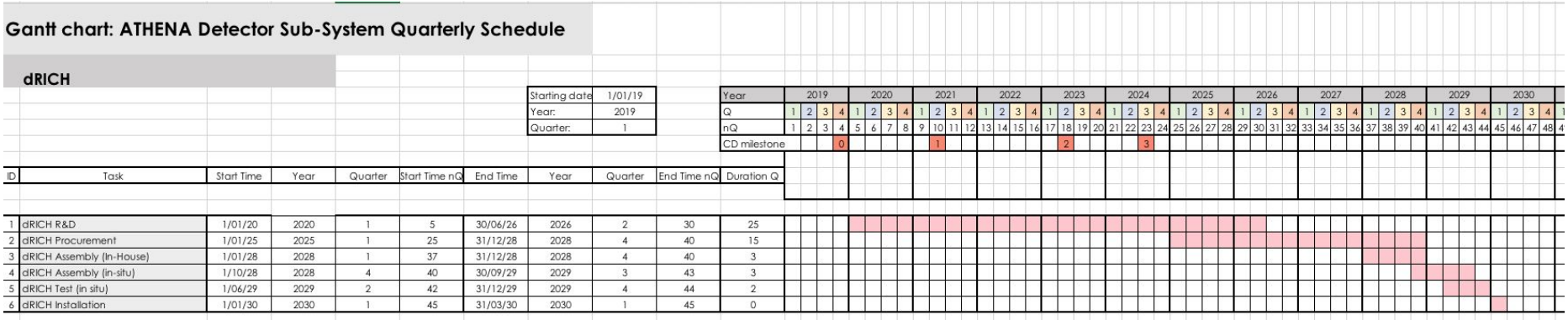
Potential dRICH timeline

Gantt chart: ATHENA Detector Sub-System Quarterly Schedule

dRICH

Starting date	1/01/19
Year:	2019
Quarter:	1

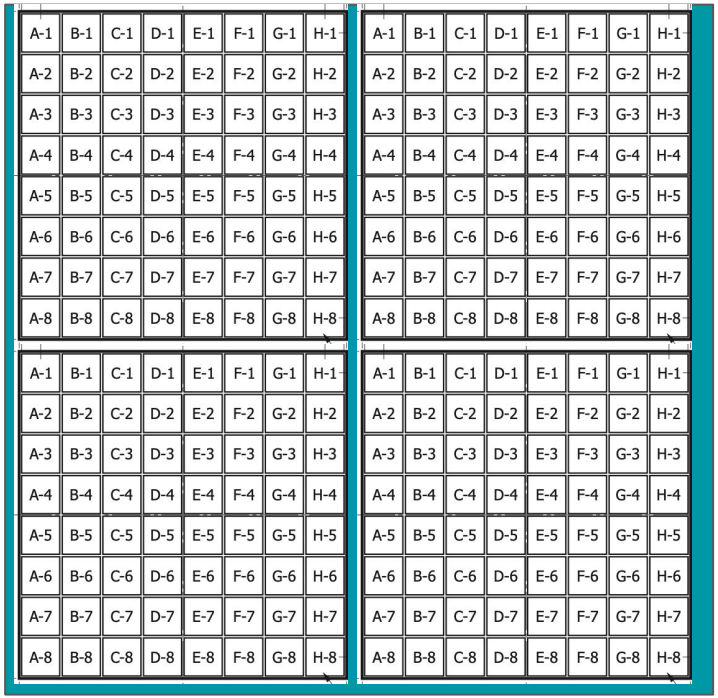
ID	Task	Start Time	Year	Quarter	Start Time nQ	End Time	Year	Quarter	End Time nQ	Duration Q
1	dRICH R&D	1/01/20	2020	1	5	30/06/26	2026	2	30	25
2	dRICH Procurement	1/01/25	2025	1	25	31/12/28	2028	4	40	15
3	dRICH Assembly (In-House)	1/01/28	2028	1	37	31/12/28	2028	4	40	3
4	dRICH Assembly (in-situ)	1/10/28	2028	4	40	30/09/29	2029	3	43	3
5	dRICH Test (in situ)	1/06/29	2029	2	42	31/12/29	2029	4	44	2
6	dRICH Installation	1/01/30	2030	1	45	31/03/30	2030	1	45	0



- some of the procurement will need to start earlier (aerogel, SiPM, ..)
- electronics might come a little bit later but ASIC for front-end critical
- by 2024/2025 we should achieve an ALCOR4EIC
- 2028 target year for electronics assembly (**dRICH tiles** + ALCOR **FEB** & **ROB**)

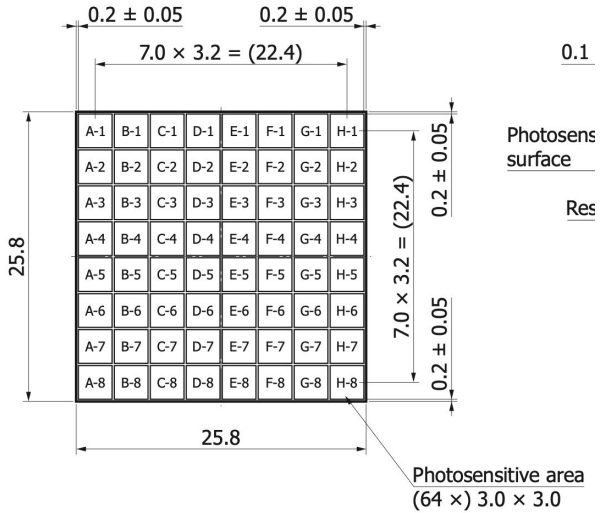
How would fit ALCOR in dRICH readout?

current scheme: caveat: used for proposal/costing not necessarily the final one. A lot of work ahead, but useful to focus on requirements



dRICH tile 5.6 x 5.6 cm^2

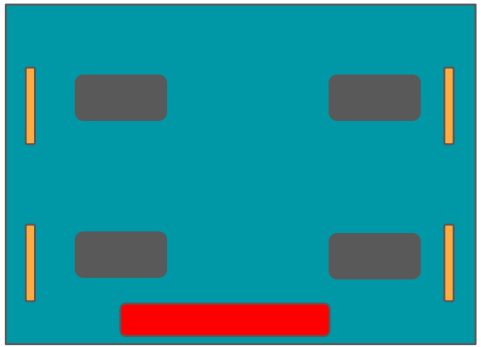
dRICH tile



dRICH FEB (front-end board)

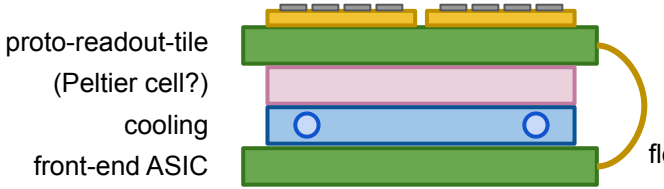
current thinking: 1 FEB serving 1 dRICH tiles

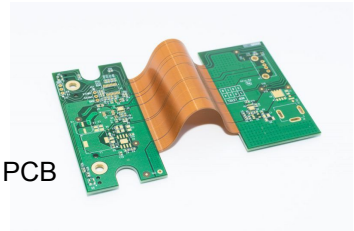
SiPM bus
readout bus + LV bus



ALCOR 64 channels

- Vbias via ALCOR? (as CITIROC) or dRICH FEB with external LV connector + routing to dRICH tile (segmentation)
- readout bus to FPGA (dRICH ROB)
- potential area for dRICH FEB: **5x5 cm^2**
- ALCOR packaging (BGA) & test



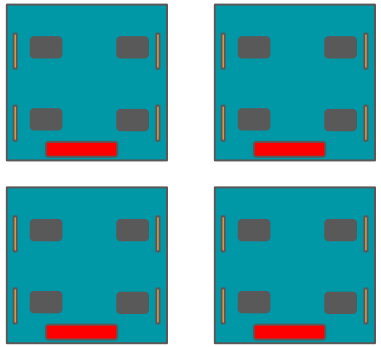


all routing of signals from ALCOR to dRICH tile to be thought hard! TSV not an option due to cooling: FlexPCB?

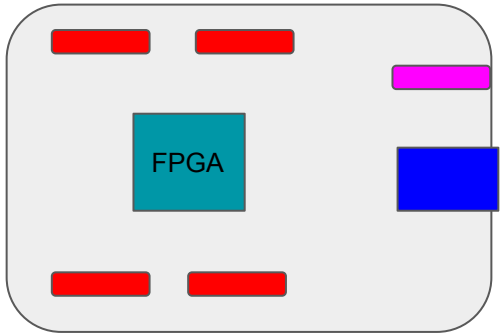
dRICH ROB (read-out board)

- based on readout/throughput considerations 4 dRICH FEB (1024 ch) should be read-out by 1 dRICH ROB (4096 channels)
- ROB acts as concentrator + data reduction (BC timing) (factor 3-5: EIC 1 BC every 9.6 ns: just get a fraction (like 2 ns of window of interest or possibly less: potential spread is 150 ps but bunch length 0.3-0.4 ns!)
- ROB potential area 10x10 cm^2

4x dRICH FEB, 16x ALCOR-64



dRICH ROB



current scheme assume ATLAS FELIX board on PC
+ lpGBT link on ROB

Using lpGBTX ASIC doesn't seem an option:
- no data reduction!
- ALCOR interface must be e-links

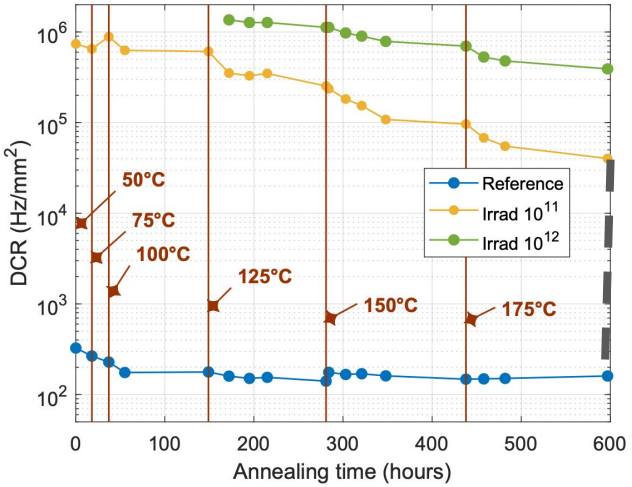
- This choice (see later) for throughput modelling keeps bandwidth on opt link to DAQ < 10 Gbps (current limitation)
- On each FEB-ROB bus expected throughput at 4 Gbps (at maximum damage from rad before annealing) if no veto on ALCOR is possible
- On each opt-link (after data reduction via timing): 5.9 Gbps (to be studied a further data reduction, if possible, via coincidences)

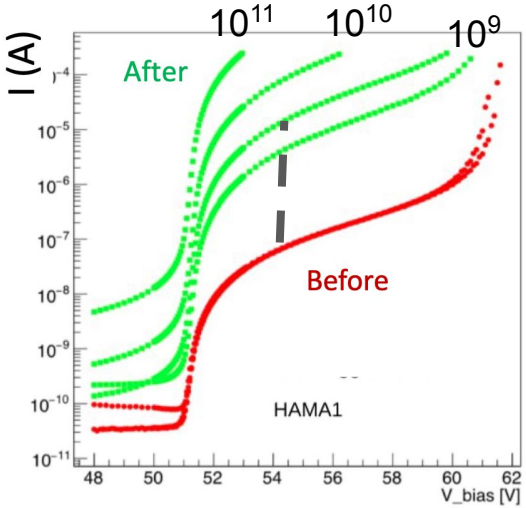
Throughput model

ALCOR hit rate (with TOT) up to 1 MHz per single channel
appears as a minimum requirement.

Key inputs:

- DCR: 300 Hz/mm^2 (Hama @ -40C)
- DCR sensor (9 mm^2): 2.7 KHz
- maximum irradiation (10^11 1 MeV-neq) + annealing penalty: 100 (Calvi et al.)
- average max tolerable DCR sensor rate: **270 KHz** (reached with some 10^9 MeV-neq… then you need to anneal!) ---> this gives already 1.8 Tbps from dRICH to DAQ (with data suppression - gated BC - by a factor 3)
- 317440 sensors





more than a factor 100 penalty in current just after 10^9 1-MeV-neq

(and indeed DCR seen growing at O(500) KHz after 10^9 1-MeV-neq)

Throughput rates and ALCOR requirements (II)

- (average) ALCOR channel: 270 kHz → 1 MHz
- 1 hit (including ToT)=64 bits
- 64 channels
- (with 1 MHz) → 2.0 Gbps/chip (current maximum)

Assuming average 270 kHz and TOT:

- 4.4 Gbps/FEB
- 18.6 Gbps/ROB ---> data reduction (BC) by a factor 3-5 (**veto signal on ALCOR?**)

Numerology:

- 4960 ALCOR (dRICH) + 75% (pfRICH)
- 1240 FEB (dRICH) + 75% (pfRICH)
- 310 ROB (dRICH) + 75% (pfRICH)
- O(10000) ALCOR [assuming 64 channels]

ALCOR & power consumptions & temperature

- Assumed 1.1 W/32 ch → 35 mW ch
- FEB → 8.9W
- ROB → (1 FPGA, 1 opt. trans. (likely VTRx), drivers) → 1A@3.3V
- dRICH total power: 12-15 KW
- moving to 64 channels will we gain something?
- Important for cooling design (aiming for -40/-50C for dRICH tile)
- operating temperature? (see dependency on temperature)
- max. temperature? (for annealing) (assuming FEB off during annealing on SiPM)

Operation with various SiPM

- nice if ALCOR works well with a large range of SiPM
  - different manufacturers, micro-cell size and capacity
  - for EIC we might eventually want to have ASIC optimised to chosen SiPM
    - but we do not know which SiPM is best to be used yet
    - best if ALCORv2 can function with large spectrum of SiPM
- SiPM-ASIC coupling
  - AC or DC
- analog part / amplification stage
  - gain should be sufficiently high
    - to work also with rad.tolerant SiPM with lower gain ~ 3 10^5
    - discriminator capable of setting a low threshold with ease (not trivial with ALCORv1)
  - low noise from the amplifier, compatible with the smaller expected signals
    - noticed that when working at low T noise figure is much better
  - baseline oscillations if FE not properly configured
    - how can avoid that?
    - have handle to setup the chip at best without using oscilloscope
- digital part / is clock at 320 MHz a must? (likely the coarse counter LSB should be close to the window we want to gate data like 2 ns over 10 ns) → power?

Summary Wishlist (all with question marks)

1. V2 fix l'incriccamento + correzioni nel fine colonna (header non mandati quando si leggono status, cambiare interfaccia SPI)
2. [indip. tra V1/V2] 64 channels
   - to ease integration/reduce connections: si' con 2 ALCOR tra 32 in un BGA. R&D nel 2022
3. [V_{bias} via ALCOR] bassa priorita' non e' neanche chiaro se necessario
   a) to help segmentation and fine tuning
4. V2 global signal (gate) to activate/inhibit input to discriminator
   a) to reduce data rate, gating only the interesting window
5. OK se 1 viene realizzato: package fitting 5x5 cm^2 // 256 channels [vedi punto 2]
   a) to fit space limitation on FEB
6. (non per V2) 1 MHz hit rate / channel → probabilmente richiede passaggio da TAC a SAR per TDC
   a) to cope with some margin with the SiPM DCR
7. V2 high gain & low-noise
   a) possibly 20 dB gain over large bandwidth (~ 2 GHz)
   b) single-photon detector of SiPM with low-gain (3 10^5)
   c) AC coupling on chip
8. T specs
   a) to sustain annealing cycles on SiPM --< abswered

→ dobbiamo capire se il ToT serve o meno
→ risoluzione temporale: binning a 50 ps (LSB) e' certamente ok, 100 ps dovrebbe ancora andare bene