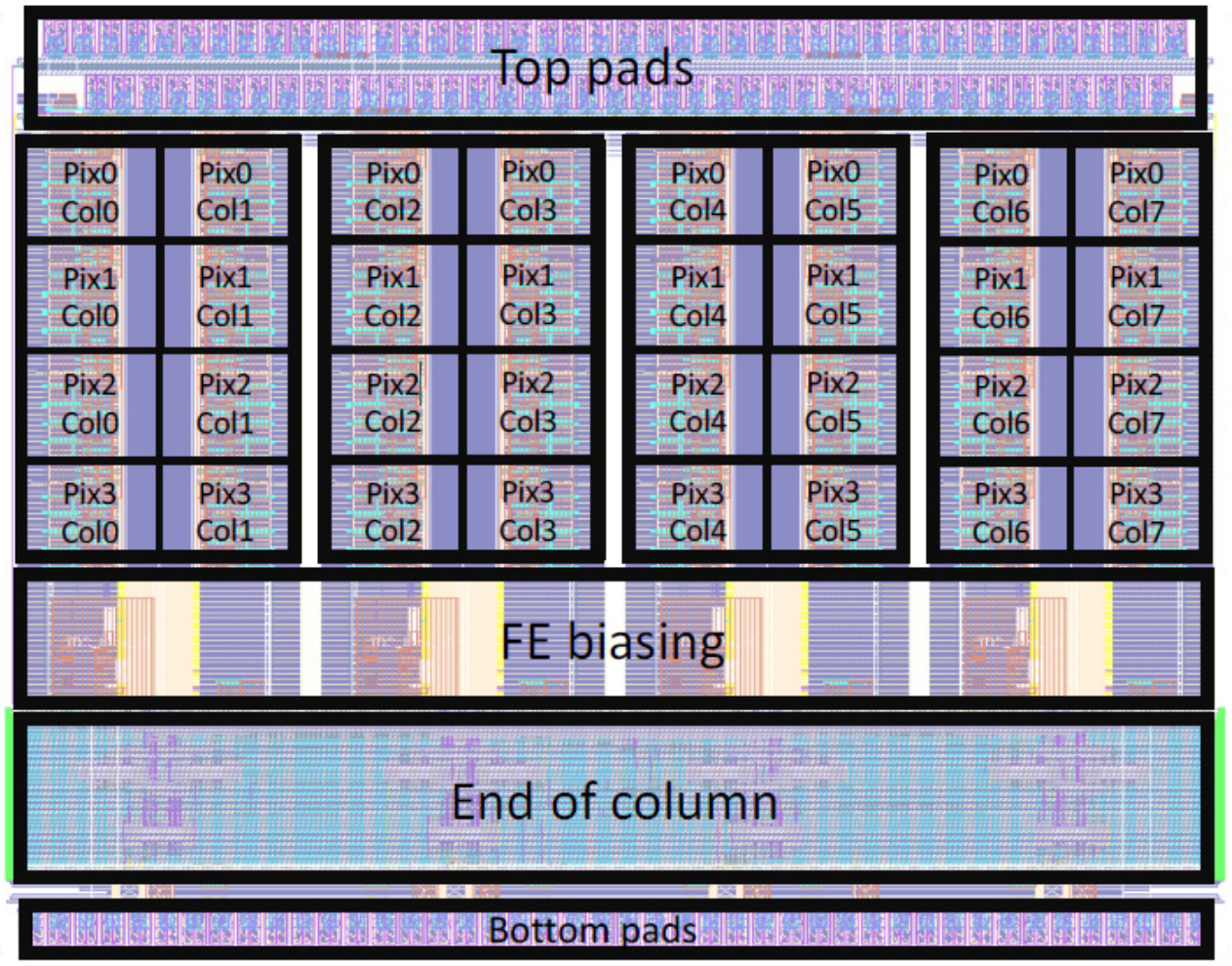
ALCOR v1

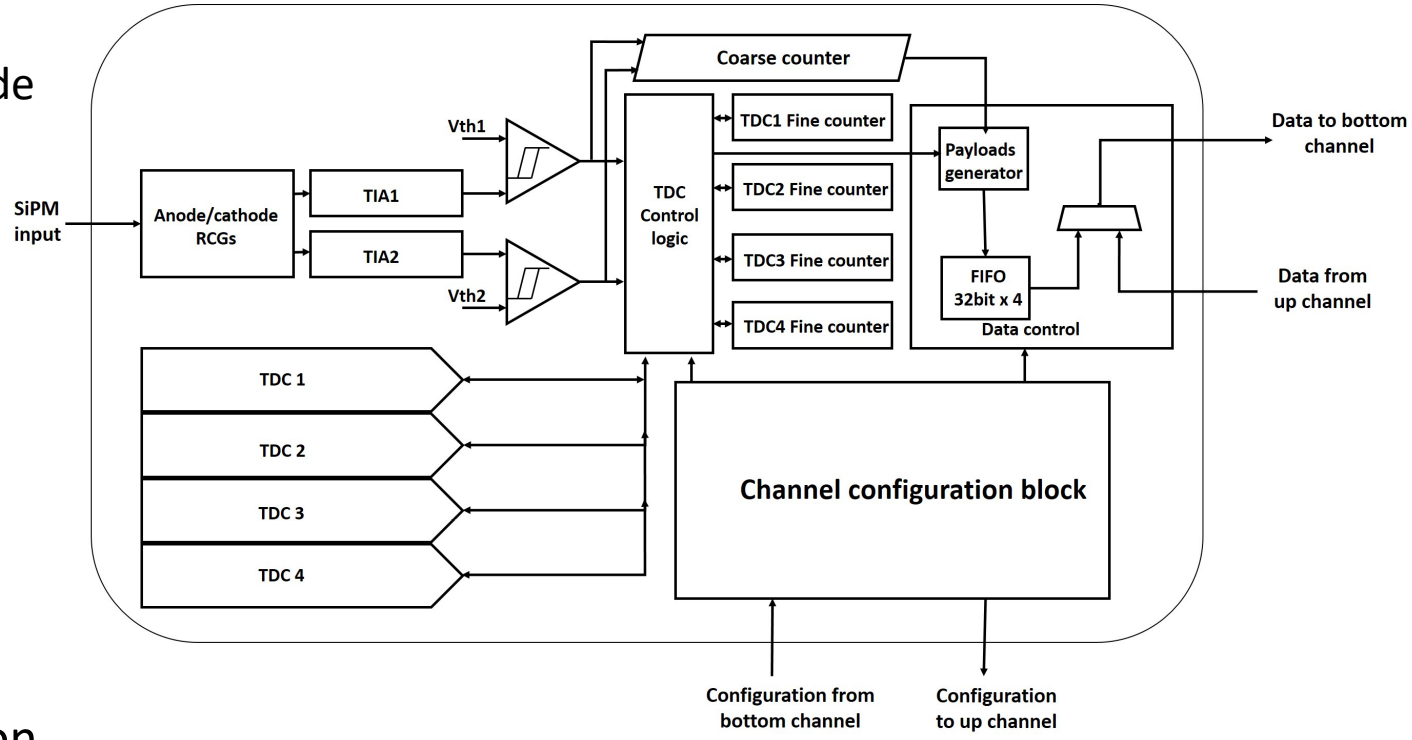
ALCOR – A Low Power Chip for Optical sensor Readout

- 32-pixel matrix mixed-signal ASIC
- 4 independent sectors (analogue bias and data transmission)
- The chip performs signal amplification and conditioning and event digitization
- Single-photon time tagging mode or time and charge measurement (Time-over-Threshold)
- Fully digital output (4 LVDS TX data links)



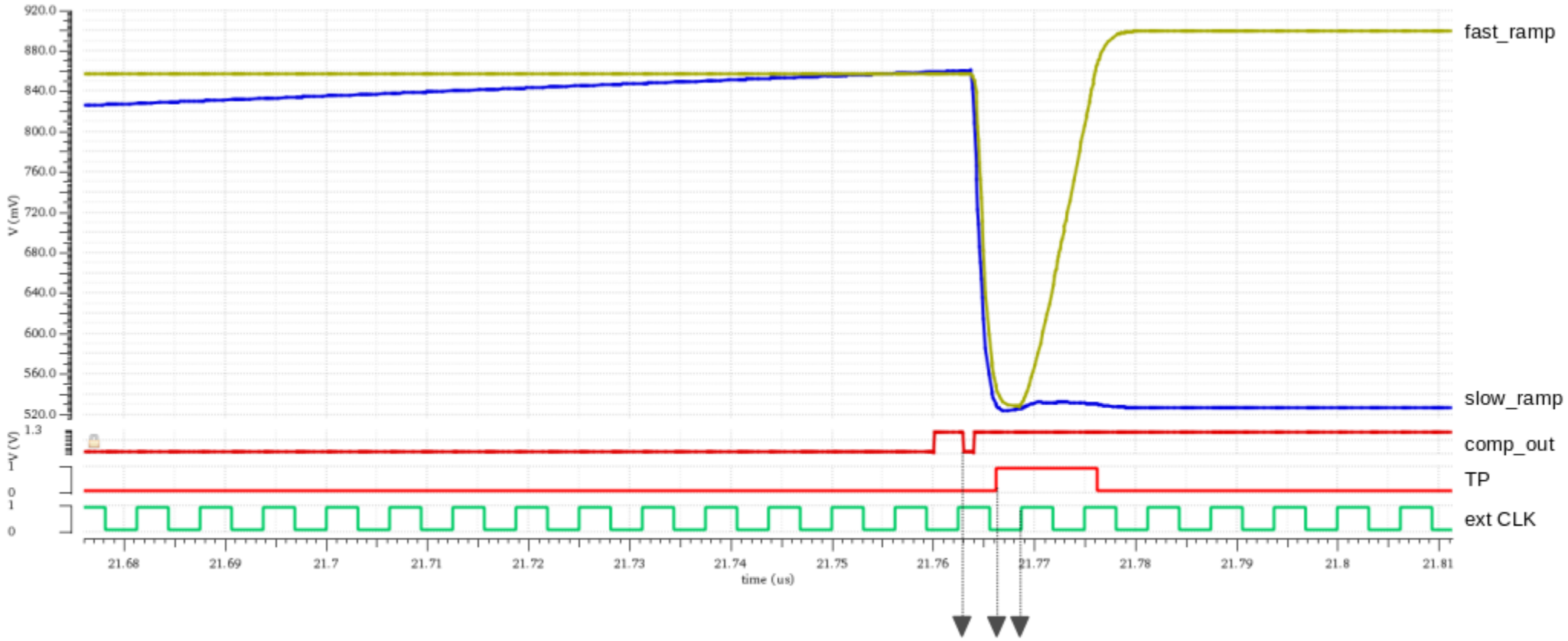
Pixel architecture

- **RCG**-based preamplifier
  - high bandwidth and low input-impedance (10-20 Ω)
  - **dual-polarity** to readout either the anode or cathode signal
- 2 independent TIA branches
  - **4 gain** settings
  - followed by **LE discriminator** with independent threshold (6-bit DAC)
- **Time measurement** from 4 **TDCs**, based on analogue interpolation (50ps time binning @320 MHz clock frequency)
- **Pixel** control **logic** handles TDCs operation, pixel configuration and data transmission



TDC logic error

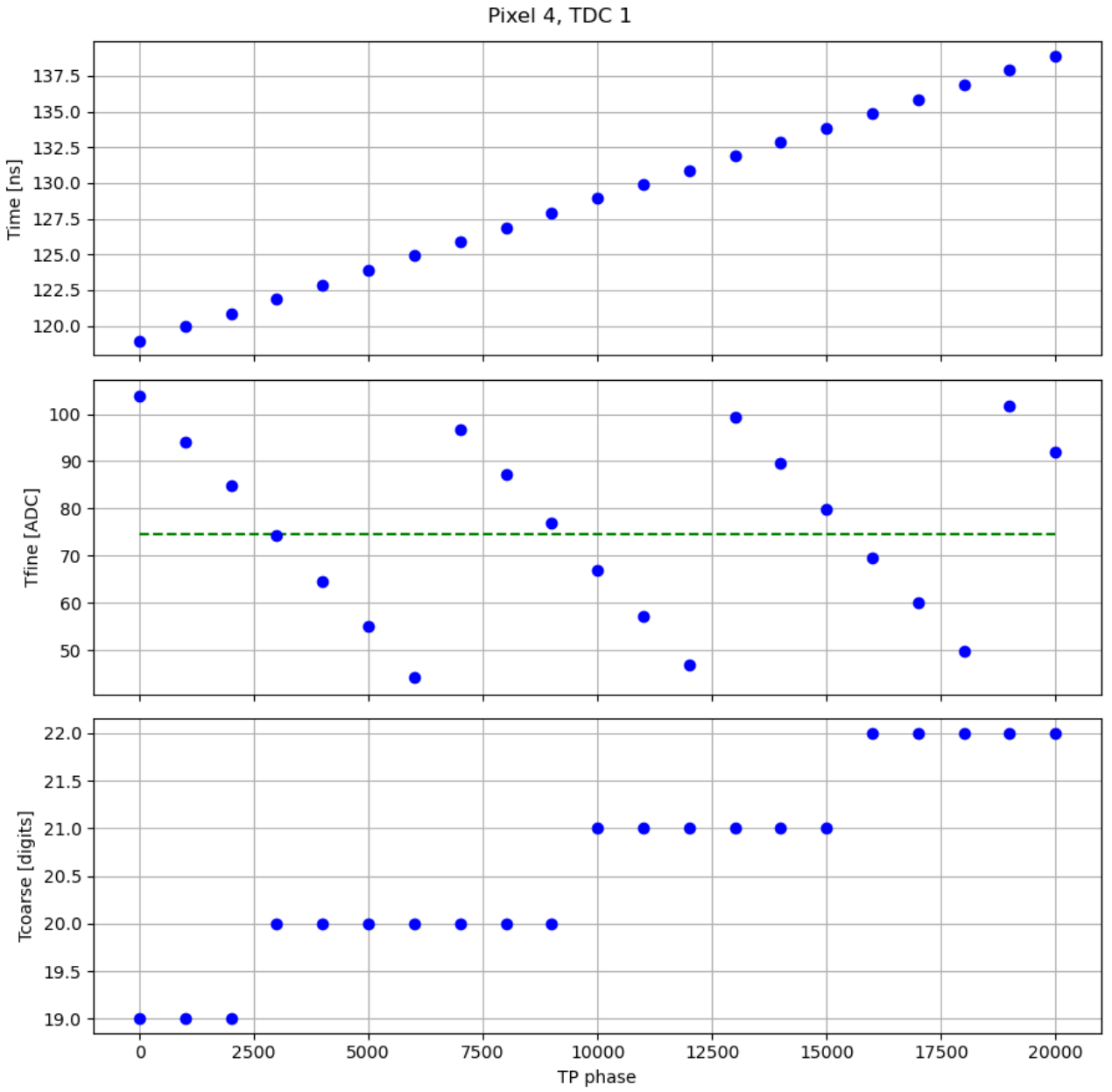
This puts the logic in a metastable state in which the same event word (with Tfine=0) is repeatedly transmitted off-chip, thus saturating the FPGA FIFO



TDC comparator defines EoC of previous event
Test-pulse arrives before next clock cycle (internal clock is shifted w.r.t. external CLK)
Fast ramp is correctly activated, while slow ramp is never activated and the TDC remains in this status until full-reset

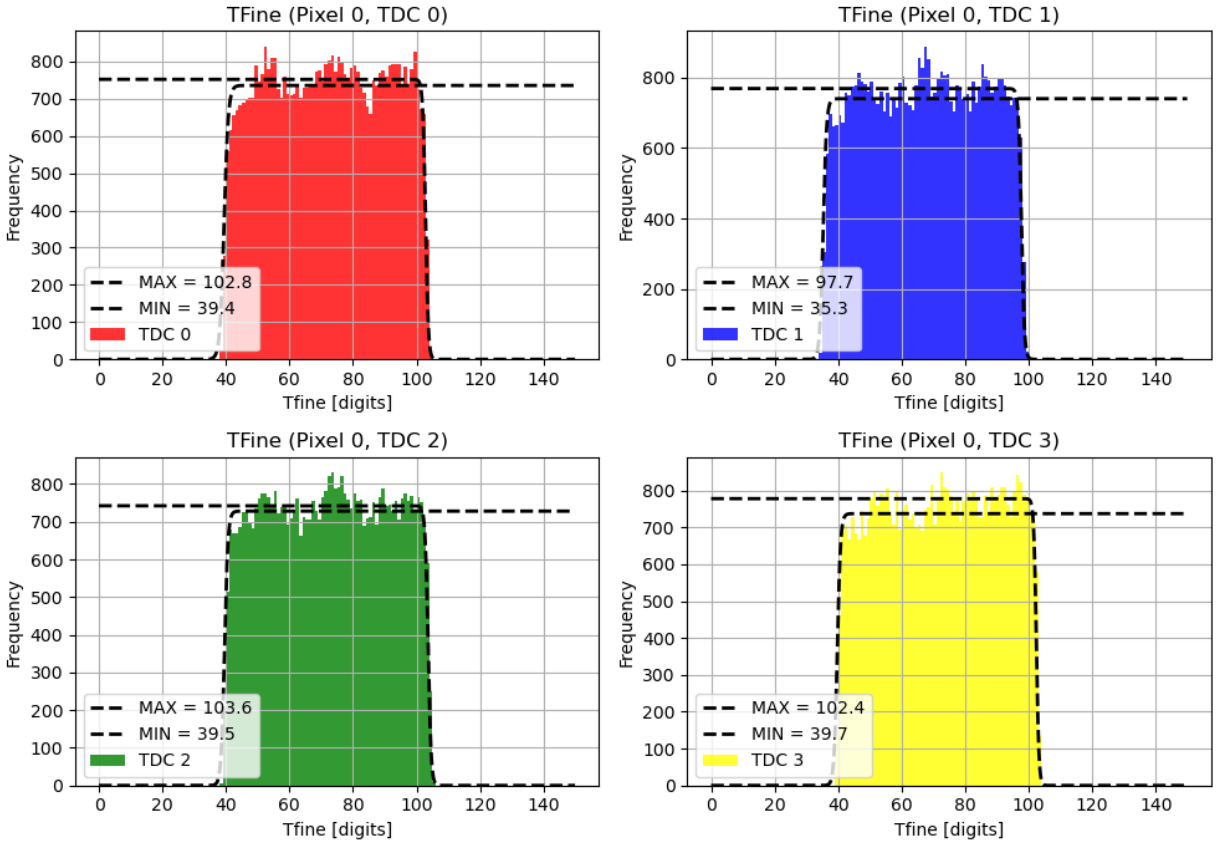
TDC – phase scan

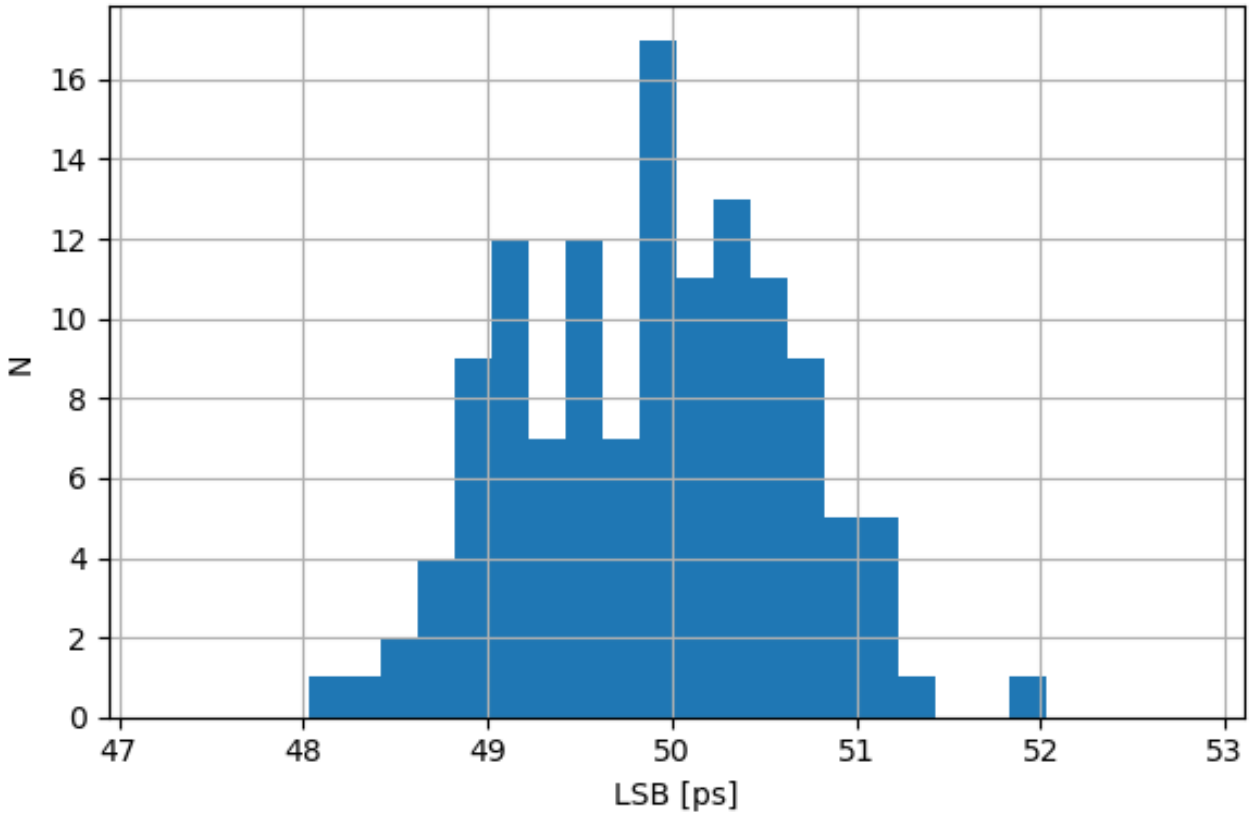
- 20 ns digital test-pulse phase scan
- Extract Tfine MIN and MAX for each TDC of each pixel → 128 entries LUT
  - IF = MAX - MIN
  - Time_bin = clk_period / IF
  - CUT = (MAX + MIN) / 2
- Tfine points across the CUT region may have a shift of 1 clock period



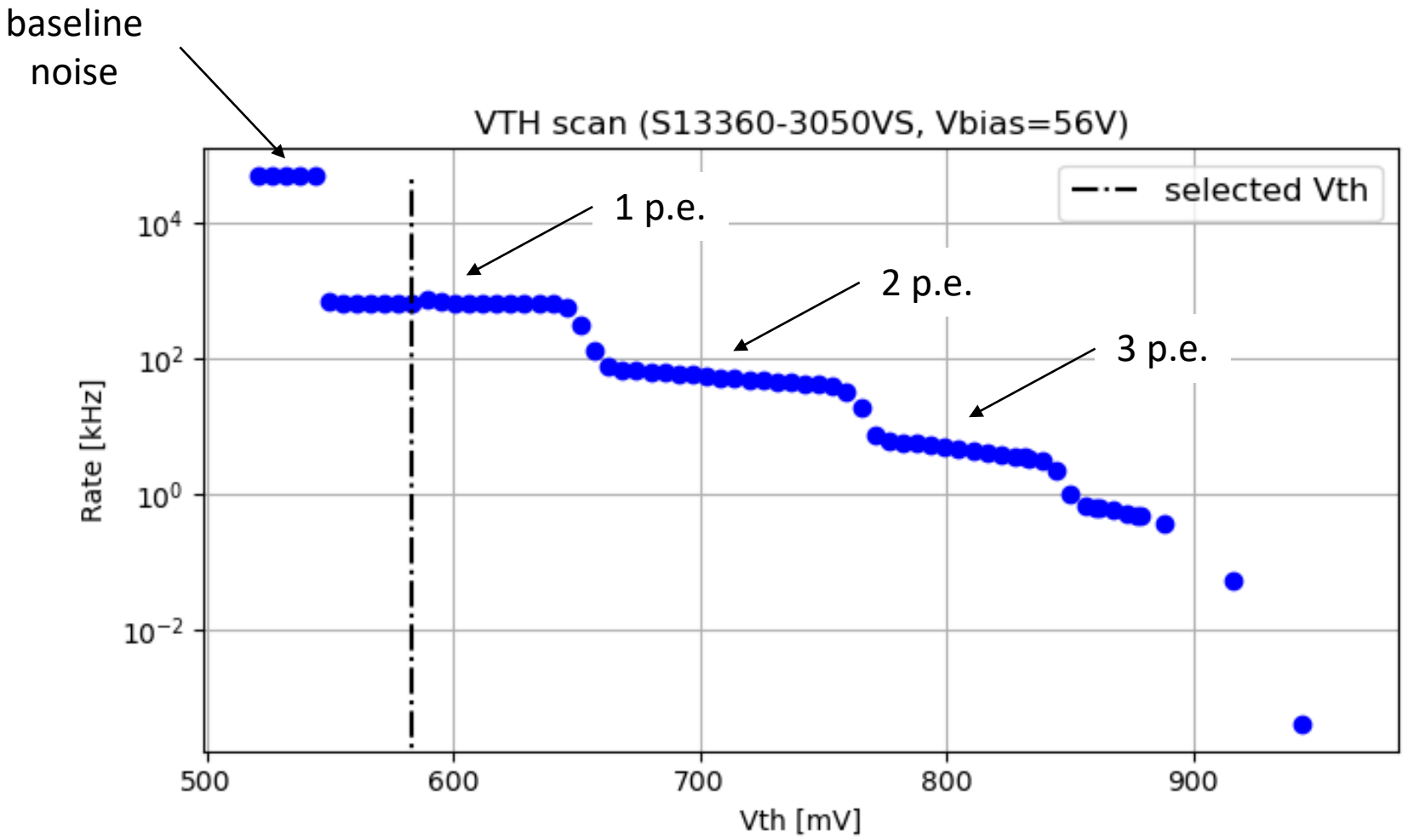
TDC – calibration from dark counts

TDCs calibration can be performed also using dark counts data



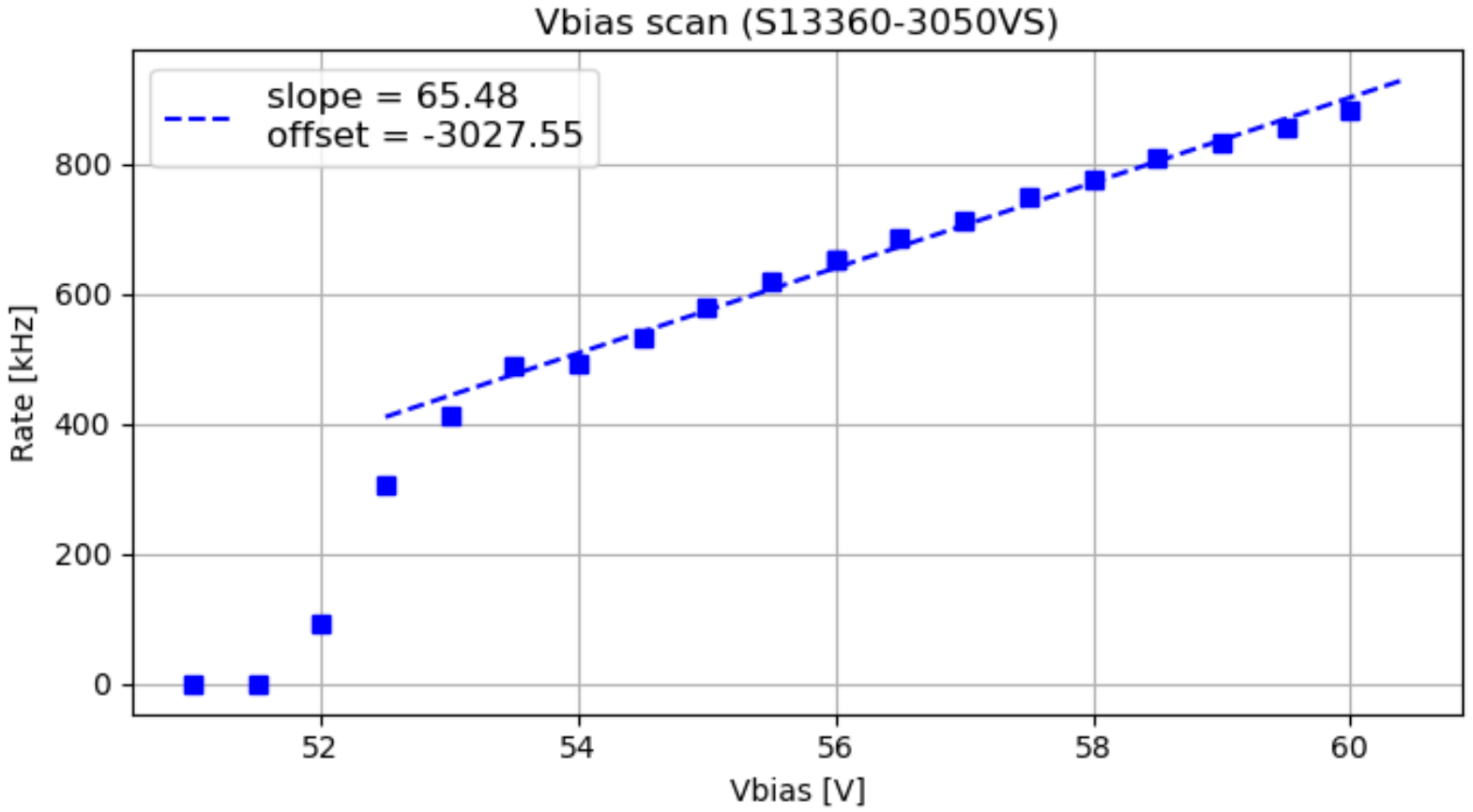


ALCOR threshold scan



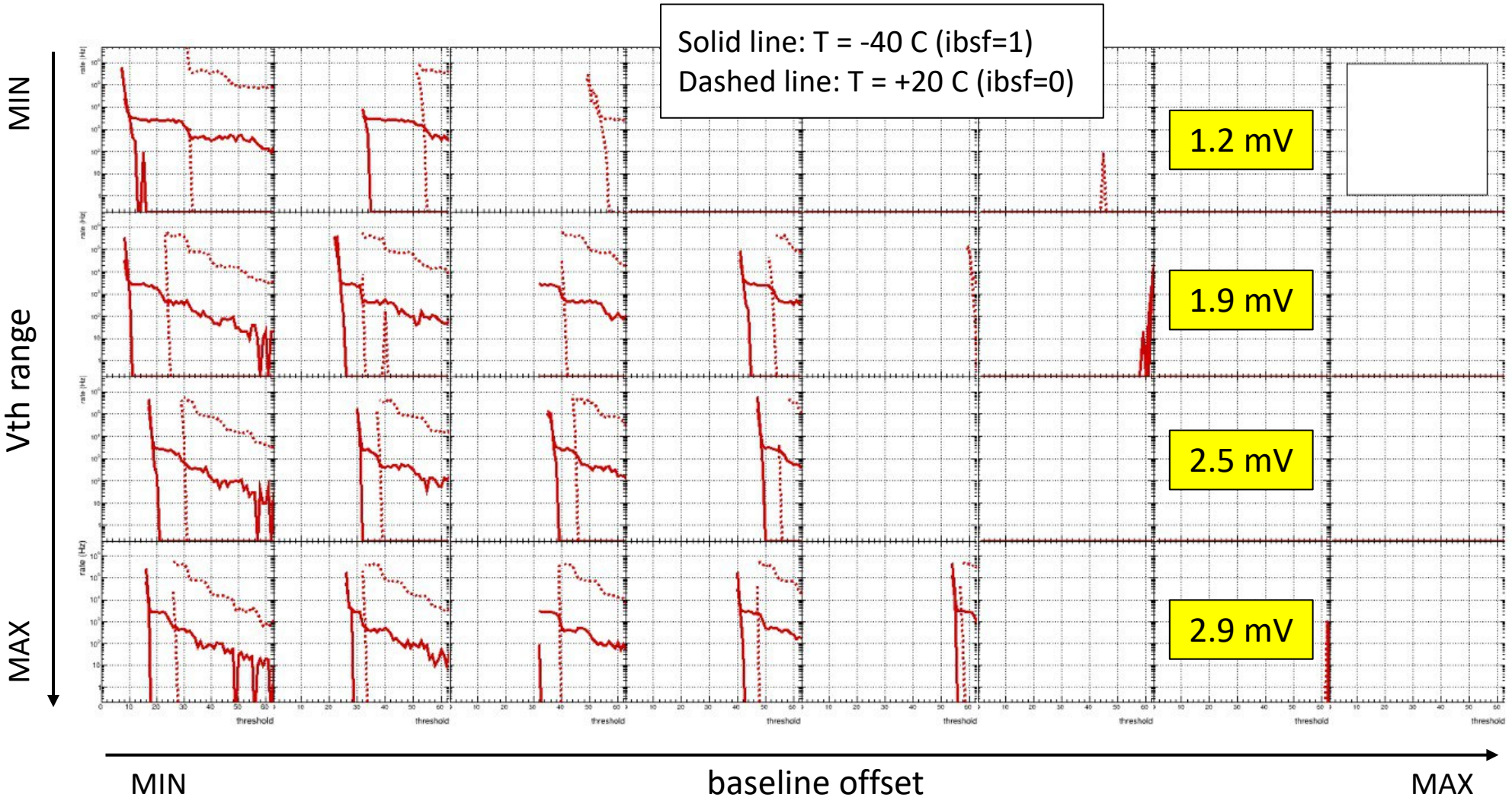
Dark-count rate *vs* threshold
→ “staircase” plot

SiPM Vbias scan



Dark-count rate *vs* Vbias
(V_{br} = 53 V, V_{op} = V_{br} + 3V)

BCOM – Vth scan (controlled temperature @Bologna)



With BCOM SiPM we need to decrease the VTH LSB in order to observe the 1 p.e. plateau

HAMA1 Vth scan was taken with default configuration: LSB = 5.6 mV

SiPM specs

Model	Gain	Ct [pF]	Cd [fF]	Vbr [V]	Vop [V]	DCR [kHz]
S13360-3050VS	$1.7 \cdot 10^6$	320	89	53	56.0	500
S13360-3025VS	$7.0 \cdot 10^5$	320	22	53	58.0	400
S14160-3050HS	$2.5 \cdot 10^6$	500	142	38	40.7	-
S14160-3015PS	$3.6 \cdot 10^5$	530	13	38	42.0	700
AFBR-S4N33C013	$1.6 \cdot 10^6$	645	66	26.9	29.9	1000
MICROFJ-300xx-TSV-TR1	$2.9 \cdot 10^6$	1070		24.5	27	500