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Development of a resource-efficient FPGA-based neural network regression model for the ATLAS muon trigger upgrades

Friday, 8 July 2022 18:00 (15 minutes)

This contribution will present a resource-efficient FPGA-based neural network regression model which was developed for potential applications in the future hardware muon trigger system of the ATLAS experiment at the Large Hadron Collider (LHC). Our model uses a neural network regression to significantly improve the rejection of the dominant source of background events in the central detector region, due to muon candidates with low transverse momenta. Effective real-time selection of muon candidates is the cornerstone of the ATLAS physics programme. The entirely new FPGA-based hardware muon trigger system will be installed in 2025-2026 that will process full muon detector data within a 10 microsecond latency. The large FPGA devices planned for this upgrade will have sufficient resources to allow deployment of machine learning methods for improving identification of muon candidates and for searching for new exotic particles. We developed a resource efficient implementation of the neural network regression model using the FPGA hardware description language. Our implementation was carefully optimised in order to minimise neural network latency and FPGA resource usage. This contribution will present simulation results of the network performance using a simplified detector model. Details of FPGA hardware implementation, optimisation and performance will also be presented. The simulated network latency and deadtime are well within the requirements of the future ATLAS muon trigger system, therefore opening a possibility for deploying machine learning methods for data taking by the ATLAS experiment at the High Luminosity LHC.

In-person participation

Yes

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