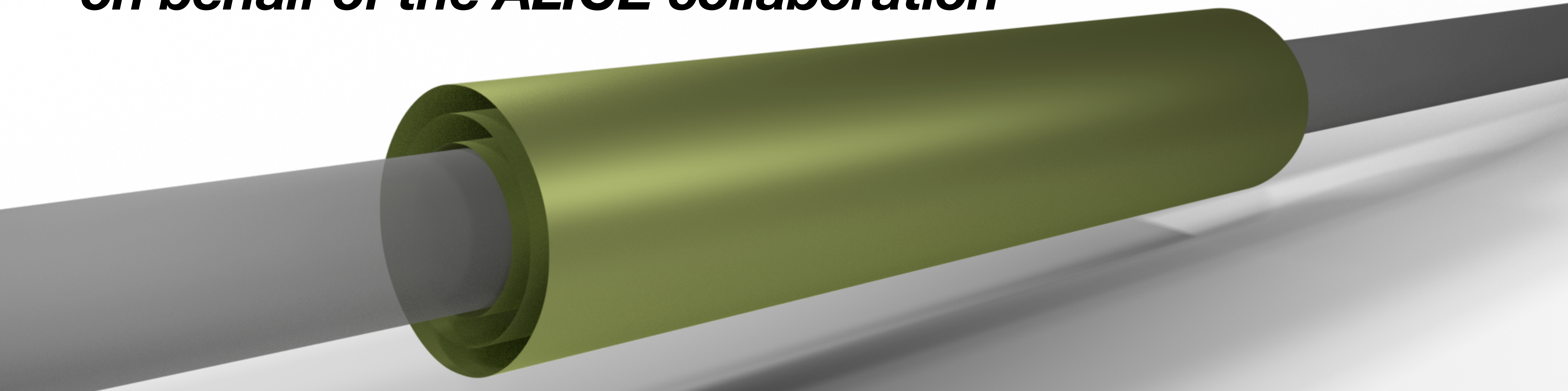
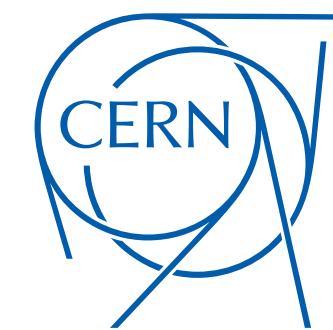


A truly cylindrical inner tracker for ALICE

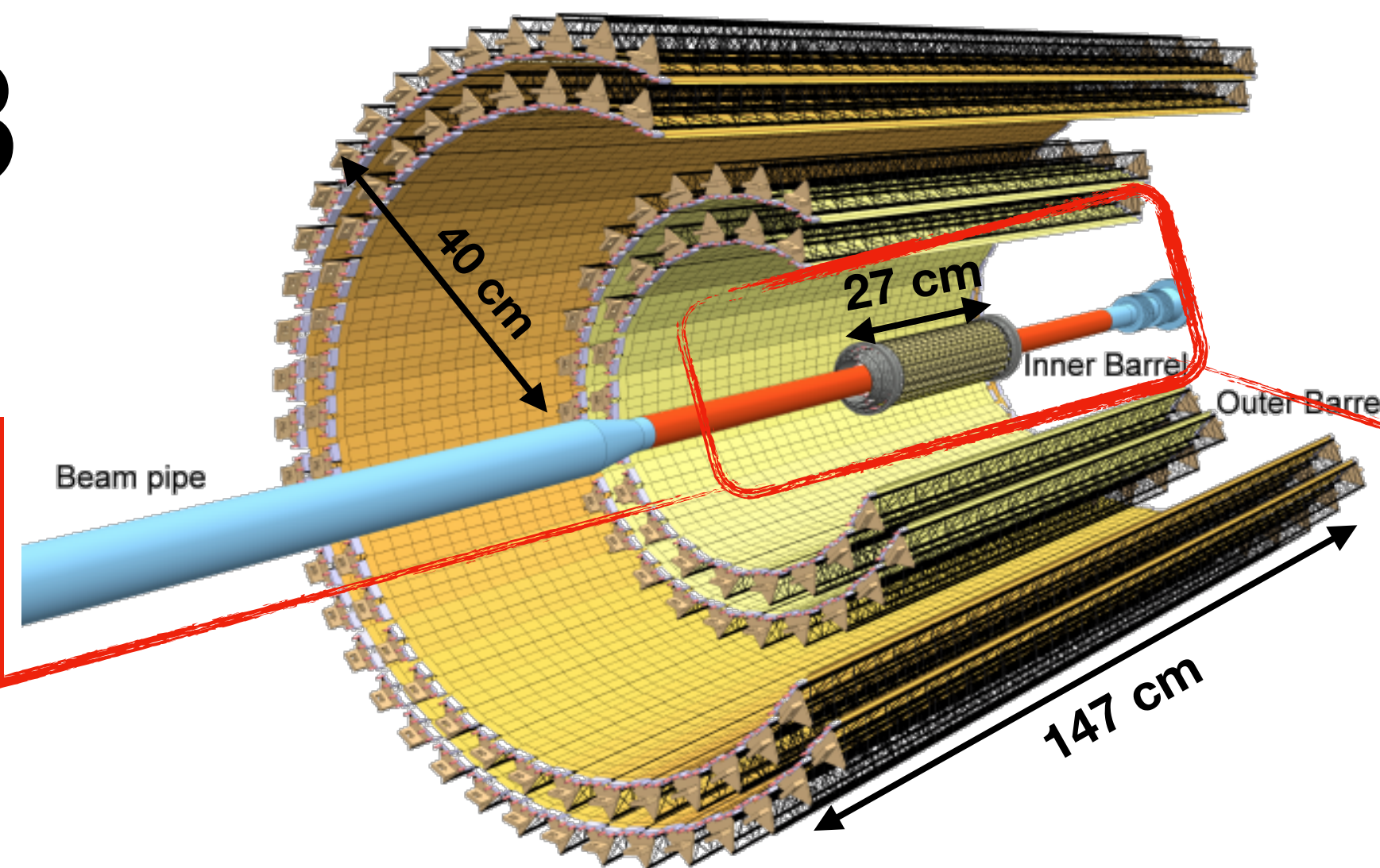
Magnus Mager (CERN)
on behalf of the ALICE collaboration



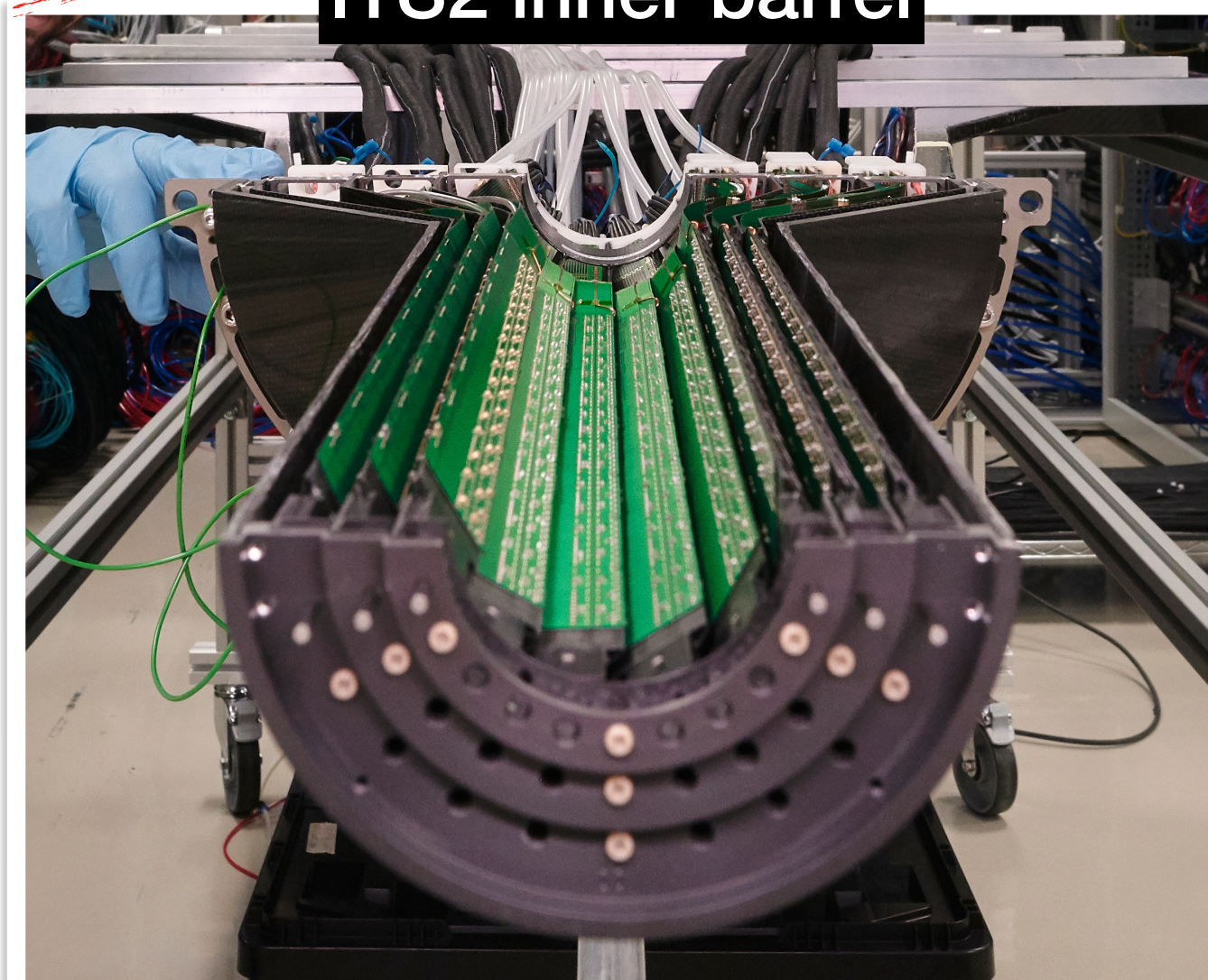
ITS2 → ITS3



→ tomorrow, 9:00:
Robert H. Münzer
Preparation of ALICE for Run 3

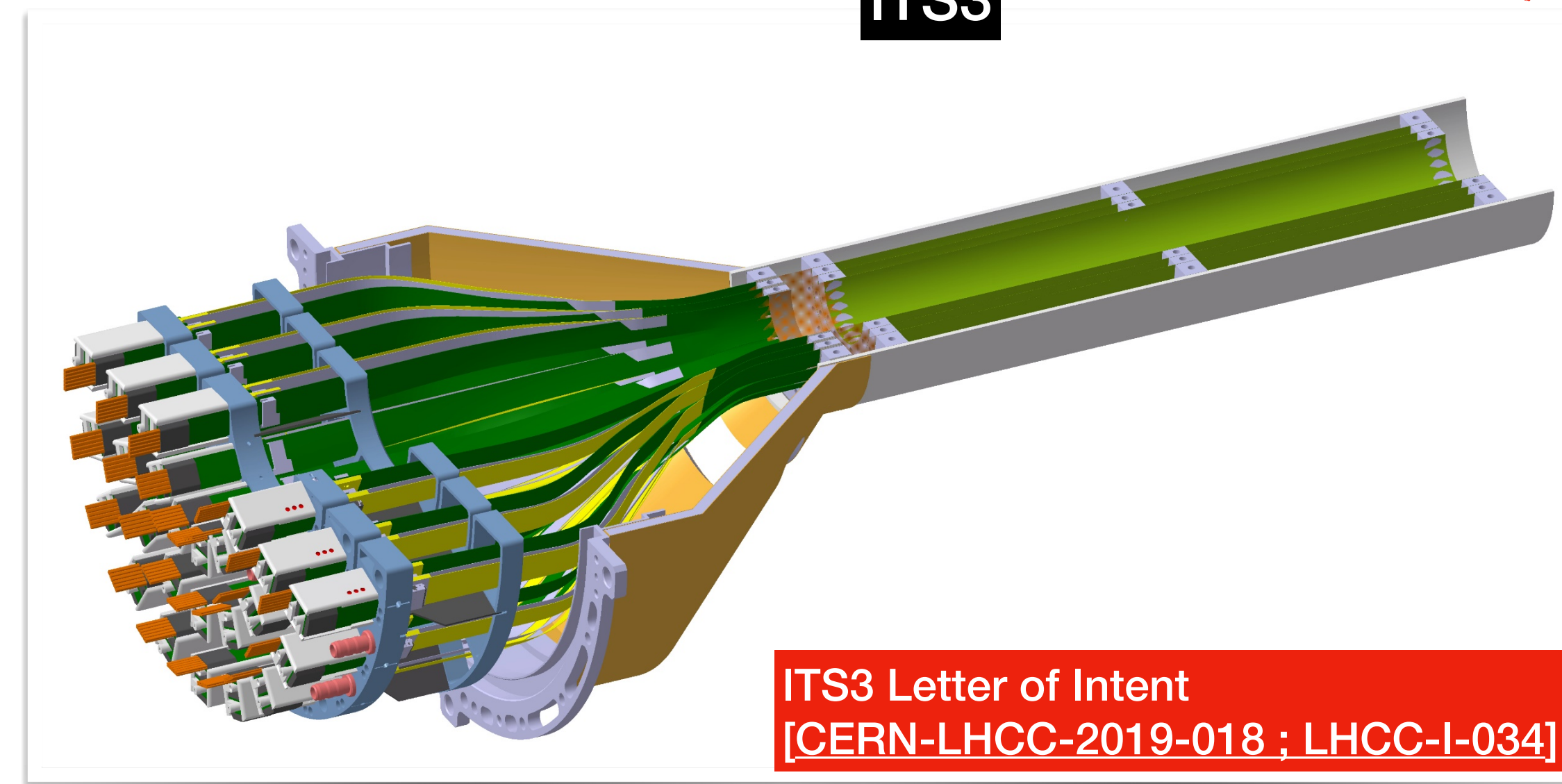


ITS2 inner barrel



LS3
replacement of inner
barrel

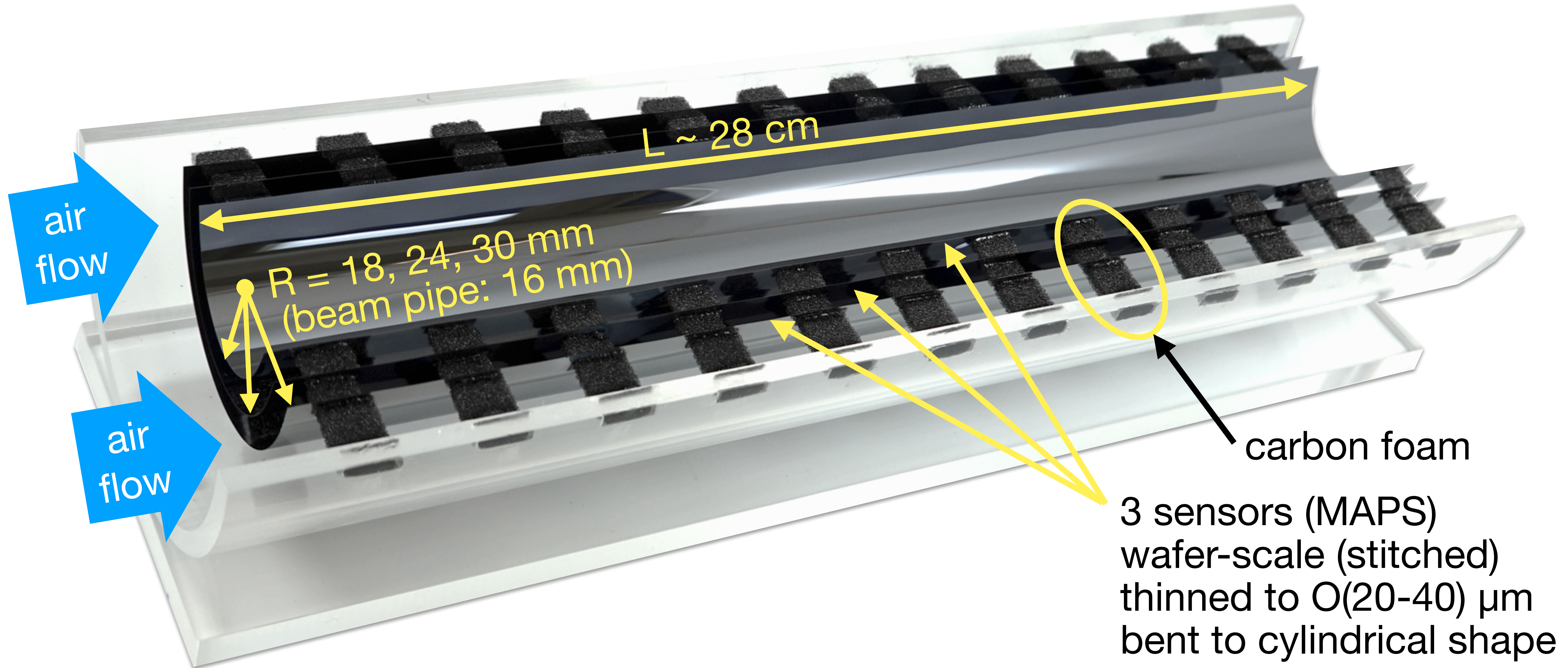
ITS3



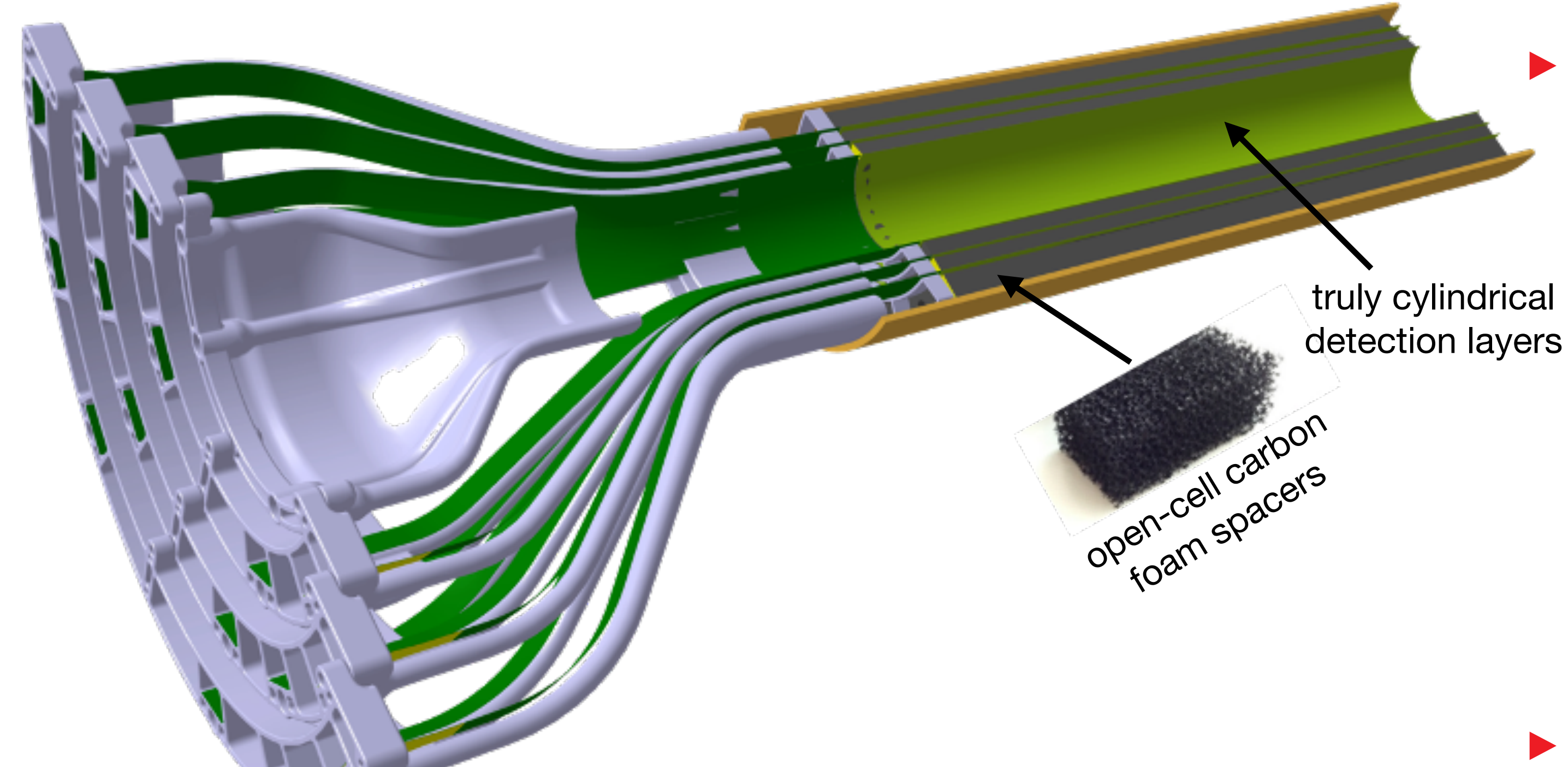
[LHC timeline]

ITS3 detector concept (1)

mechanical mockup using silicon dummies



ITS3 detector concept (2)



► Key ingredients:

- 300 mm wafer-scale sensors, fabricated using stitching
- thinned down to 20-40 μm (0.02-0.04% X_0), making them flexible
- bent to the target radii
- mechanically held in place by carbon foam ribs

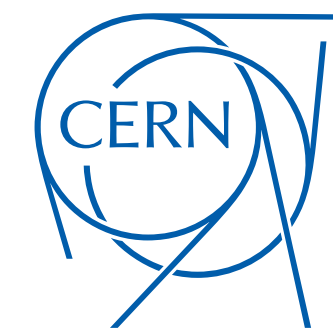
► Key benefits:

- extremely low material budget: 0.02-0.04% X_0 (beampipe: 500 μm Be: 0.14% X_0)
- homogeneous material distribution: negligible systematic error from material distribution

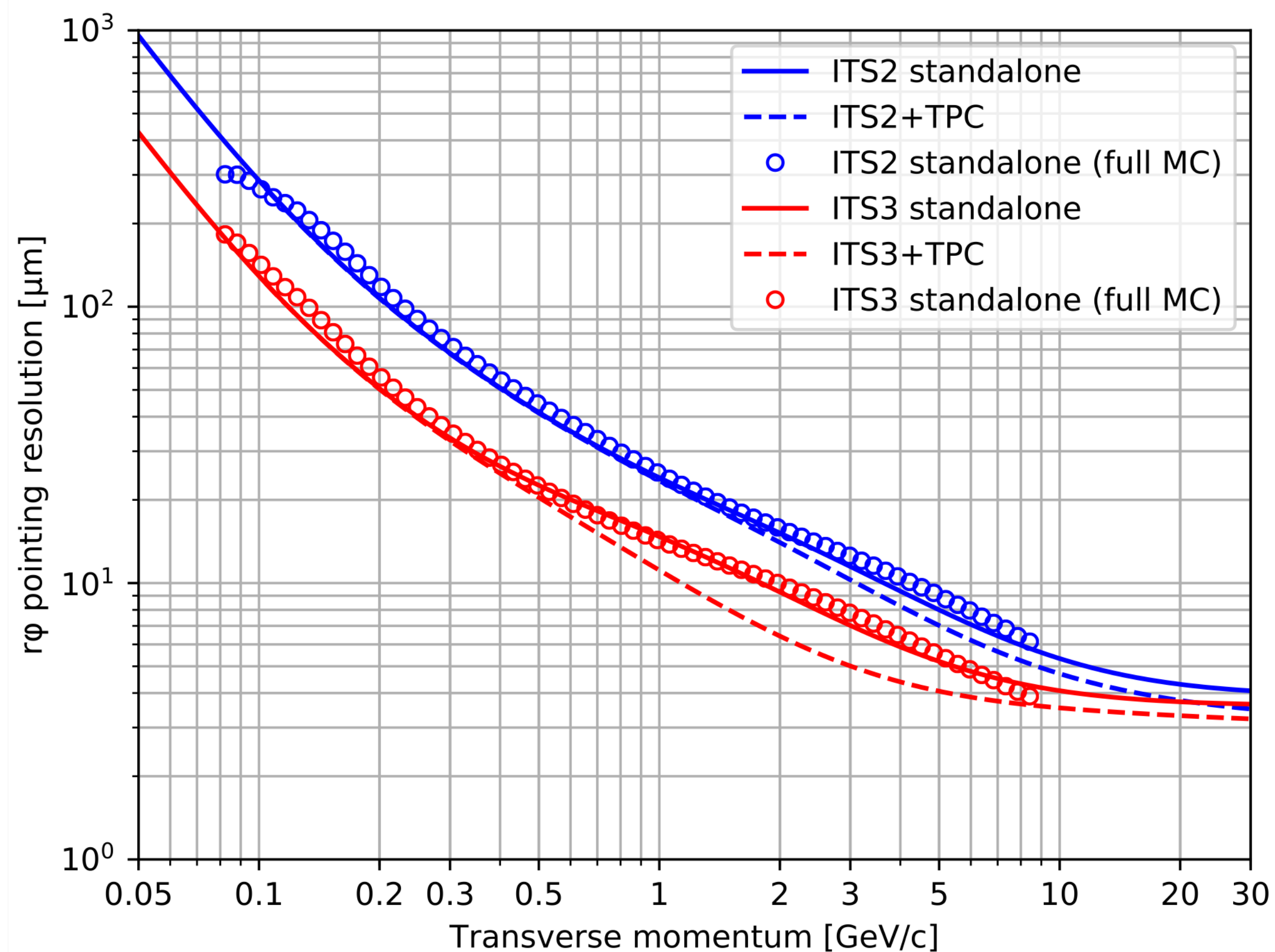
Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	± 2.5	± 2.3	± 2.0
Active area (cm ²)	610	816	1016
Pixel sensor dimensions (mm ²)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

The whole detector will consist of six (!) sensors (current ITS IB: 432) – and barely anything else

Performance improvement



pointing resolution



[ALICE-PUBLIC-2018-013]

improvement of factor 2 over all momenta

- ▶ Improvement of pointing resolution by:
 - drastic reduction of **material budget** ($0.3 \rightarrow 0.05\%$ X_0/layer)
 - being **closer** to the interaction point ($24 \rightarrow 18$ mm)
 - thinner and smaller and **beam pipe** ($700 \rightarrow 500 \mu\text{m}$; $18 \rightarrow 16$ mm)
- ▶ Directly boosts the ALICE core physics program that is largely based on:
 - low momenta
 - secondary vertex reconstruction
- ▶ E.g. Λ_c S/B improves by factor 10, significations by factor 4

Main R&D lines towards ITS3

Ultra-light mechanics and cooling

- ▶ mechanical concept to hold thin sensors “without” material
 - development of assembly procedure
 - qualification of carbon foams
- ▶ verification and optimisation of air cooling concept

Thinning, bending, interconnection

- ▶ development of procedures to handle and bend large thin chips
- ▶ characterisation of electrical and mechanical properties of sensors after bending
- ▶ development of electrical interconnection to bent chips

Wafer-scale sensor development

- ▶ switch to 65 nm technology (TPSCo)
 - verification of the technology for radiation tolerance and charge collection
- ▶ stitched sensor design
 - chip architecture
 - optimisation for yield

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Bending of wafer-scale sensors procedure



$R = 30 \text{ mm}$ (layer 2)
50 μm silicon

Bending of wafer-scale sensors procedure



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 $50 \text{ }\mu\text{m}$ silicon

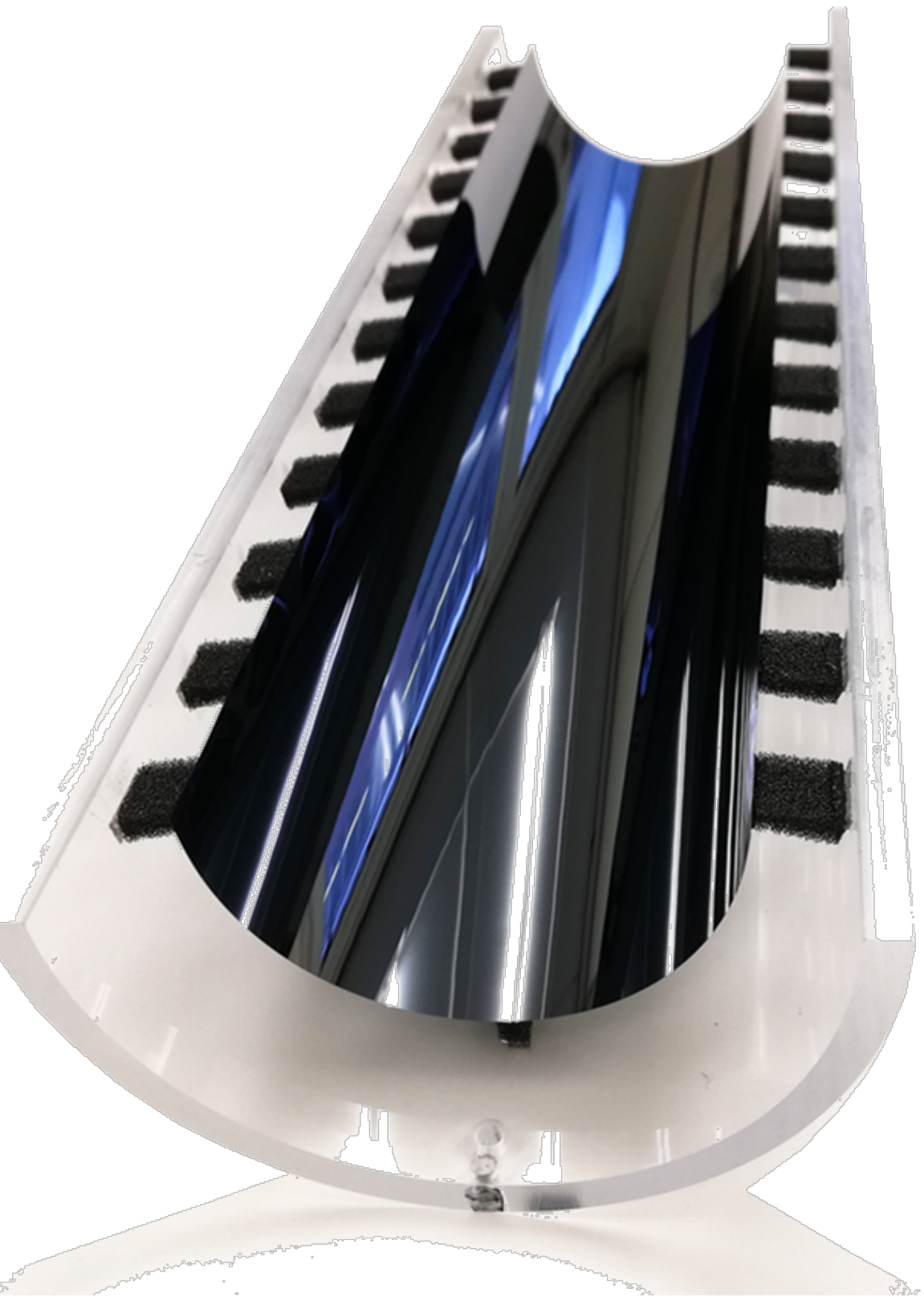
Bending of wafer-scale sensors procedure



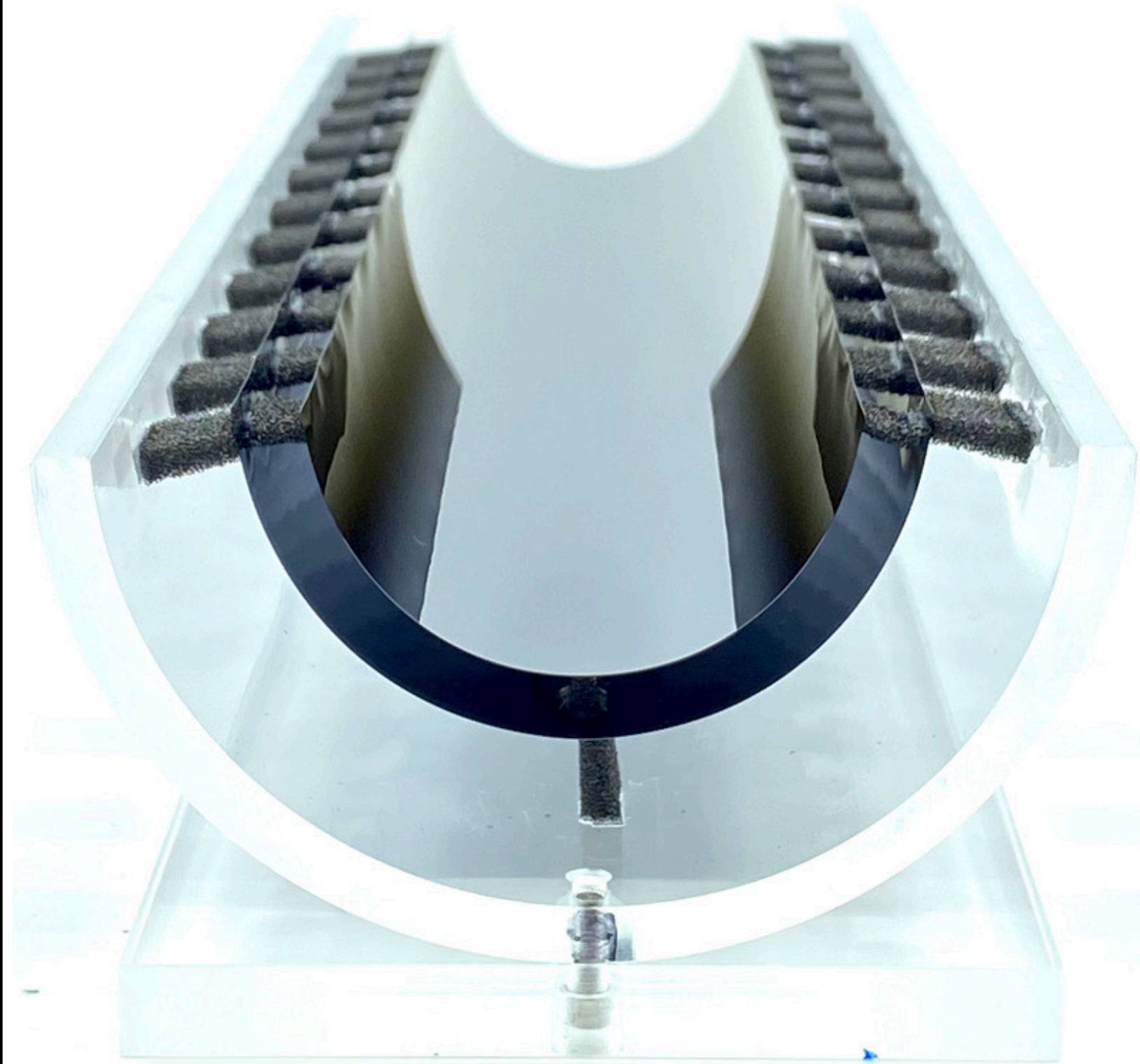
$R = 30 \text{ mm}$ (layer 2)
 $50 \text{ }\mu\text{m}$ silicon

Layer assembly

Layer 2



Layers 2+1



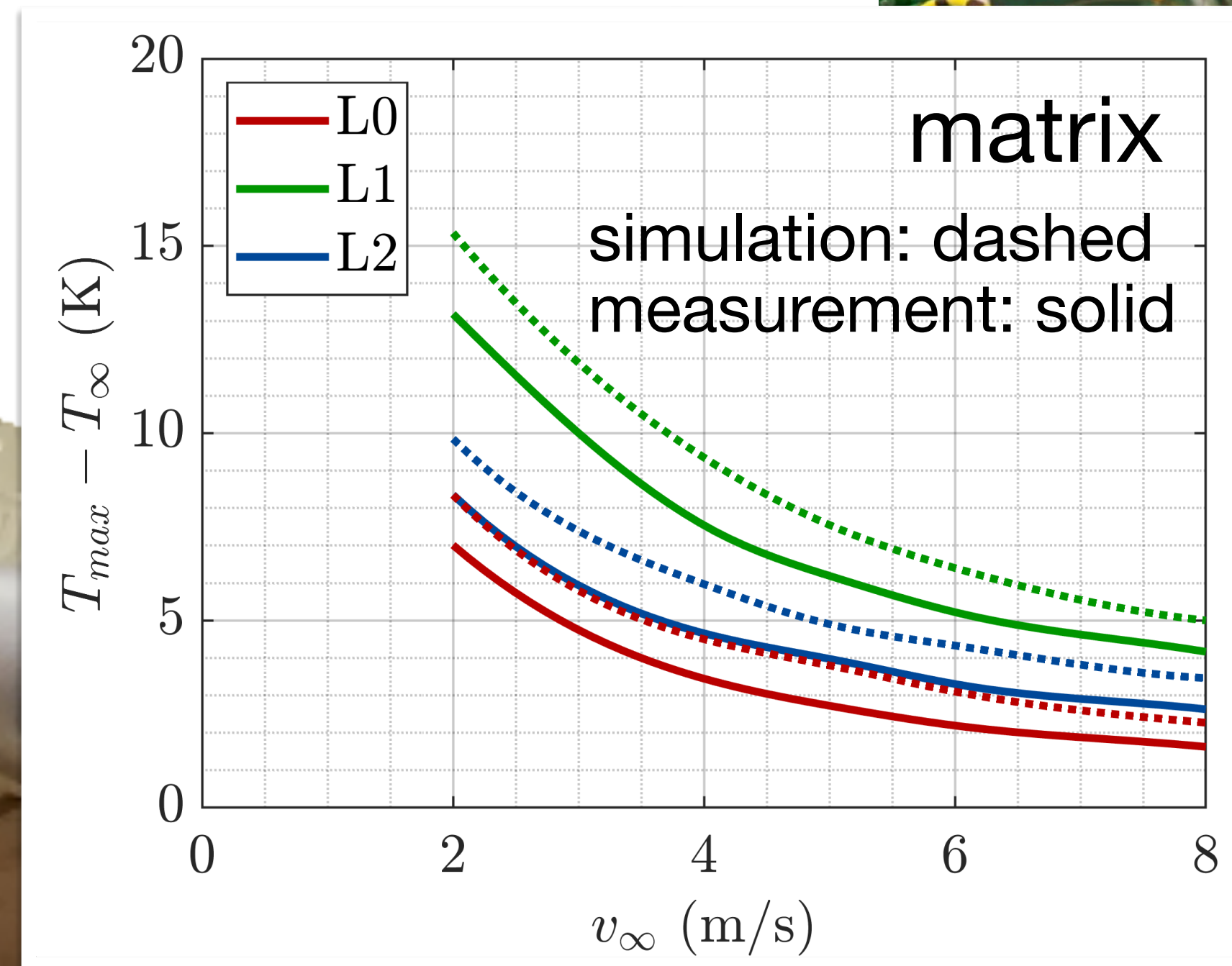
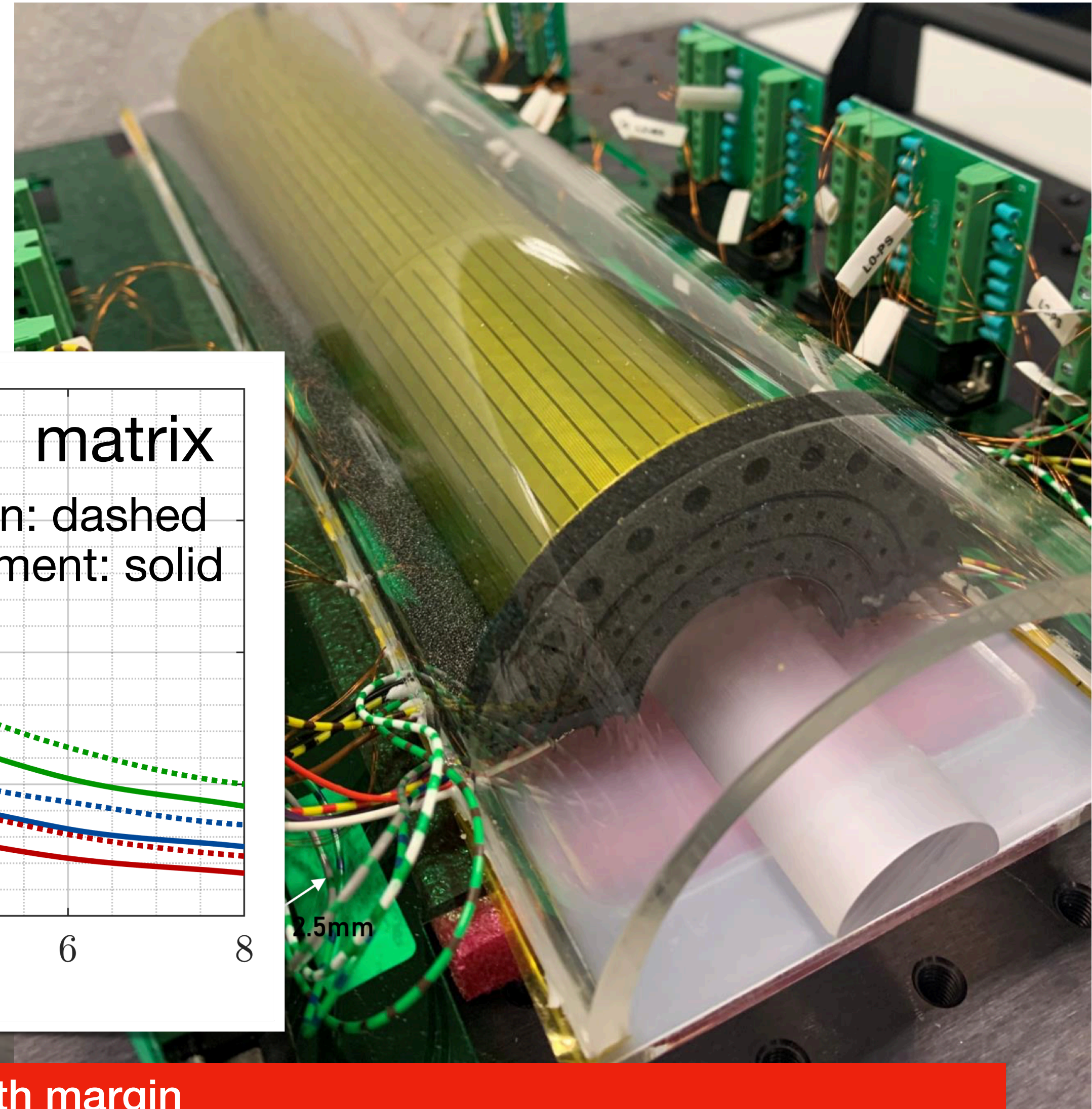
Layers 2+1+0



Mechanically, the integration is very feasible – now the assemblies are characterised and optimised

R&D on air cooling

- ▶ A set of models based on heating elements are being developed
- ▶ Placed in a custom wind tunnel, thermal and mechanical properties are studied



Air cooling is feasible with margin

Main R&D lines towards ITS3

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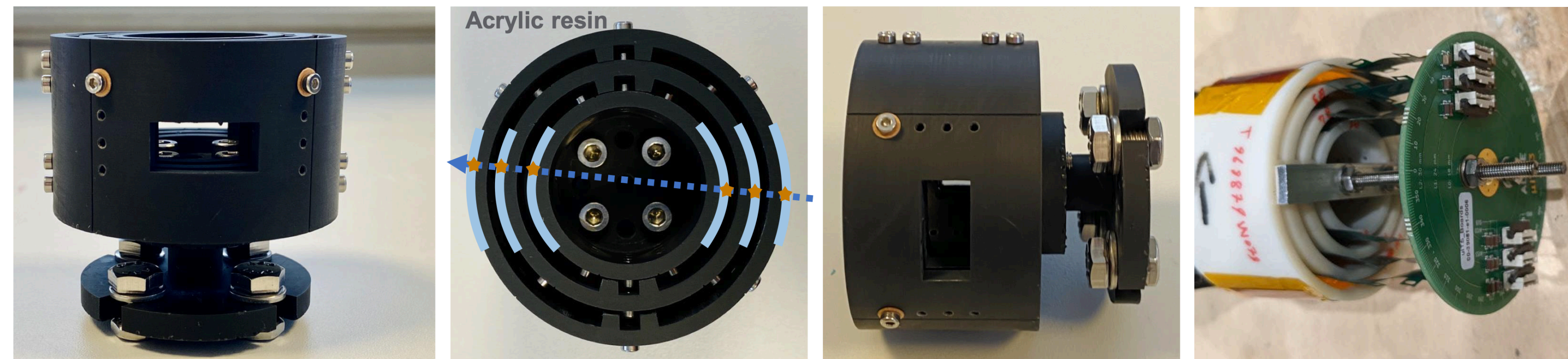
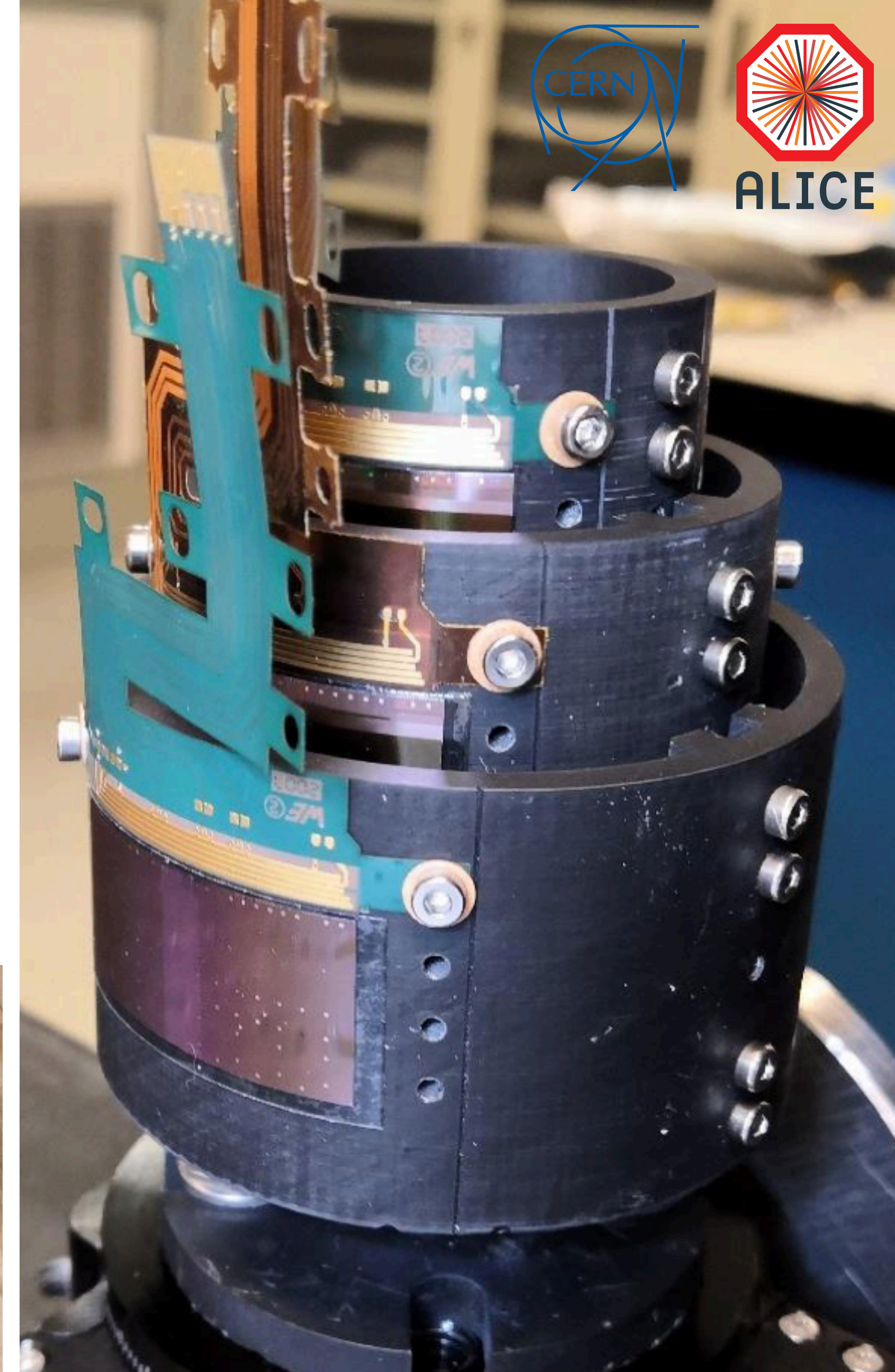
Wafer-scale sensor development

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 - verification of the technology for radiation tolerance and charge collection
- ▶ stitched sensor design
 - chip architecture
 - optimisation for yield

Bent ALPIDEs

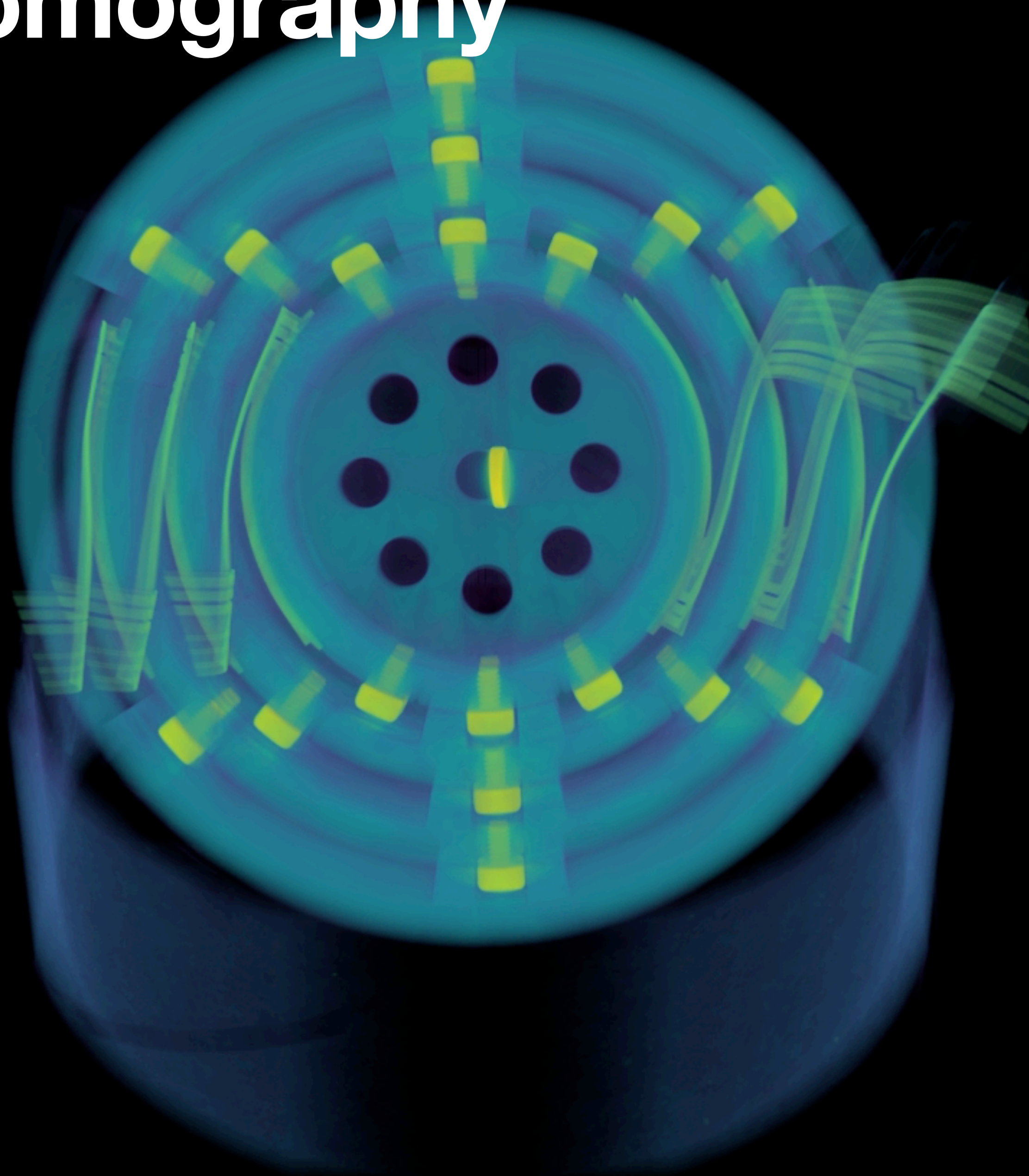
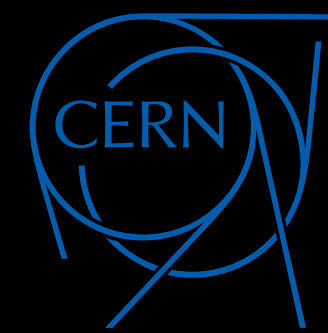
[doi:10.1016/j.nima.2021.166280]

- ▶ Functional chips (ALPIDEs) are bent routinely
 - several different ways were explored (bending before bonding, or vice versa, different jigs)
 - all radii of ITS3 are easily achievable
- ▶ Chips continue to work
 - tested at several beam campaigns
- ▶ By now, we have a full mock-up of the final ITS3, called “ μ ITS3”
 - 6 ALPIDE chips, bent to the target radii of ITS3

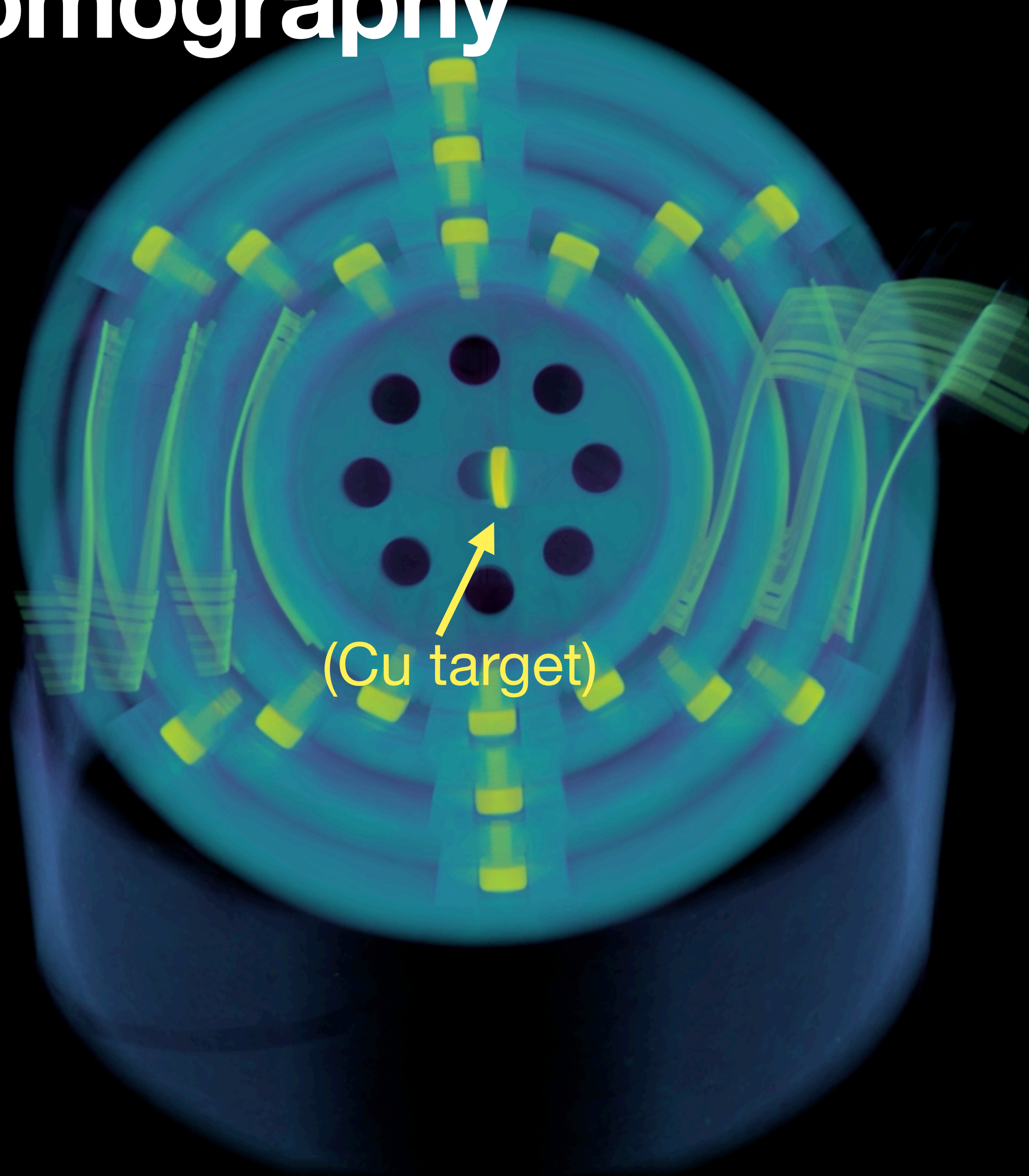
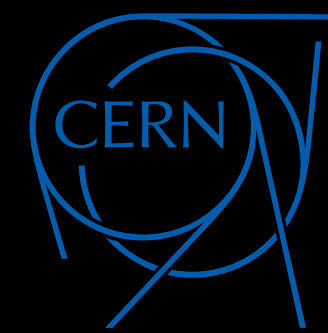


Mechanically, the integration is very feasible – now the assemblies are characterised and optimised

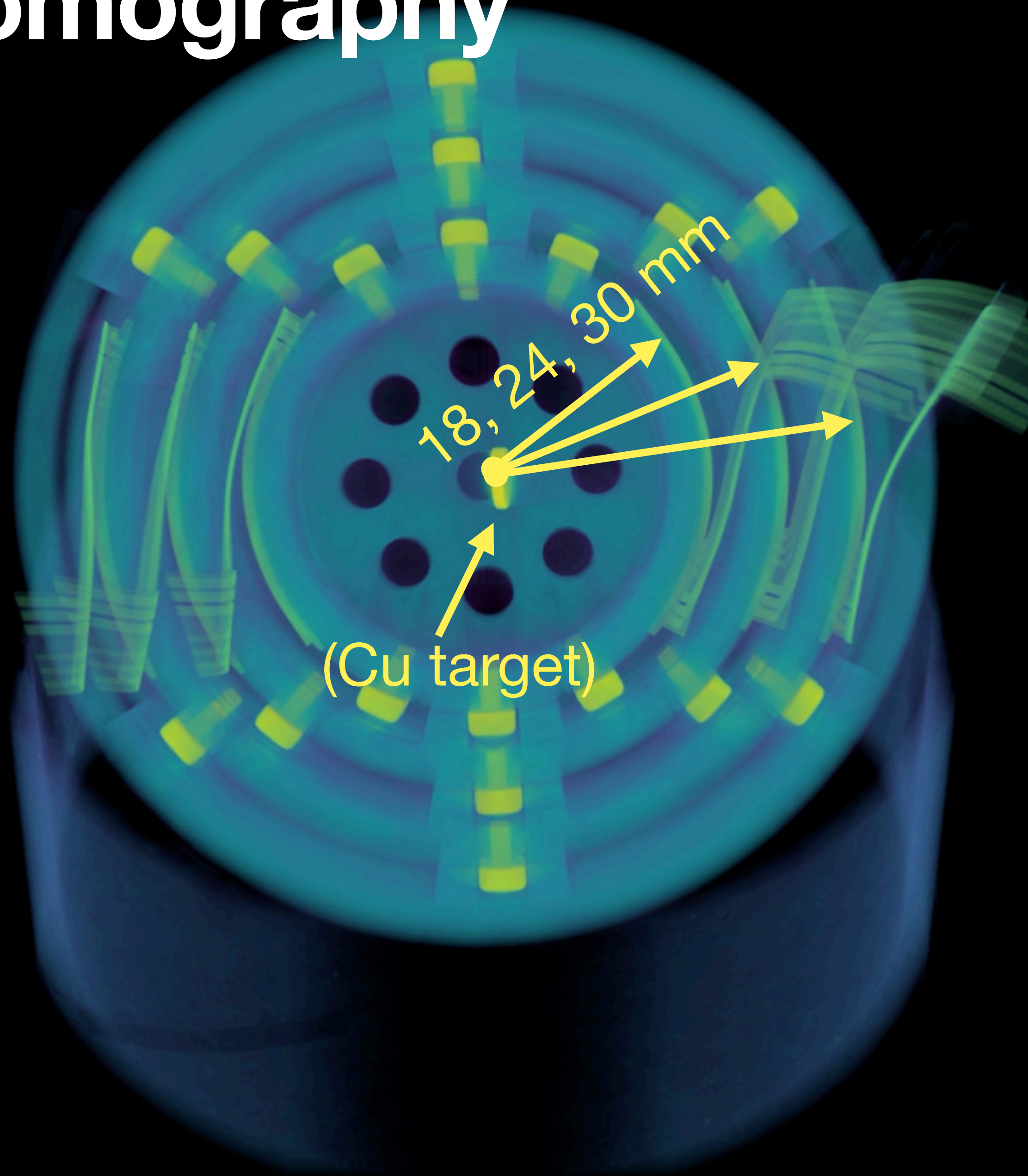
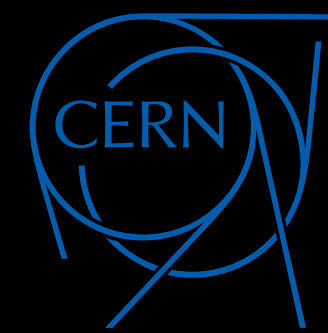
μ ITS3 X-ray tomography



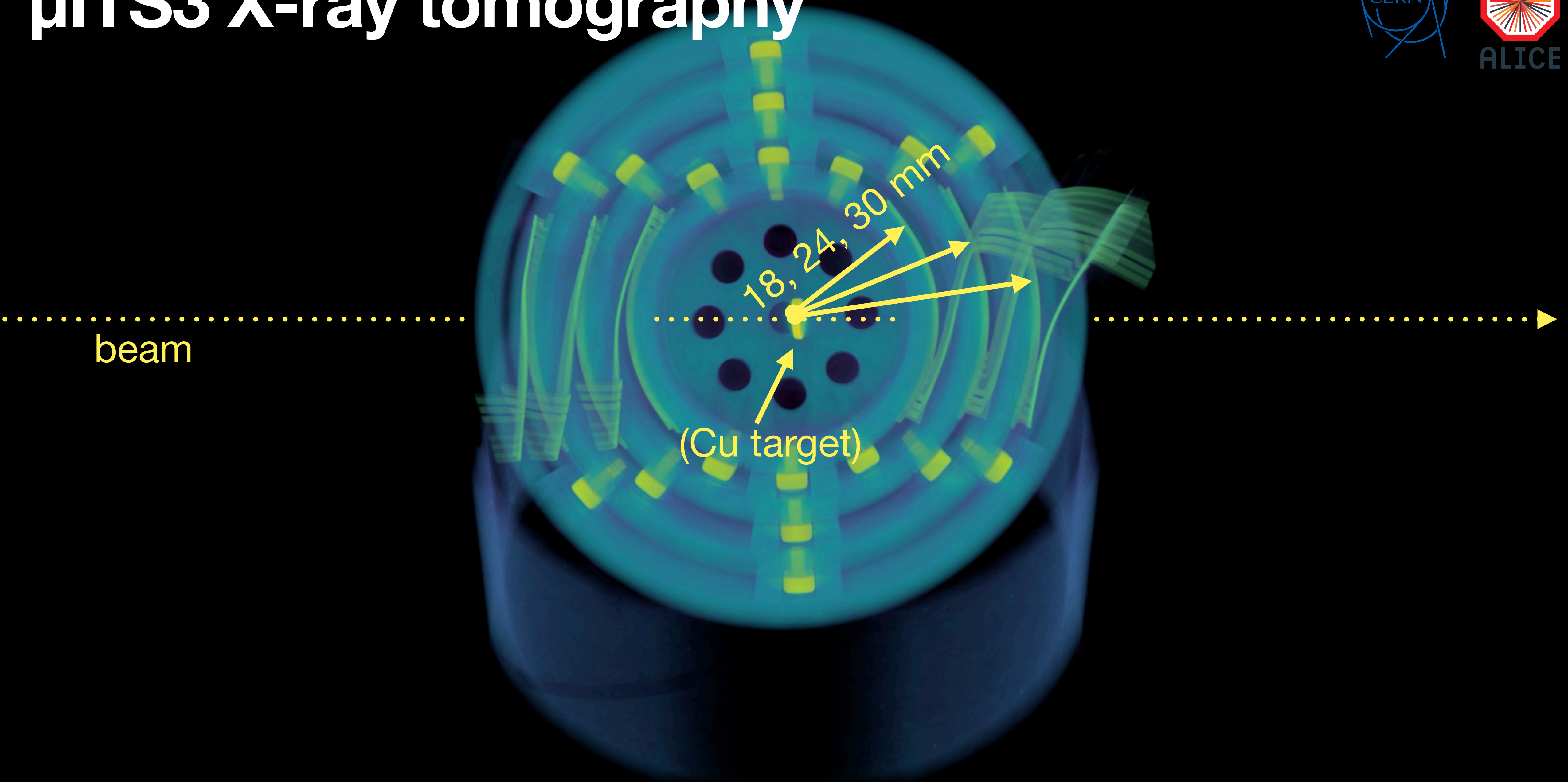
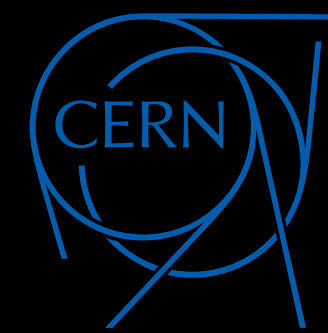
μ ITS3 X-ray tomography



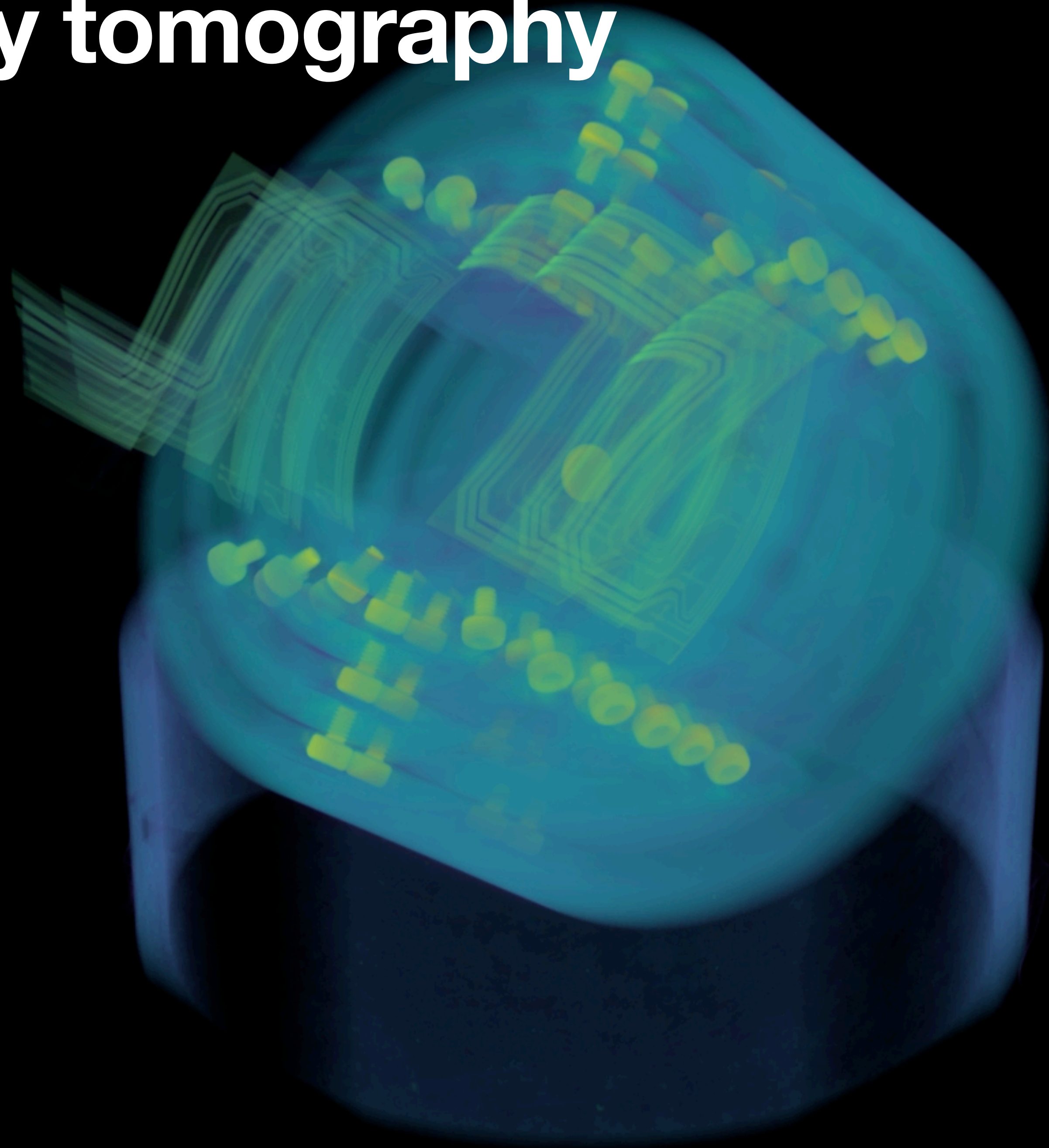
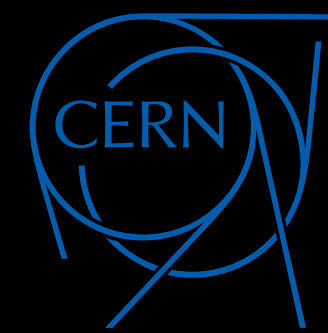
μ ITS3 X-ray tomography



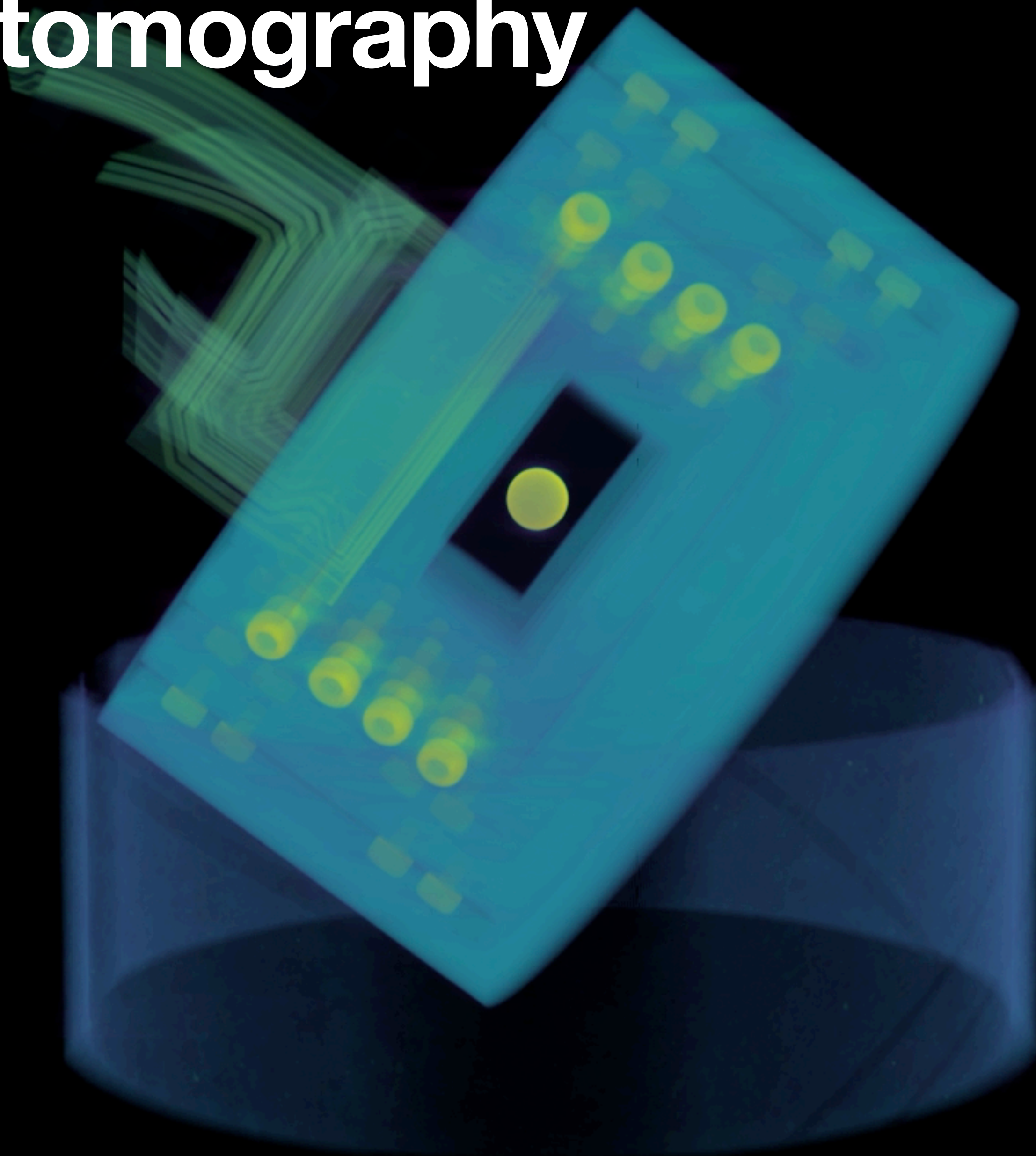
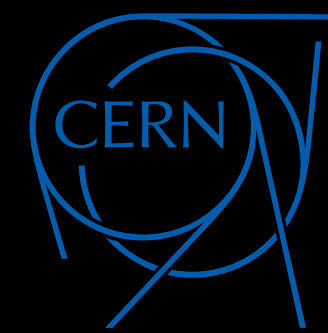
μ ITS3 X-ray tomography



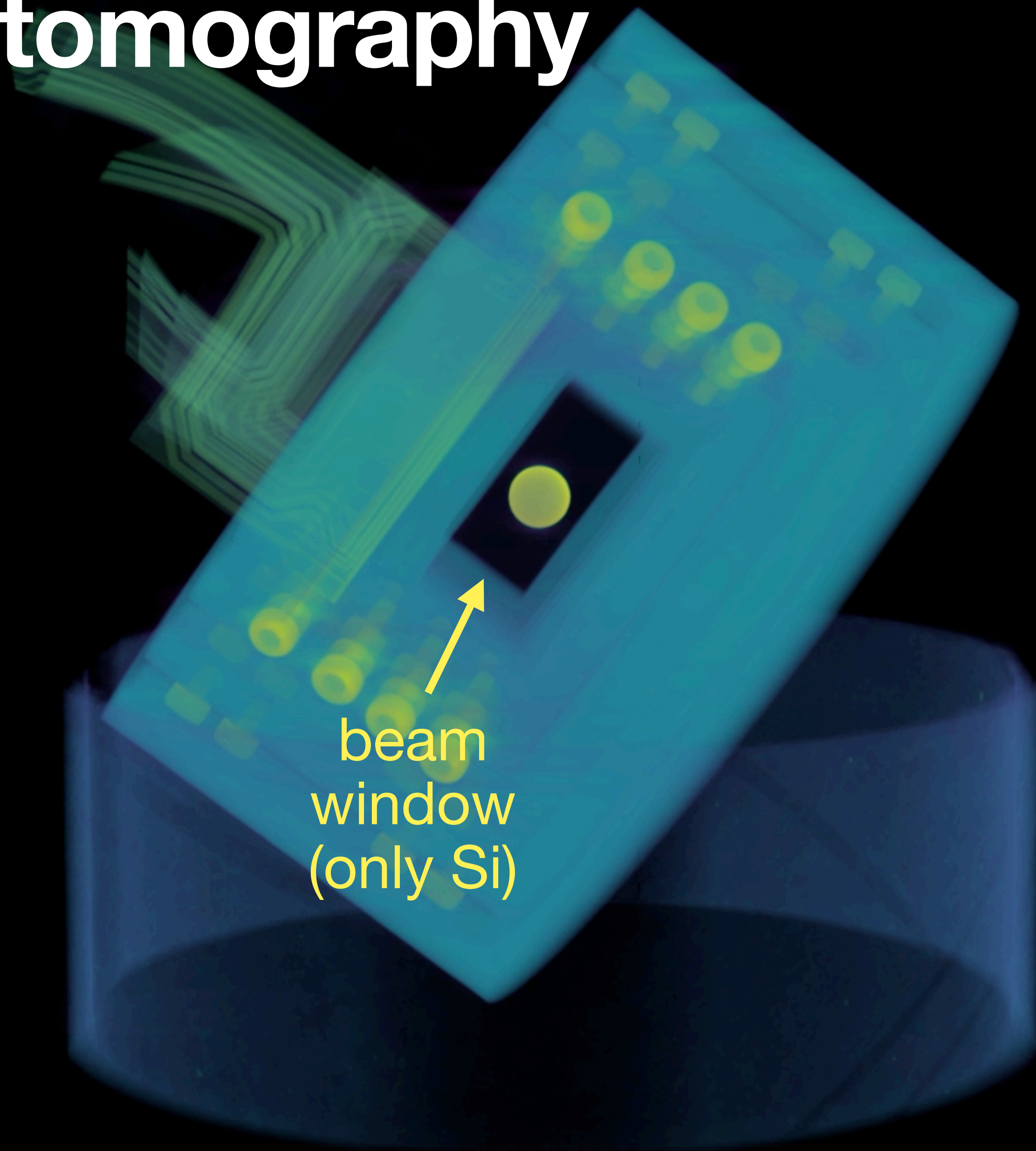
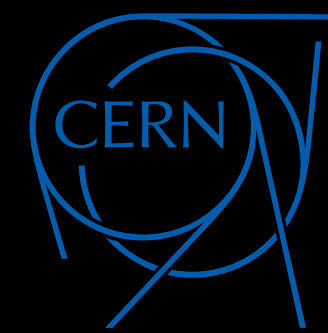
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μ ITS3 X-ray tomography



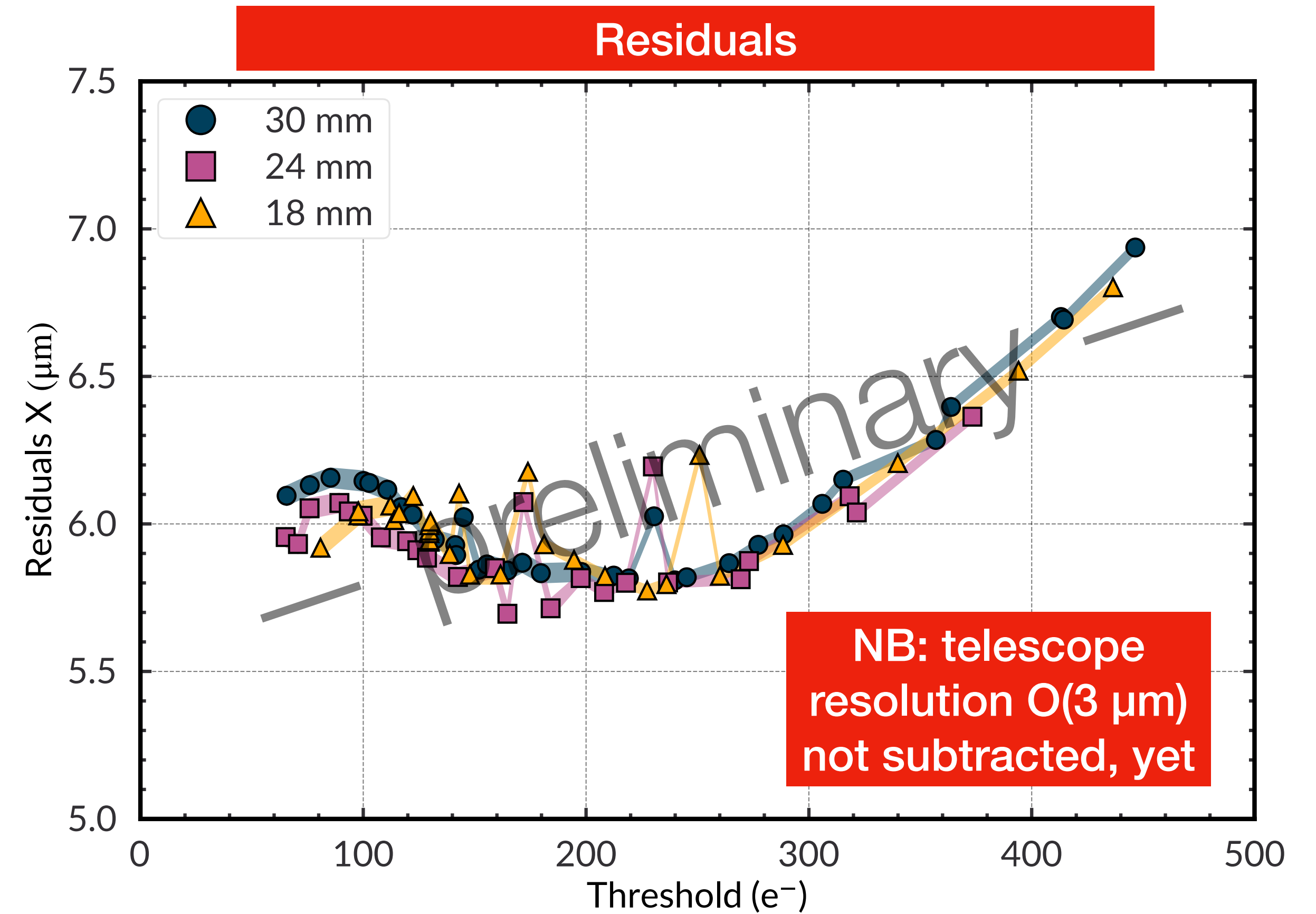
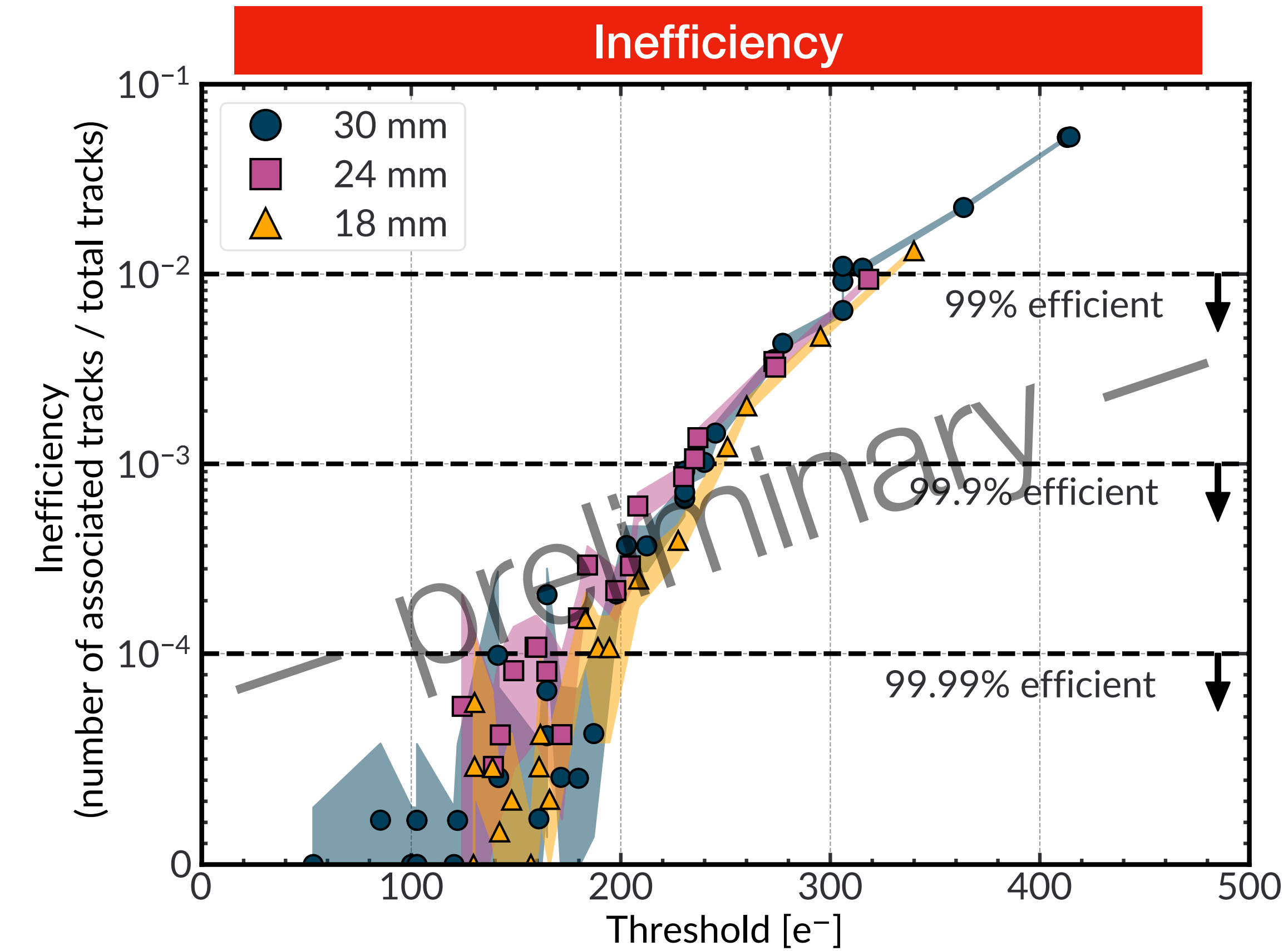
μ ITS3 X-ray tomography



beam
window
(only Si)

Bent ALPIDEs — beam test results

at all nominal ITS3 radii



Bent MAPS “just” continue to work! – bending is not visible in main performance figures

Main R&D lines towards ITS3

Ultra-light mechanics and cooling

- ▶ mechanical concept to hold thin sensors “without” material
 - development of assembly procedure
 - qualification of carbon foams
- ▶ verification and optimisation of air cooling concept

Thinning, bending, interconnection

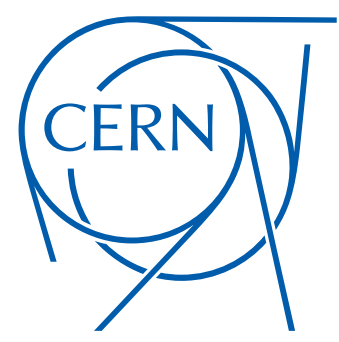
- ▶ development of procedures to handle and bend large thin chips
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- ▶ development of electrical interconnection to bent chips

Wafer-scale sensor development

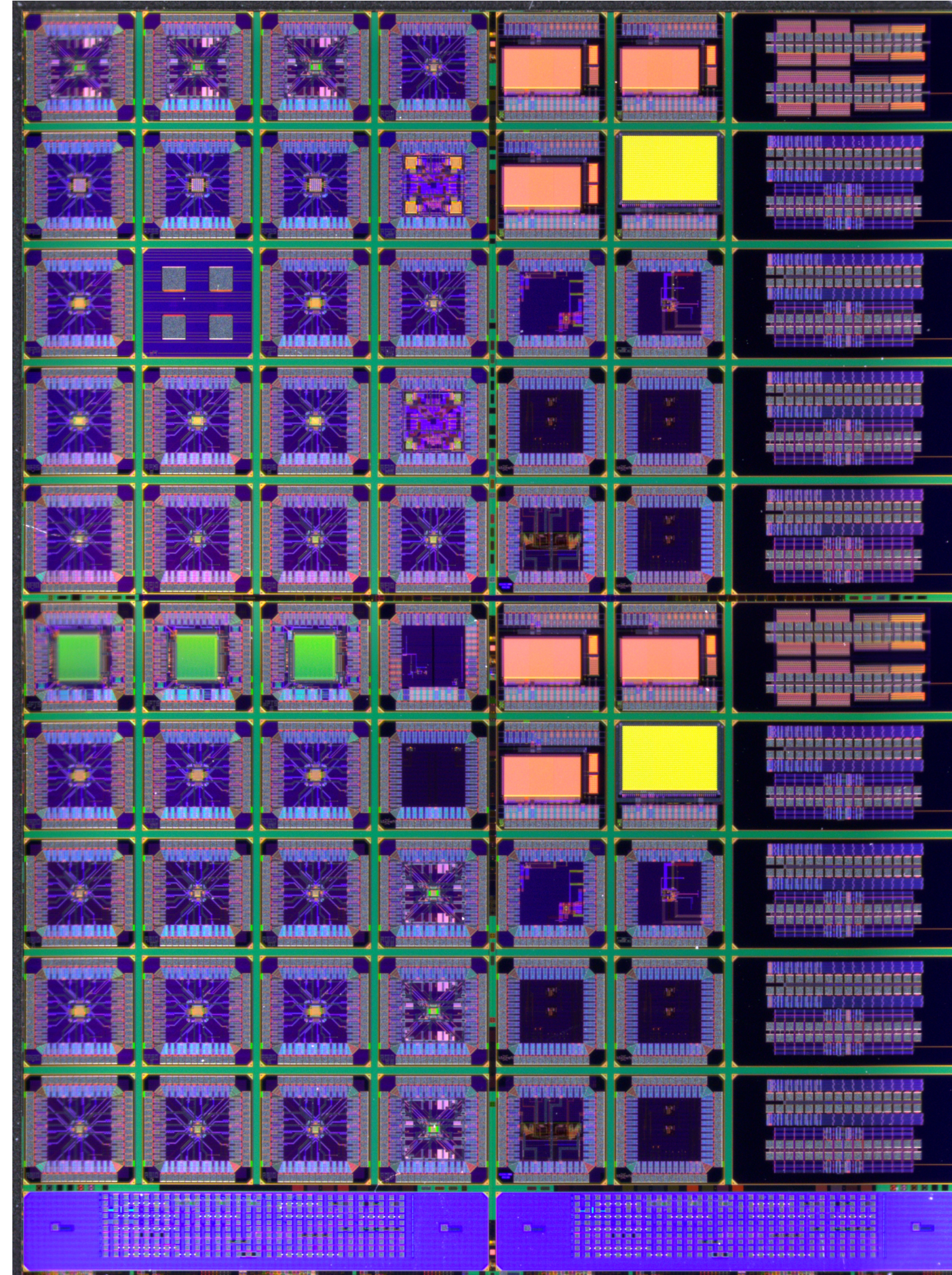
- ▶ switch to 65 nm technology (TPSCo)
 - verification of the technology for radiation tolerance and charge collection
- ▶ stitched sensor design
 - chip architecture
 - optimisation for yield

Sensor design: advancing the technology

qualifying the TPSCo 65 nm CMOS Imaging Technology

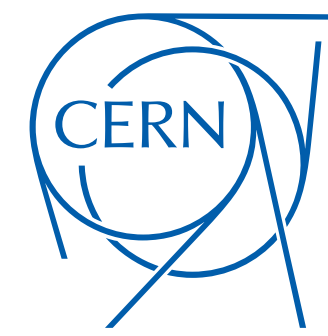


- ▶ Together with CERN EP R&D
- ▶ Leverages on experience with 180 nm process (ALICE ITS2 and beyond)
 - excellent links to foundry
- ▶ Comprehensive *first* submission: **55** prototype chips
 - different processing flavours were tried
- ▶ Immense dataset for ITS3 and the community at large



This technology has a large potential for the field, not only because it is done on 300 mm wafers!

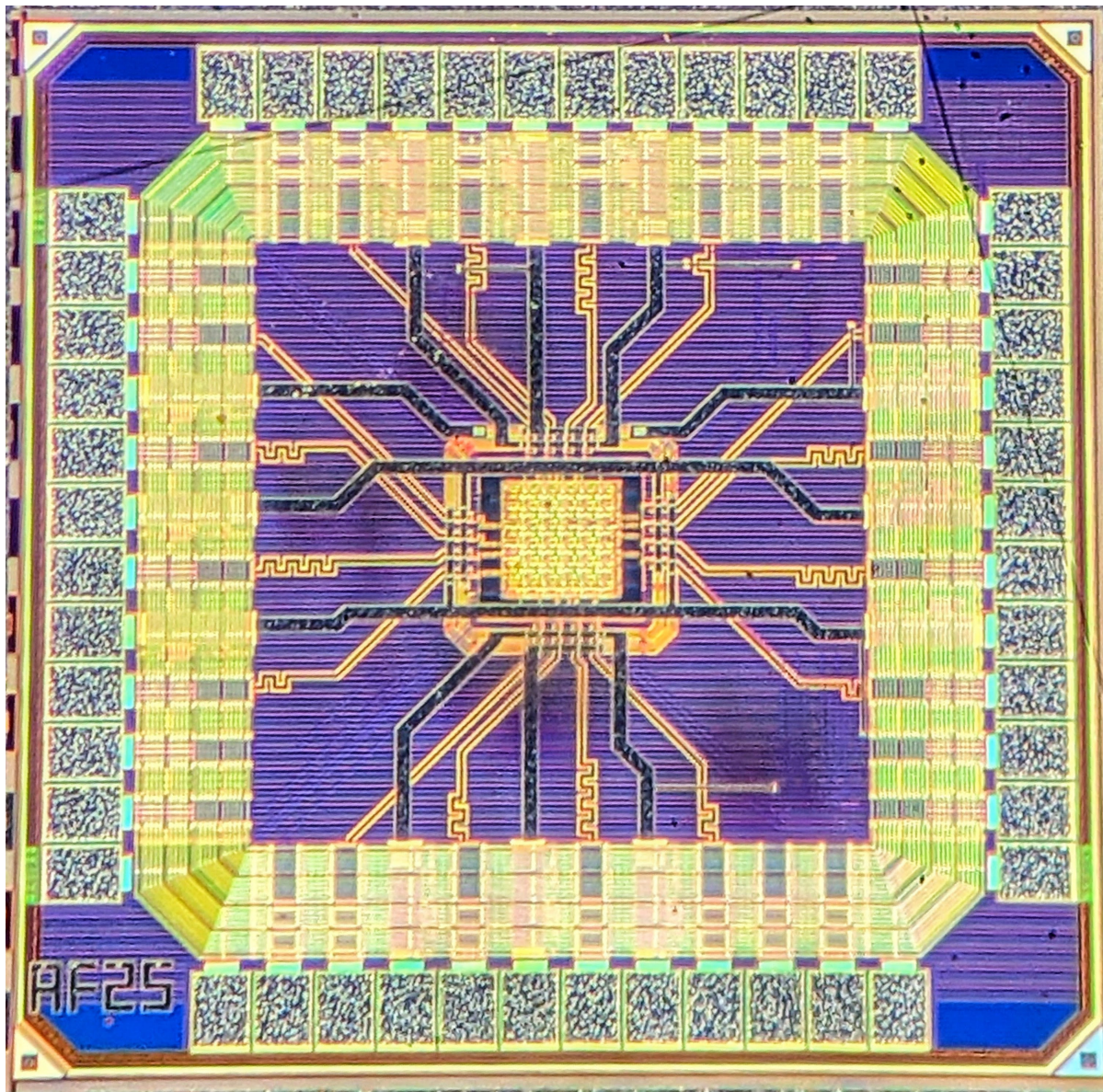
Pixel prototype chips (selection)



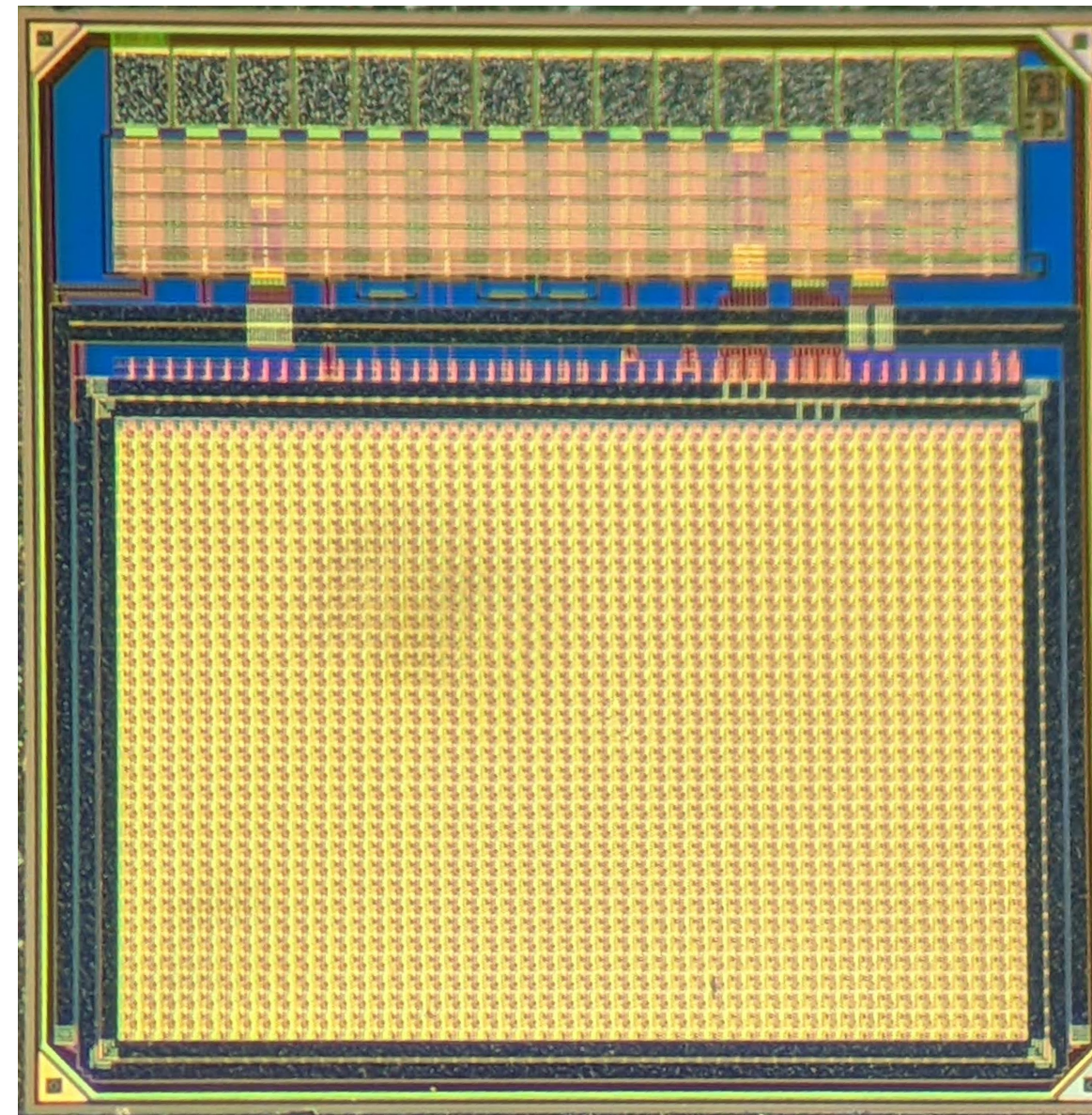
APTS

CE65

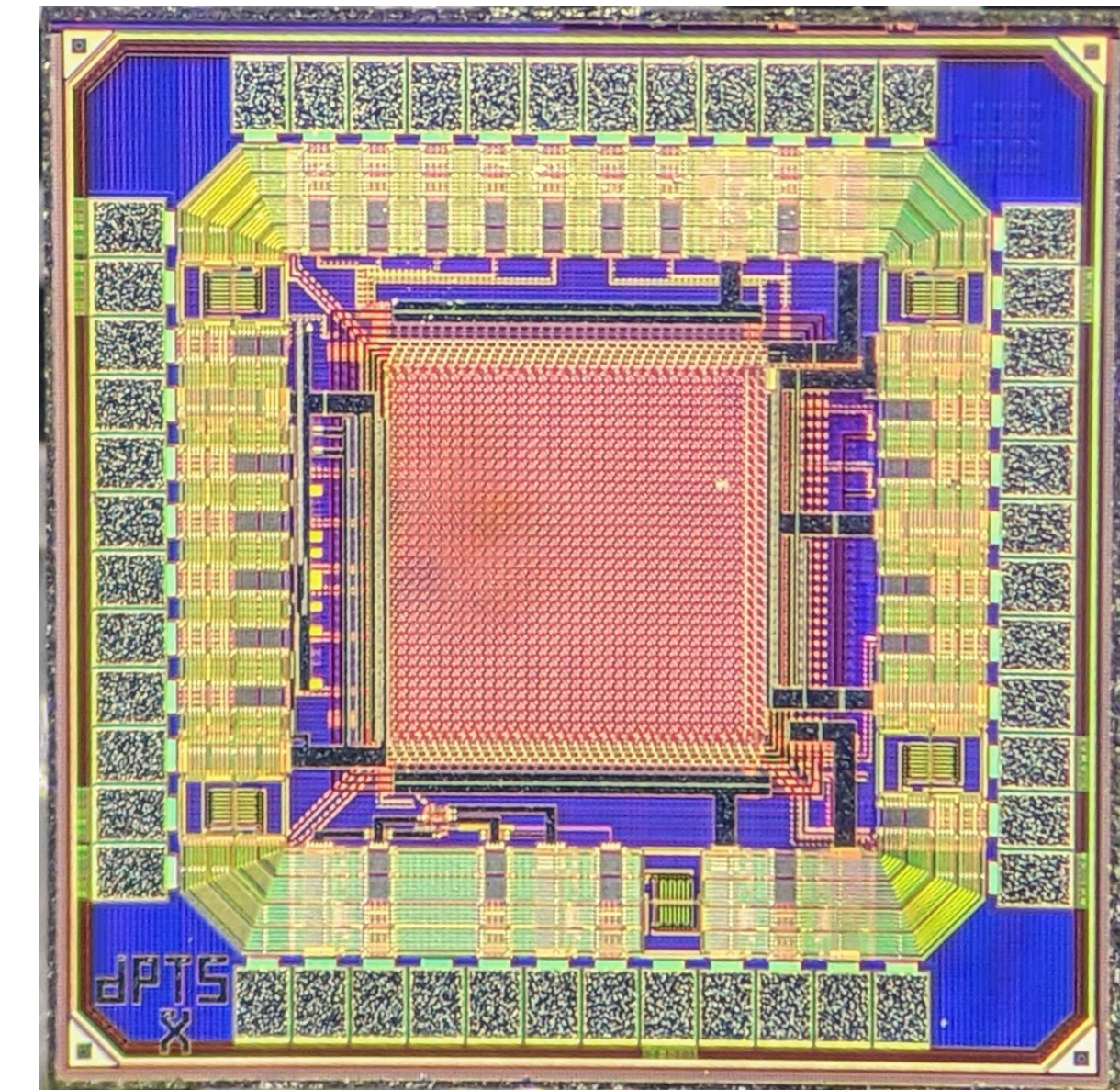
DPTS



- ▶ **matrix:** 6x6 pixels
- ▶ **readout:** direct analog readout of central 4x4
- ▶ **pitch:** 10, 15, 20, 25 μm
- ▶ **total:** 34 dies



- ▶ **matrix:** 64x32, 48x32 pixels
- ▶ **readout:** rolling shutter analog
- ▶ **pitch:** 15, 25 μm
- ▶ **total:** 4 dies



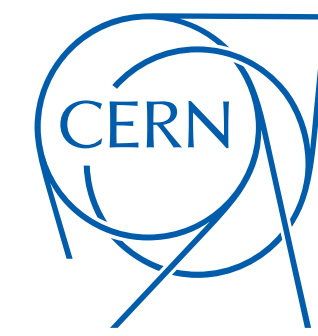
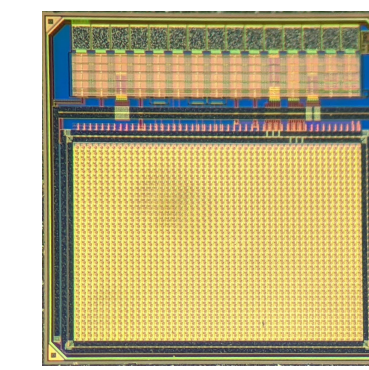
- ▶ **matrix:** 32x32 pixels
- ▶ **readout:** async. digital with ToT
- ▶ **pitch:** 15 μm
- ▶ **total:** 3 dies

Comprehensive set of prototypes and variants to explore the technology for particle detection

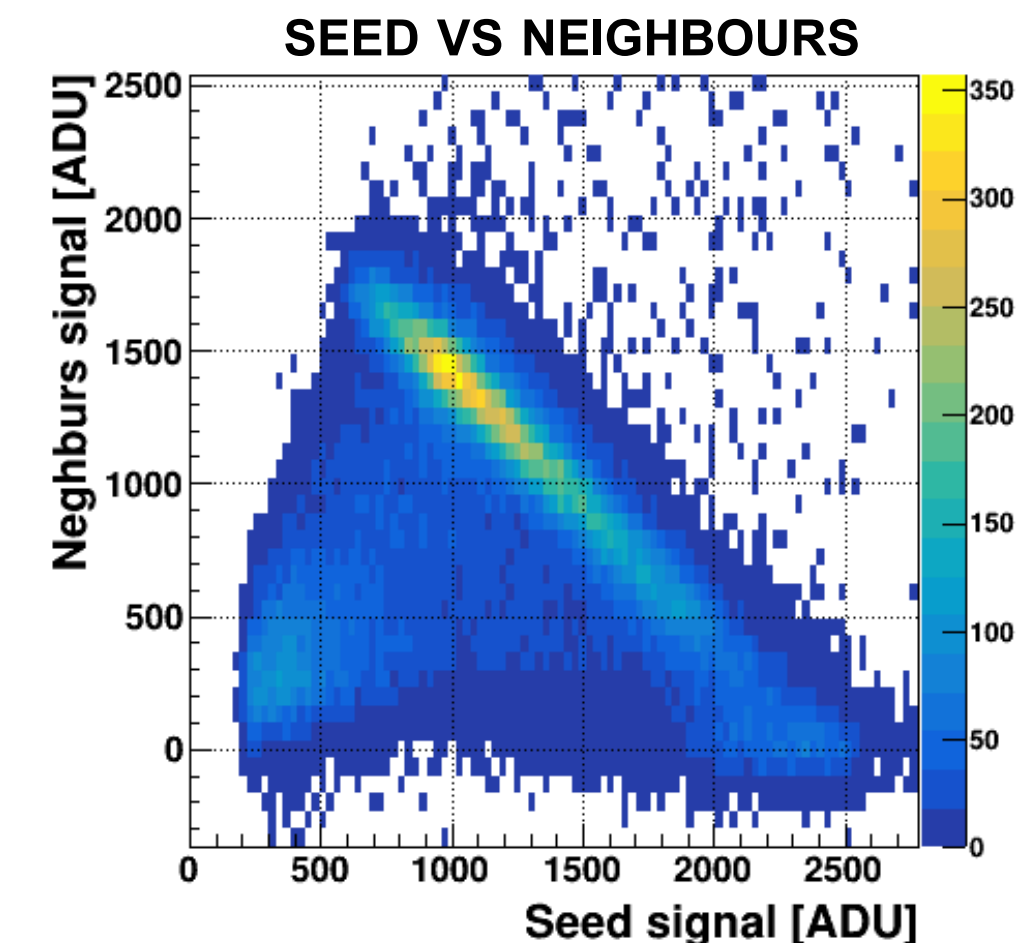
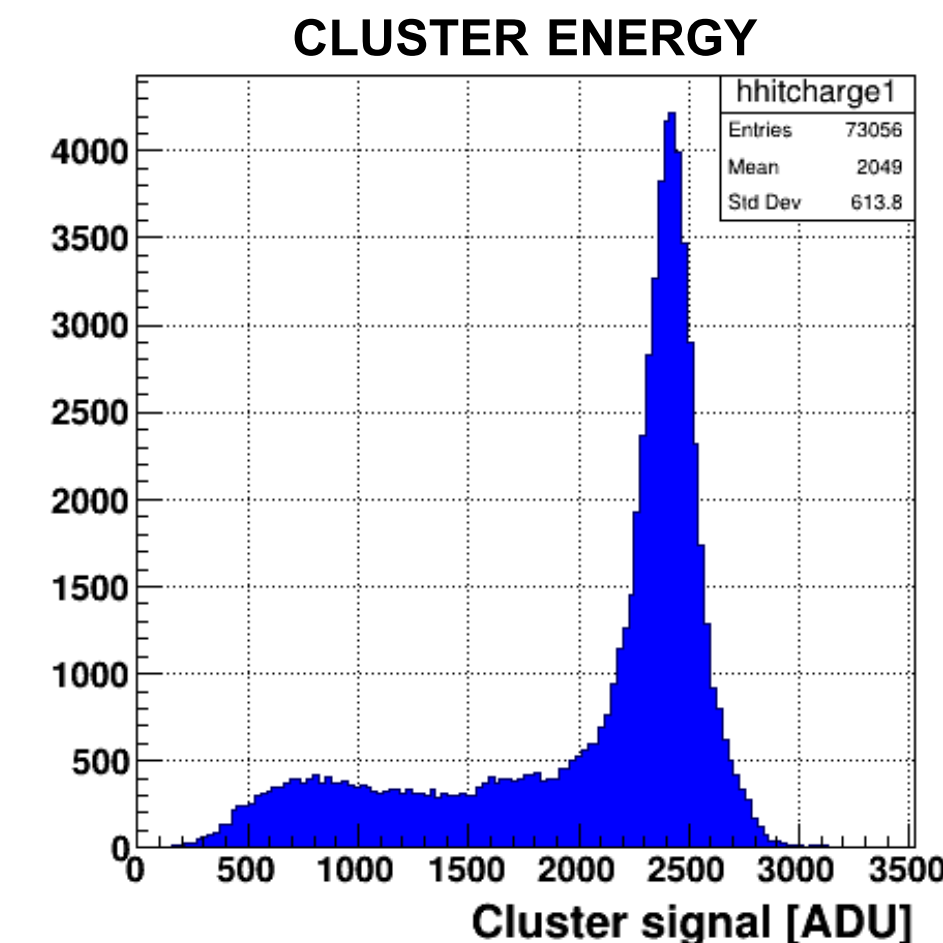
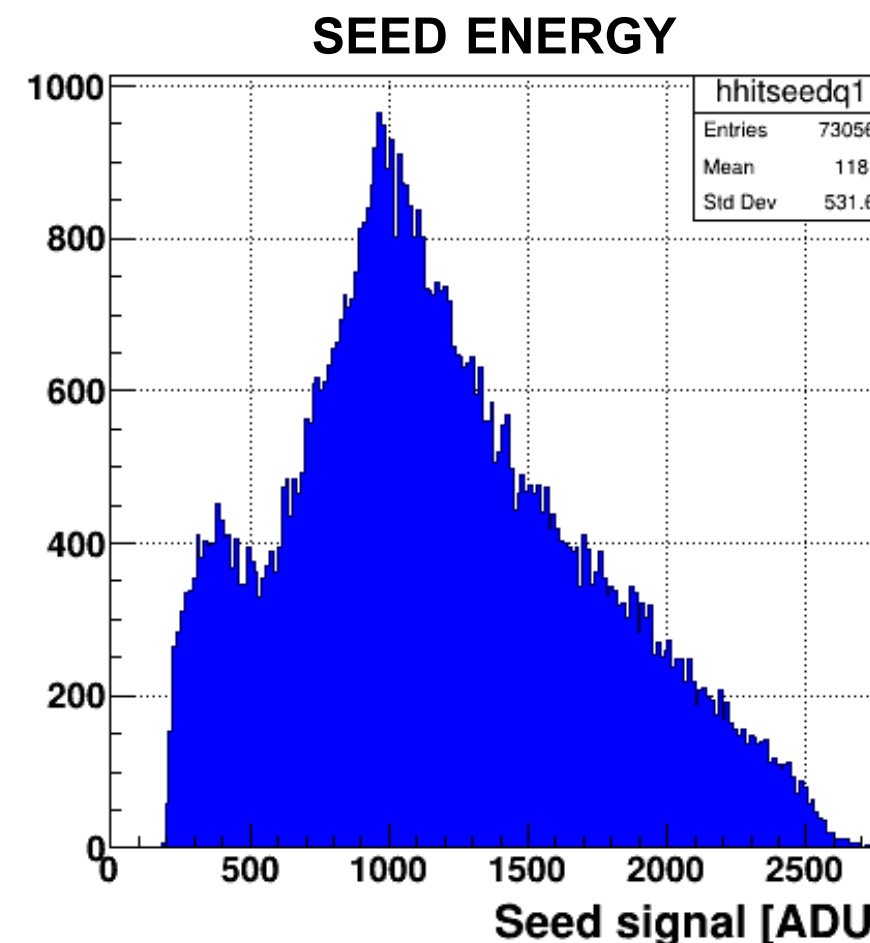
CE65 – Fe-55 lab tests

charge sharing

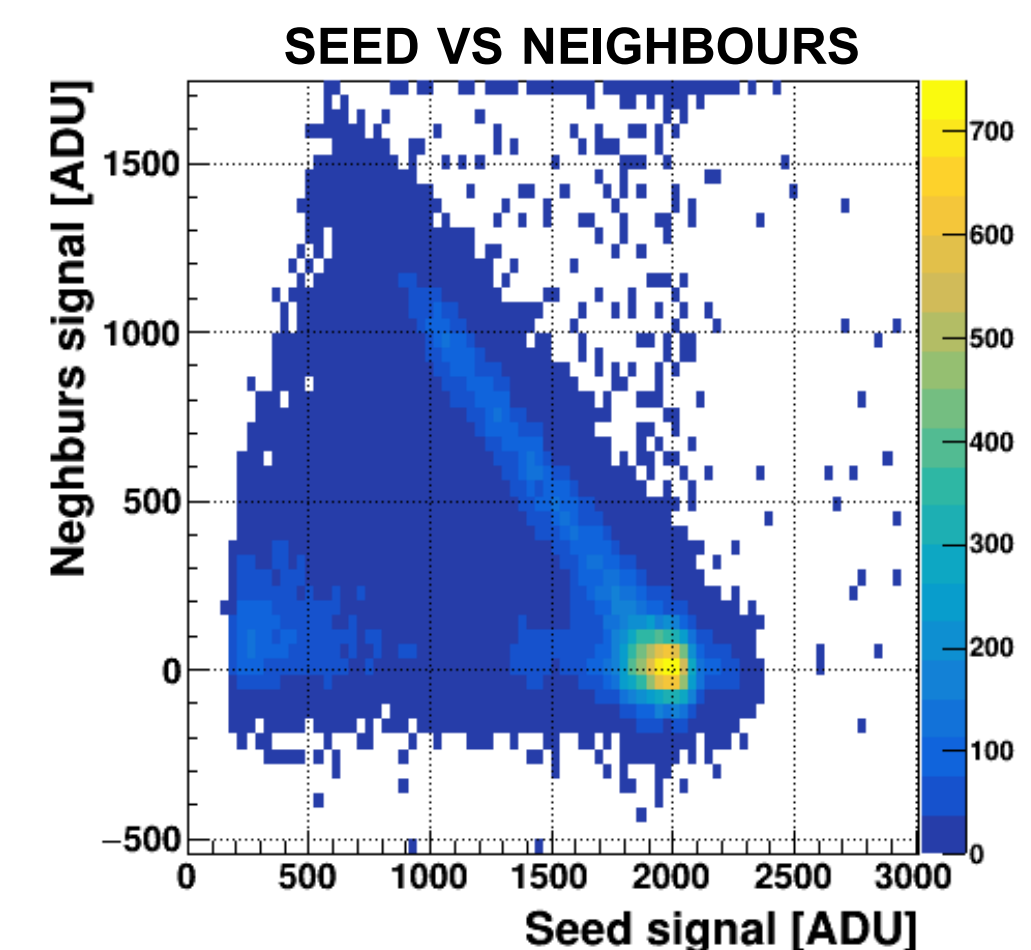
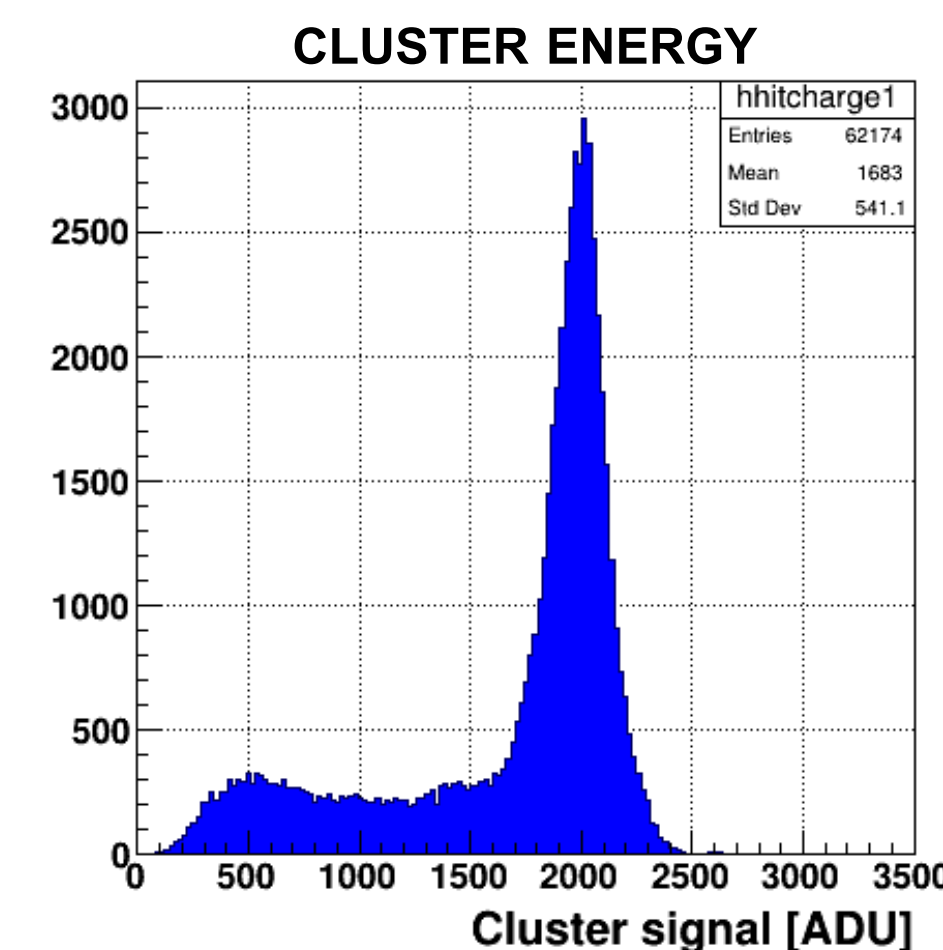
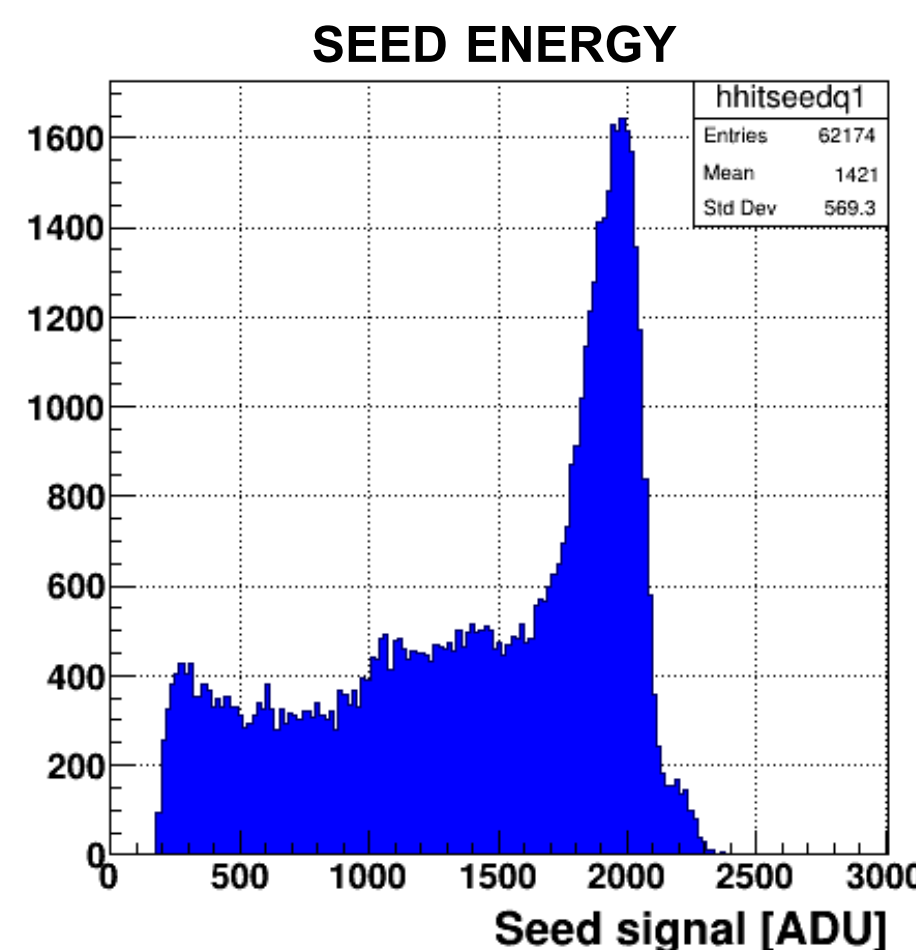
- ▶ Very good charge collection properties
- ▶ Effect of different optimisation can be seen very clearly
- ▶ Now being also verified
 - after irradiation
 - in beam tests



BASIC DIODE [A4]:

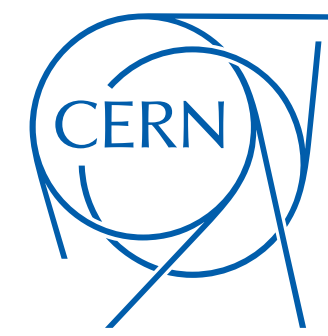
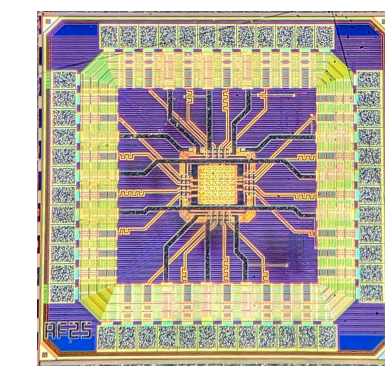


OPTIMIZED DIODE [B4]:

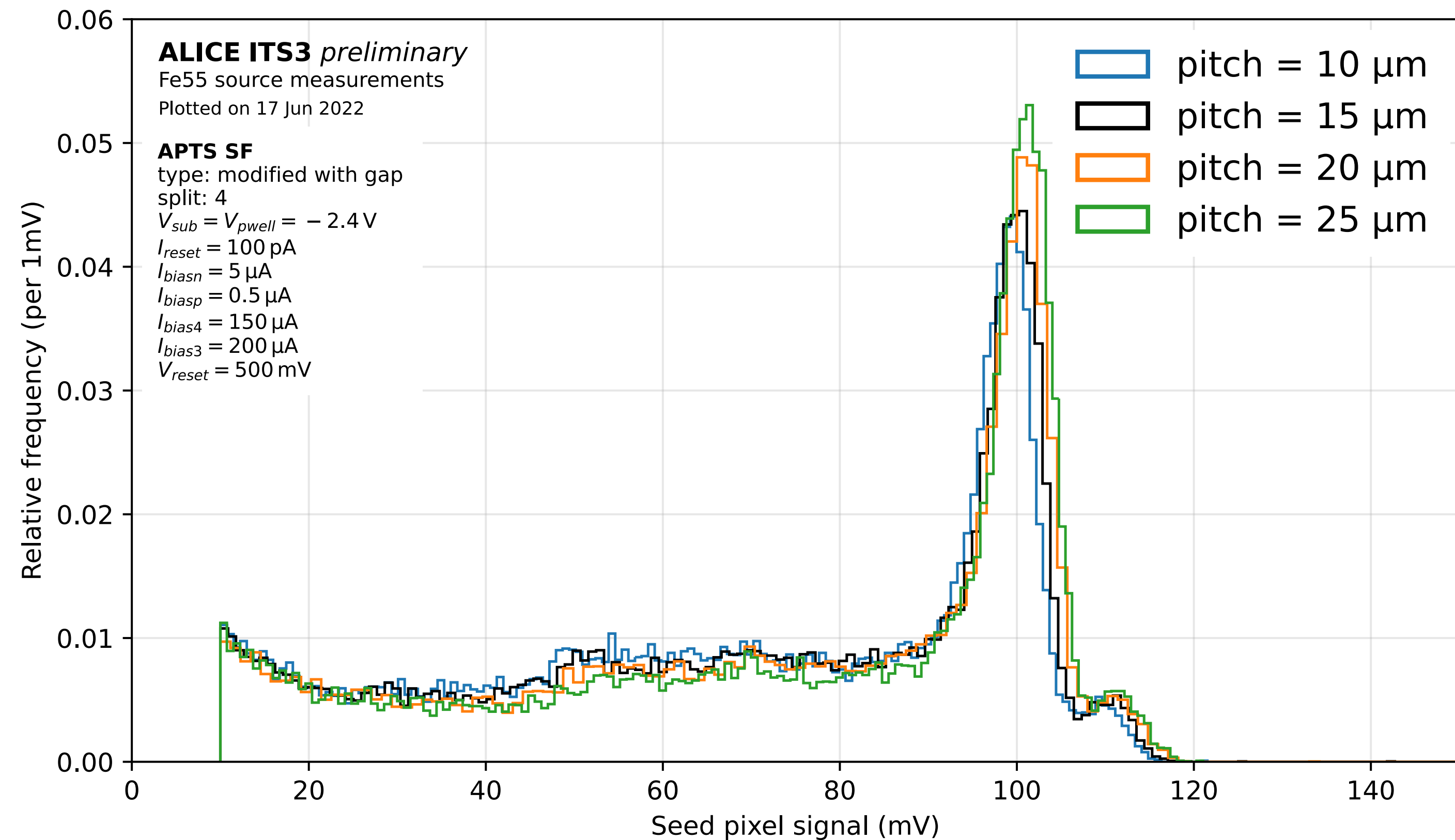


APTS – Fe-55 lab tests

comparison of pixel pitches



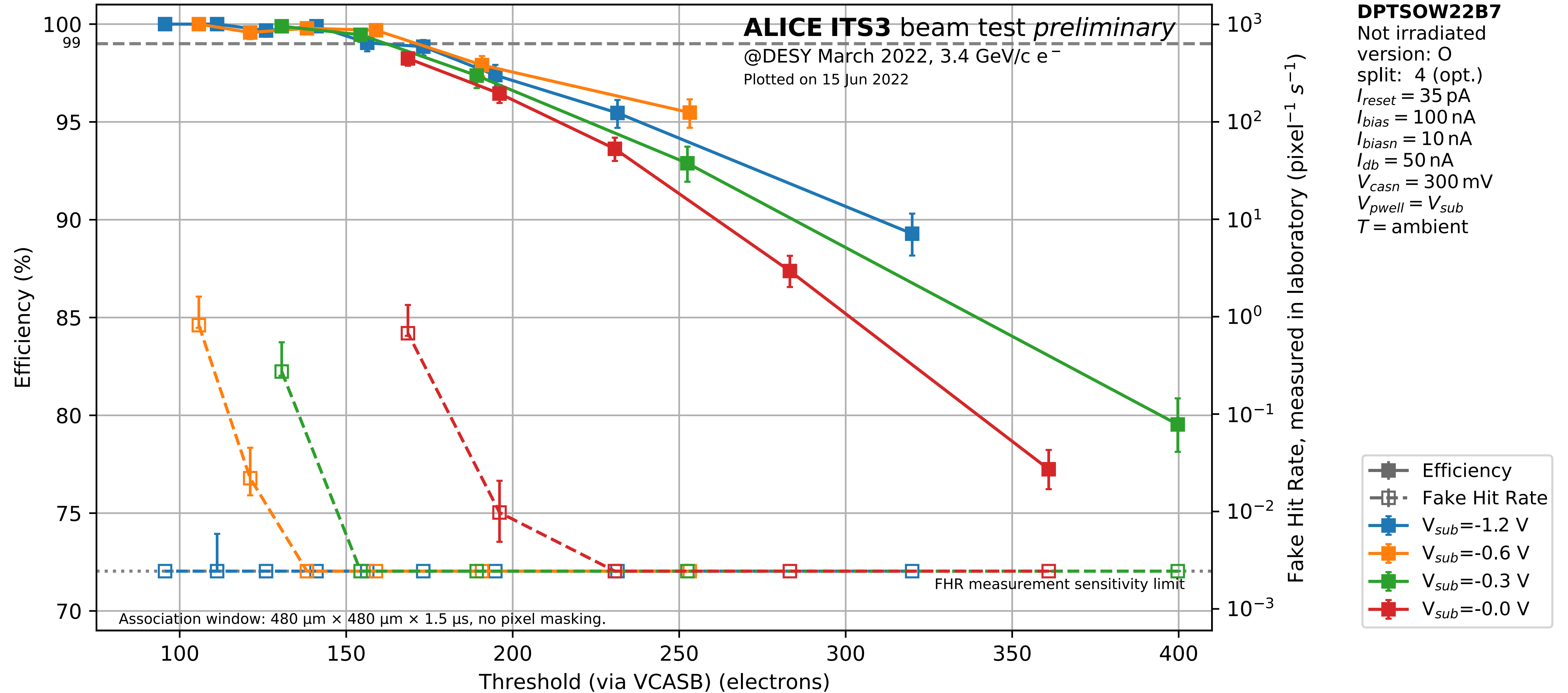
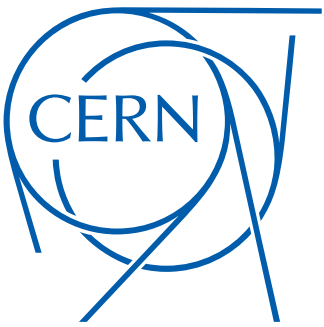
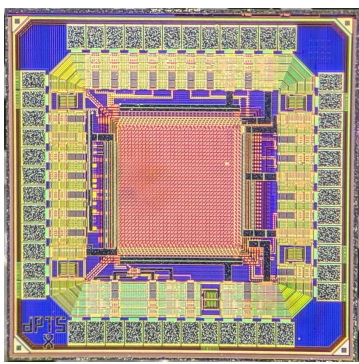
- ▶ Process modification was introduced:
 - full depletion of sensors
 - electric field pointing to collection electrodes
- ▶ Pixels of pitches of 10-25 μm show similar results
 - indicates that the charge collection is very efficient
- ▶ Allows to *choose* optimal pitch for the final sensor



This is a remarkable result — now being verified with beam tests

DPTS – beam tests

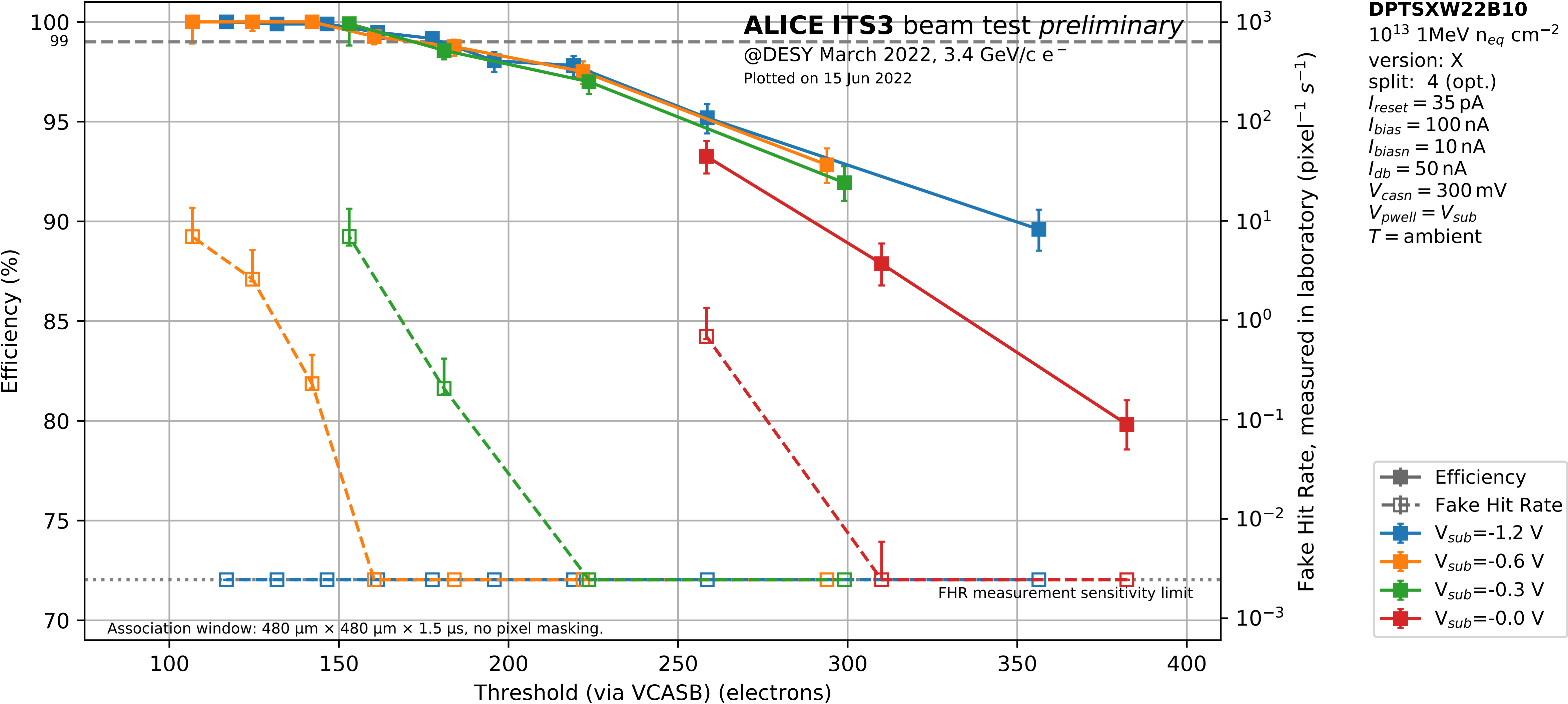
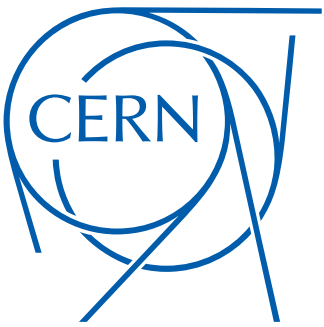
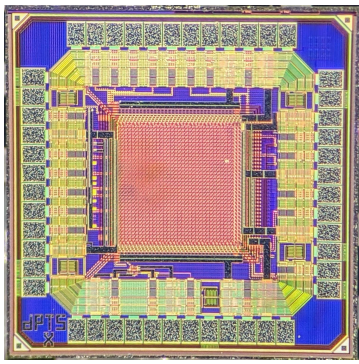
efficiencies and fake hit rates



Excellent detection efficiency at very low fake hit rates over large threshold range!

DPTS – beam tests

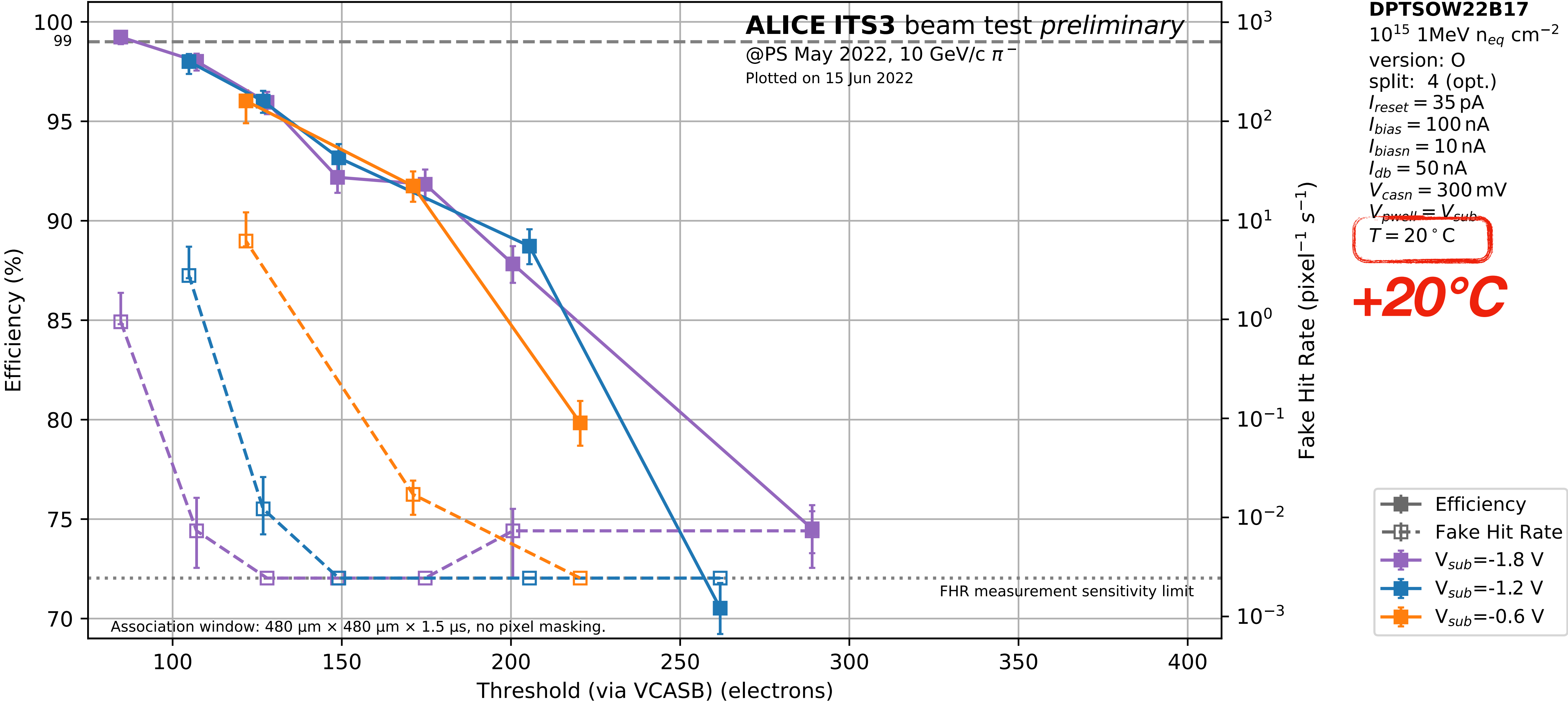
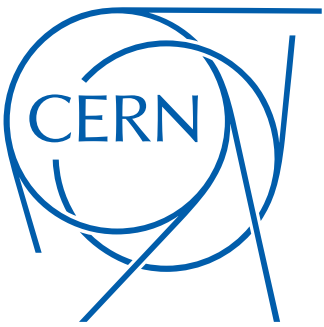
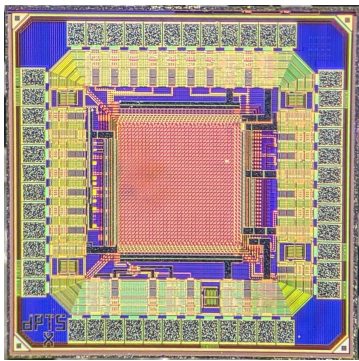
after irradiation: “ 10^{13} NIEL”



At ALICE conditions: slightly larger fake rates, but still large operational margin

DPTS – beam tests

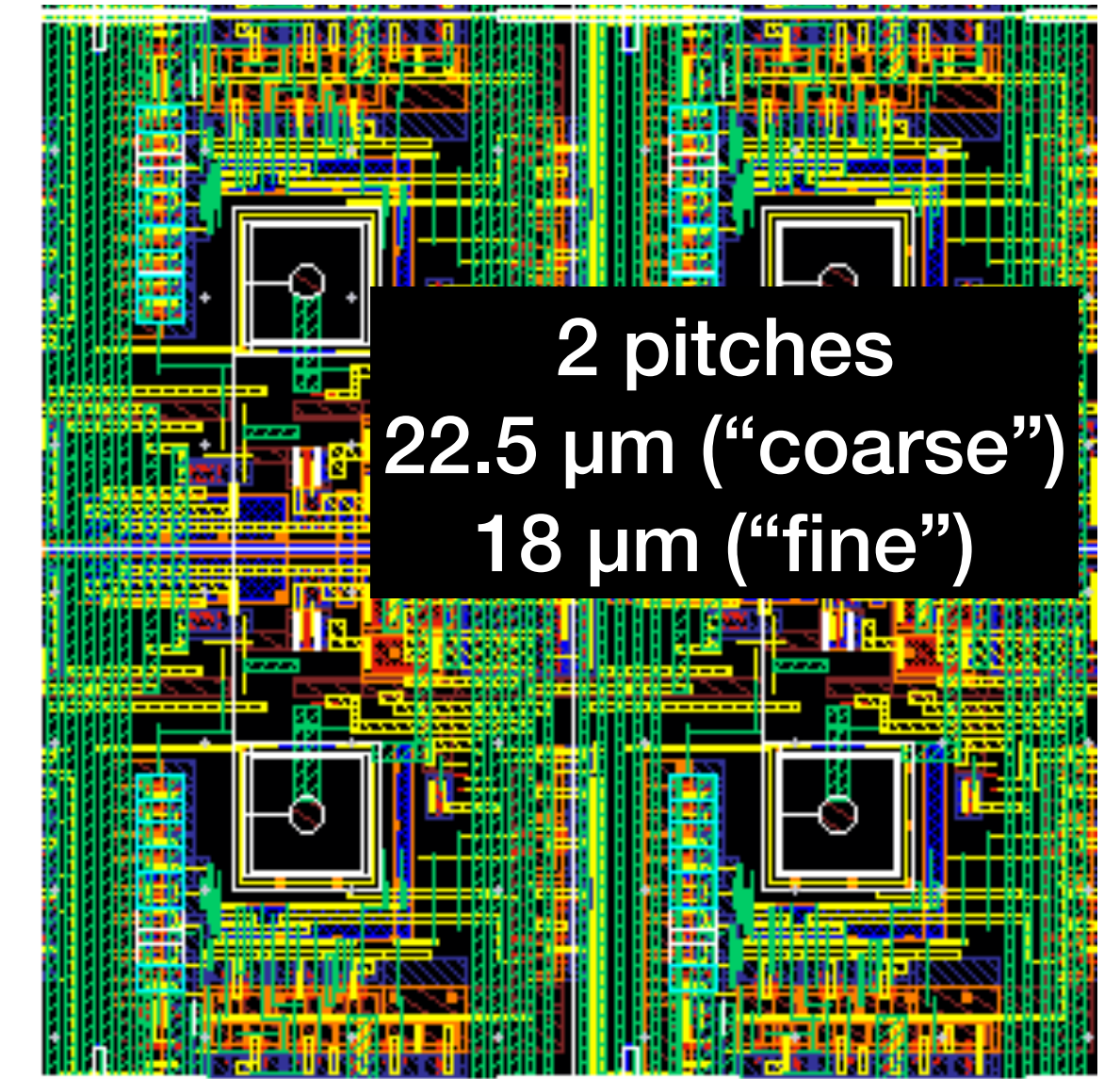
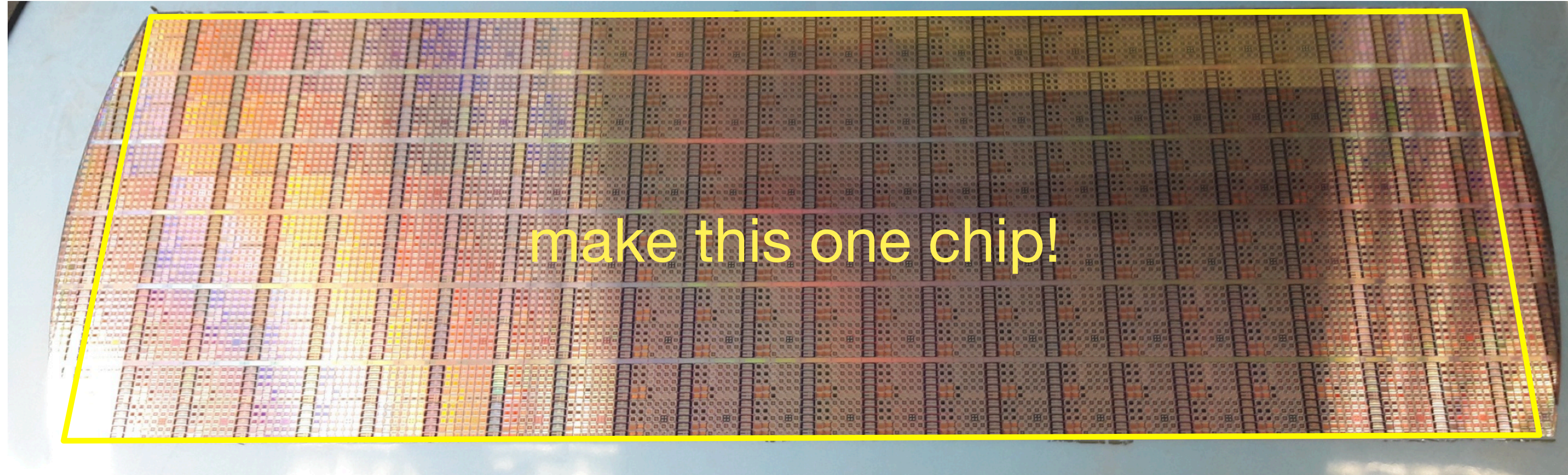
after more irradiation: “ 10^{15} NIEL”



At 10¹⁵: still possible to attain 100% detection efficiency at room temperature w/o being flooded in noise

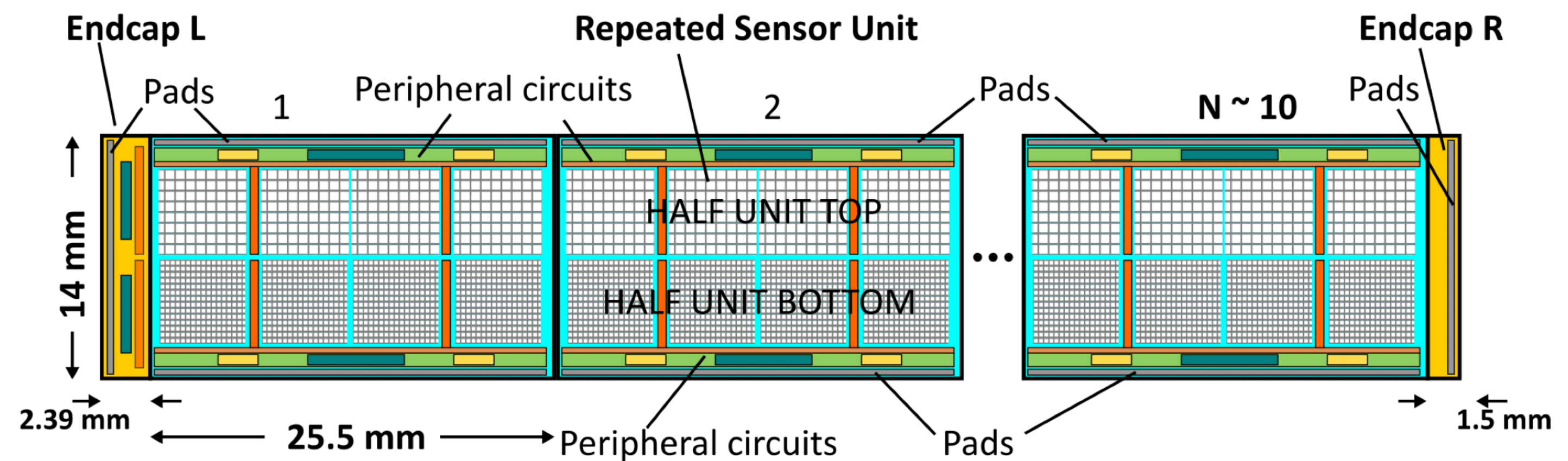
Next chip submission: stitching

- ▶ Next goal (submission this summer, “ER1”):



Requires dedicated design effort:

- understanding of “stitching” rules
 - incorporation of redundancy, fault tolerance
- ▶ Crucial exercise to understand:
- yield
 - uniformity



We are taking the next and last critical step!

Summary & Outlook



- ▶ **ALICE** is carrying out the R&D for a **new class** of vertex detectors
 - target: installation of new inner layers, **ITS3**, for LHC **LS3**
- ▶ Large improvement in tracking **precision** by:
 - new material budget record: **< 0.05% X_0** per layer
 - radial distance from IP: only **18 mm**
- ▶ **Advancing MAPS** technology towards:
 - deeper sub micron technology node: **65 nm**
 - wafer-scale sensors: **stitching**
- ▶ **Ultra-thin, bent, wafer-scale MAPS** are becoming a reality!
 - for ALICE ITS3, *and beyond!*

→ next talk:
Nicolo Jacazio
ALICE 3

Thank you!

