CAEN Electronic Instrumentation

Tools for Discovery

Power electronics in HEP experimental caverns

FERDINANDO GIORDANO
ON BEHALF OF THE POWER SUPPLIES R&D GROUP

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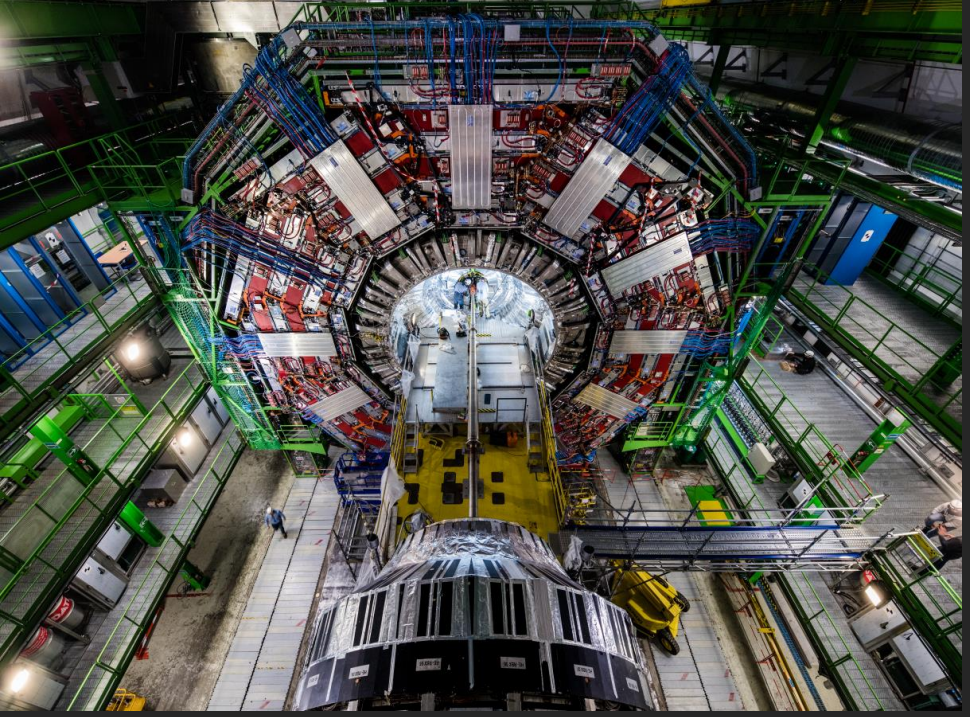
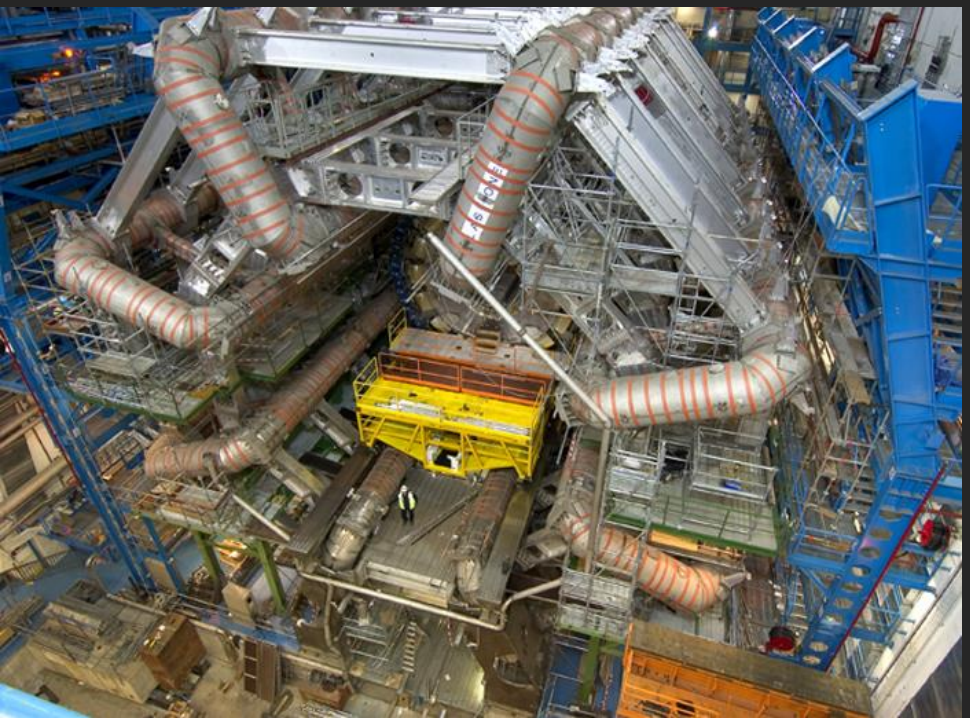
Summary

- The HL-LHC and the experimental caverns
- Technical solutions
- Irradiation campaign and radiation damage
- Magnetic field resilience

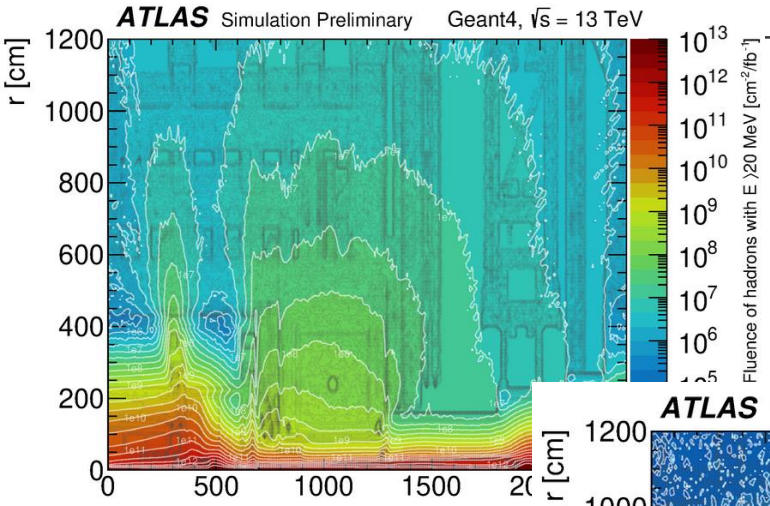


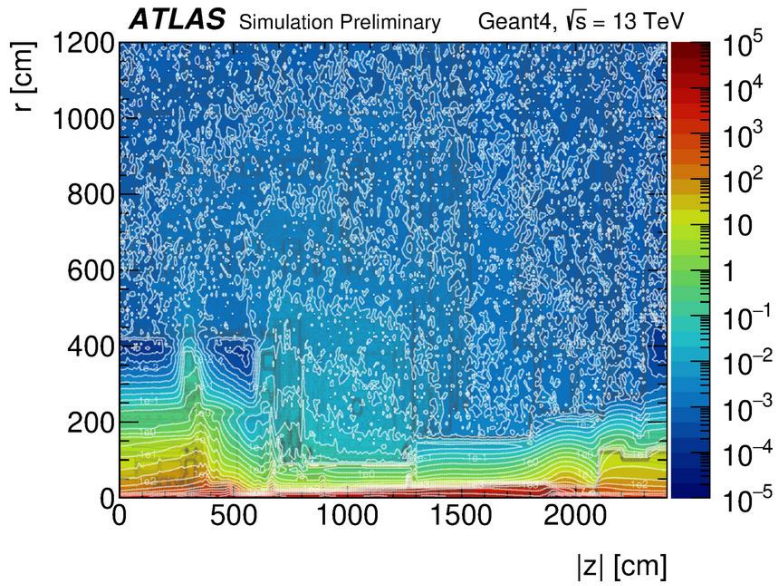


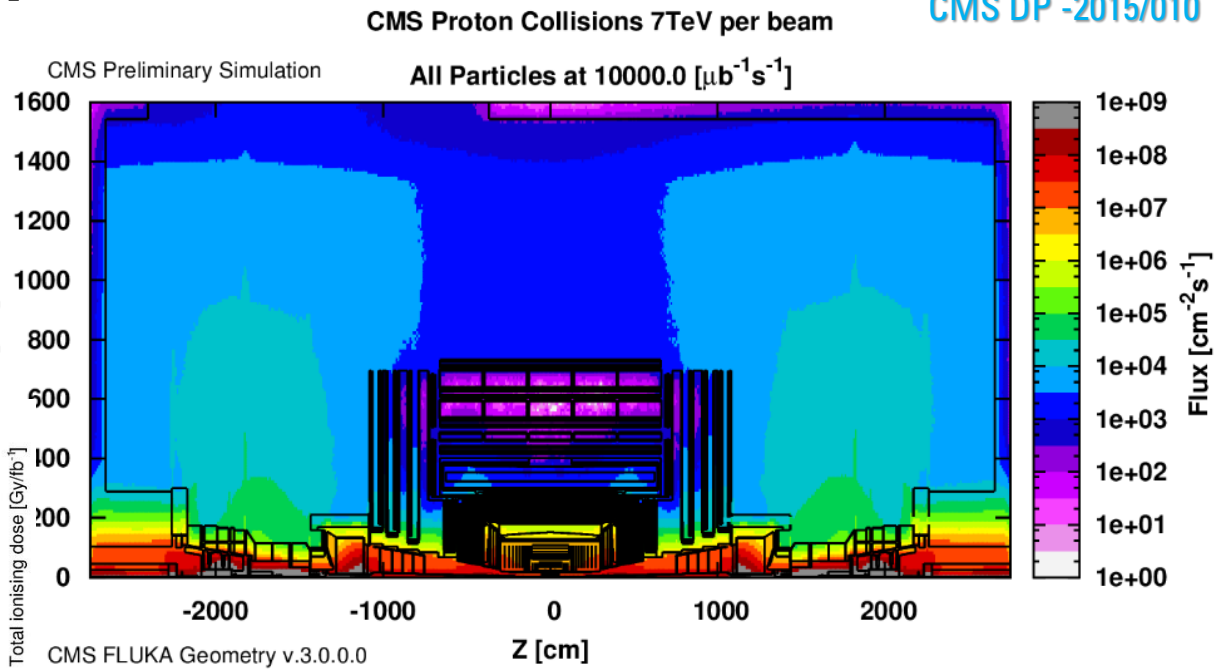
High Energy Physics experimental caverns

Some physics experiments are placed inside caverns located underground; Ohm’s law and their dimension call for power supplies to be placed as close as possible to detectors. On the other hand, in the detector proximity residual magnetic fields and various radiations are often found.

Hostile environment requirements

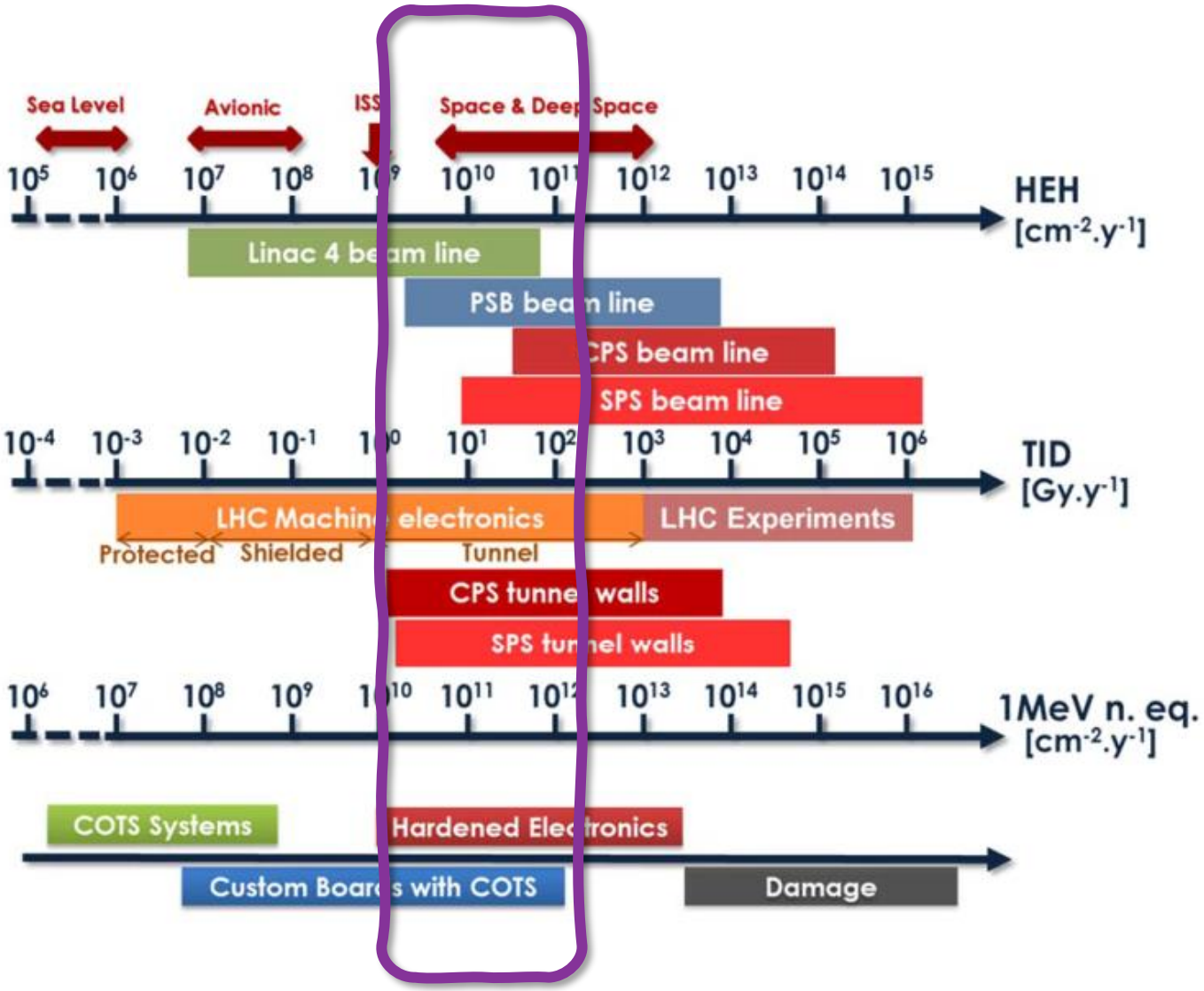






CMS DP -2015/010

AtlasPublic/RadiationSimulationPublicResults



credits to Andrea Coronetti talk at R2E annual meeting

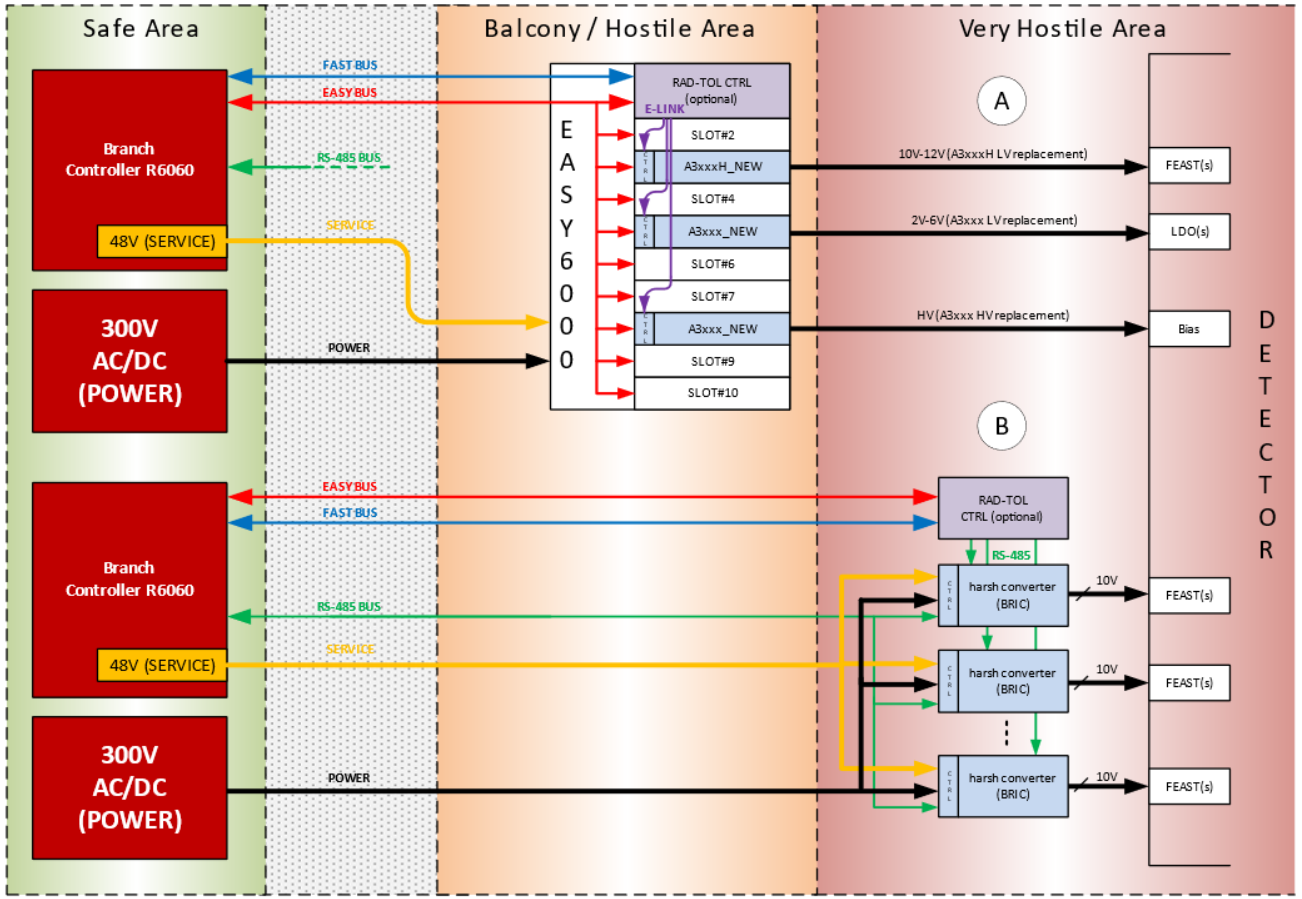
Electronics for HL-LHC

Examples of TID, DD, and HEH for HL-LHC.

Our range of interest is marked in the violet square, at the edge of the custom boards with COTS.

To be noticed that the LHC experiments are higher because the radiation is higher at the interaction point, not where the power supplies are generally located.

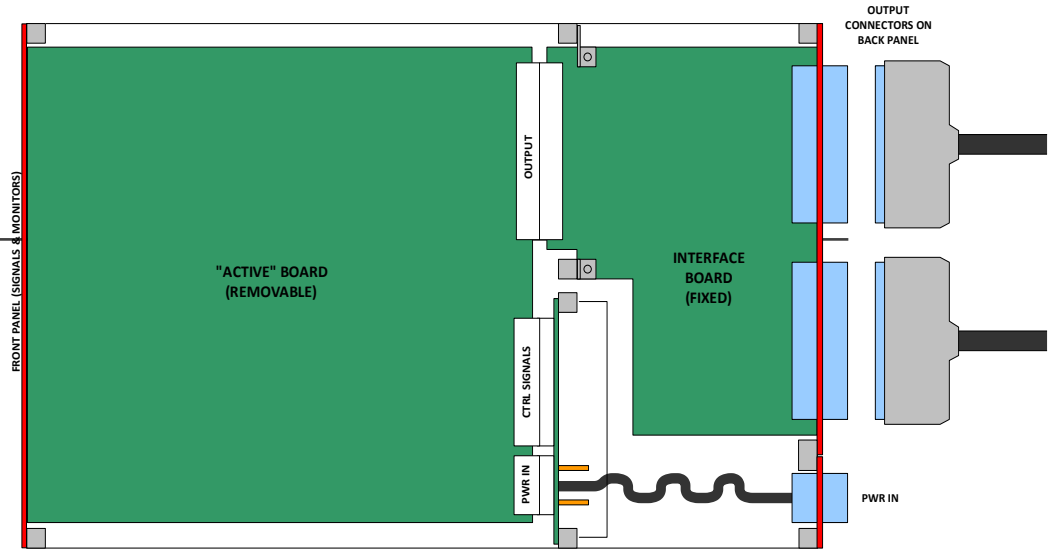
The EASY concept



- **Extremely flexible architecture,** allowing more configurations than the previous generation
- New harsh converters for **Very Hostile Area** (>200 Gy) to be placed closer to the detector (~m) optimizing cable power loss
- New **faster connection** to DCS thanks to the brand new R6060 branch controller with Gb Ethernet
- New **faster connection** to the EASY remote boards thanks (CAN for back-compatibility, SFP+ for high-bandwidth, RS-485 for robustness and easy implementation.
- **More power** thanks to a ~360V bulk power line from service to experimental caverns:
  - 6x higher voltage -> 6x less current -> much less cable area to have the same power efficiency or much better power efficiency keeping the same cables

EASY operation

- The boards will be **adaptable** via a back/interface-board to various cable types
- The back/interface-board will ensure an easy and fast swap between boards, so the maintenance time spent in Controlled Radiation Areas is minimal according to the **ALARA principles**



The **safety of the system** is granted thanks to many precautions:

- Careful component and system tests in hostile environment (several MOSFETs, BJTs, PWM ICs, analog ICs, Vref, Opamp, Data converters, Drivers,… tested during last 3 years in H.E.)
- Robustness of the most delicate circuits ensured by design (component de-rating, selection of best circuit topologies, proper devices biasing strategy,…)
- Redundancies where needed (both in HW, FW and SW)
- Advanced Diagnostics: sensors and on-board algorithms to predict and avoid failures

Test campaign

We undertook a test campaign on various irradiation facilities **testing** electronic **components** and **assemblies** before testing **whole** power supplies **boards**.

Various irradiation facilities were selected (many thanks to RADNEXT), able to provide neutrons (DD), protons (SEE) and gamma (TID). Thus, we could test different radiation damages and see how the boards would react to these effects.

The resilience to magnetic fields was also tested, in these case we studied how the orientation of the field with respect to the principal electronic components would affect the efficiency of the boards establishing its operational range. We performed these tests at CERN and at INFN-LASA with large electro-magnet capable to reach 1 T.

Irradiation facilities

PSI – 200 MeV protons:

- We had two irradiation nights, eventually more than we had been promised
- One single setup with two boards diagonally to the beam line (V-shape)
  - Various points across the two nights from 1E6 p/cm^2/s to 1E8 p/cm^2/s (also 2E8 to kill a micro)

Thanks to Rudy and PSI

NPI-CAS – 0-30 MeV neutrons:

- One full irradiation day
- One "sandwich" setup with all boards
  - One step of various time for each order of magnitude from 1E5 n/cm^2/s to 1E9 n/cm^2/s

Thanks to Mitja and his team

JYU – 55 MeV protons:

- We had two irradiation days
- Three different setups, 9 h beam time for each:
  - 3 hours at 1E6 p/cm^2/s -> 3 hours at 3E7 p/cm^2/s -> 3 hours at 1E8 p/cm^2/s

Thanks to Heikki and the whole JYU physics dept.

Irradiation facilities

ENEA – ^{60}Co ~ MeV gamma:

- We had three experimental setups and three irradiation days
- The limitation was the number of cables and diagnostic modules available.
  - Reached and exceeded 200 Gy, during the day low rate to simulate operations while in the night higher rate to integrate the required total dose

Thanks to Calliope and FNG teams

TIFPA – 140 MeV protons:

- Two irradiation evenings
- A single setup with HV channels and controller
  - The goal was to integrate at least 1E9 p/cm^2, to avoid discharges we ran at 1E7 p/cm^2/s

Thanks to Enrico and Daniele for organizing the test

CHARM – mixed fields:

- We had two irradiation weeks before 2020 for the ATLAS NSW project
- Simulated one of the most stressful HL-LHC environment:
  - 1E12 p/cm^2 – 6E12 n/cm^2 – 200 Gy

Thanks to CERN and Salvatore

Briefing on radiation damage

We can divide the radiation damage into to main groups:

- Total dose
- Single Event

Total dose: it might be of different kinds, but it is fundamentally deterministic, and it depends on the total adsorbed radiation. Testing for resilience to TID and DD is relatively simple since a single device is already representative of the final setup.

Single Events: they might be due different processes and affect the electronics in many ways (either temporary or permanently); single events are probabilistic and therefore in large setups these must be scaled accordingly.

General test setup

Irradiation area

Control room

DUT

Adapter Board

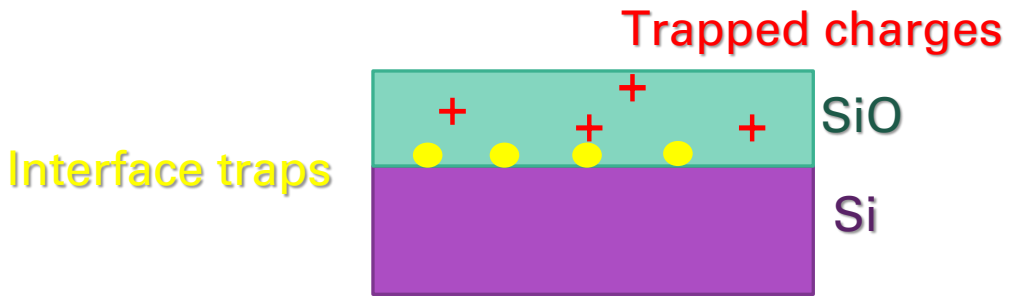
Picoscope

Logger

PW supplies

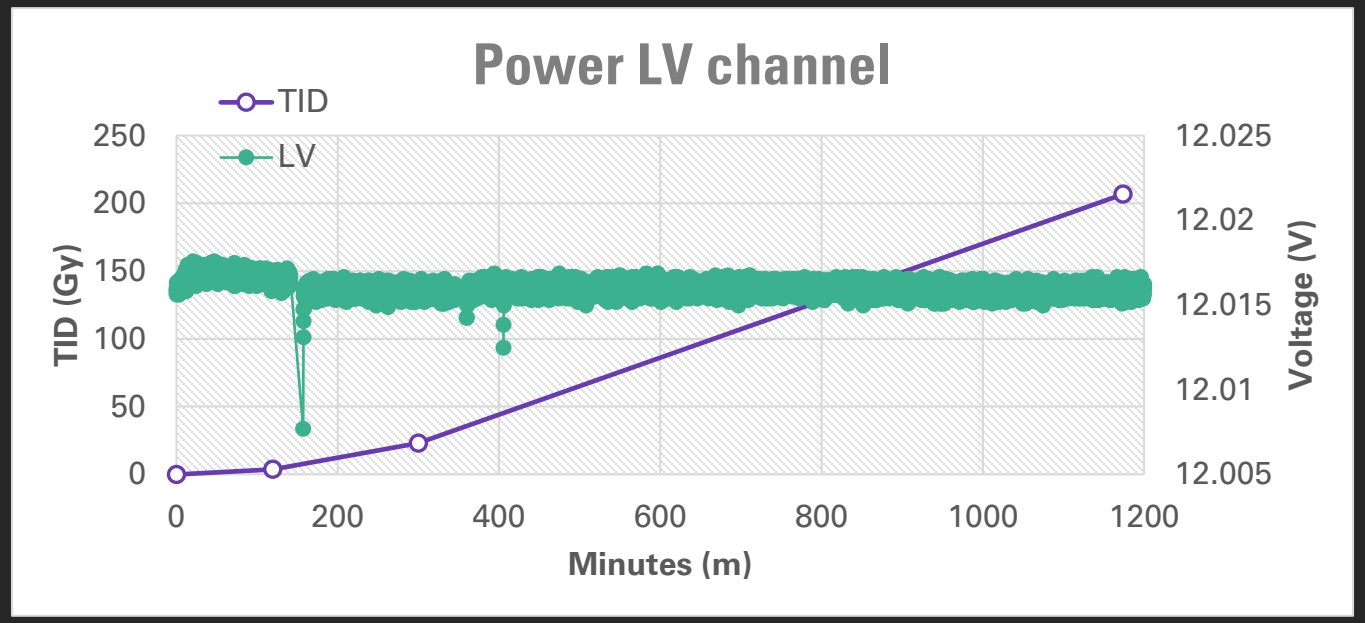
Total Ionizing Dose

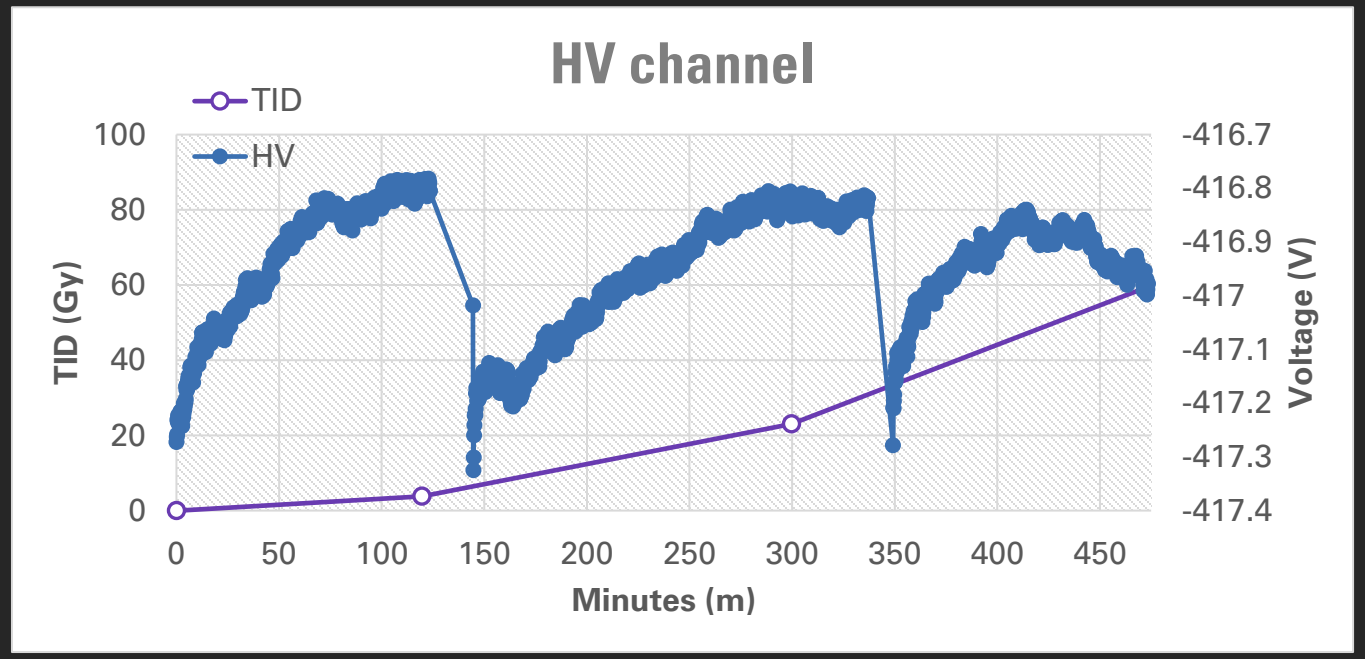
The TID indicates the **cumulative damage** by ionizing radiation. To extensively test against these effects, we used gamma rays as they are less likely to cause other damages in the silicon, but all charged particles can ionize.

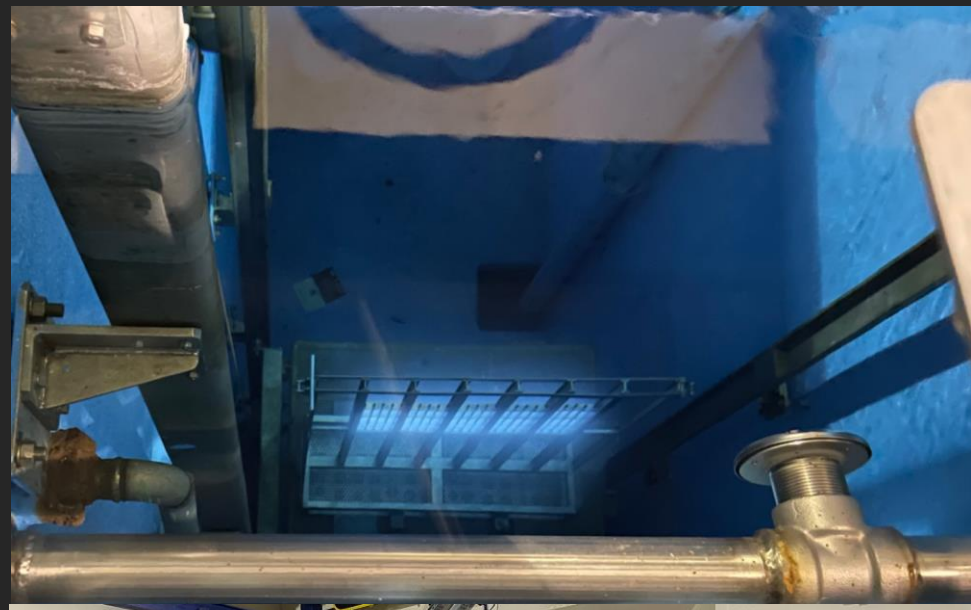


Some of the damage is recovered if irradiation stop (annealing).

MOSFET are particularly sensitive to TID as more and more charged are trapped in the oxide, eventually a transistor is incapable to turn OFF at V_{gs} = 0 V (depletion mode).

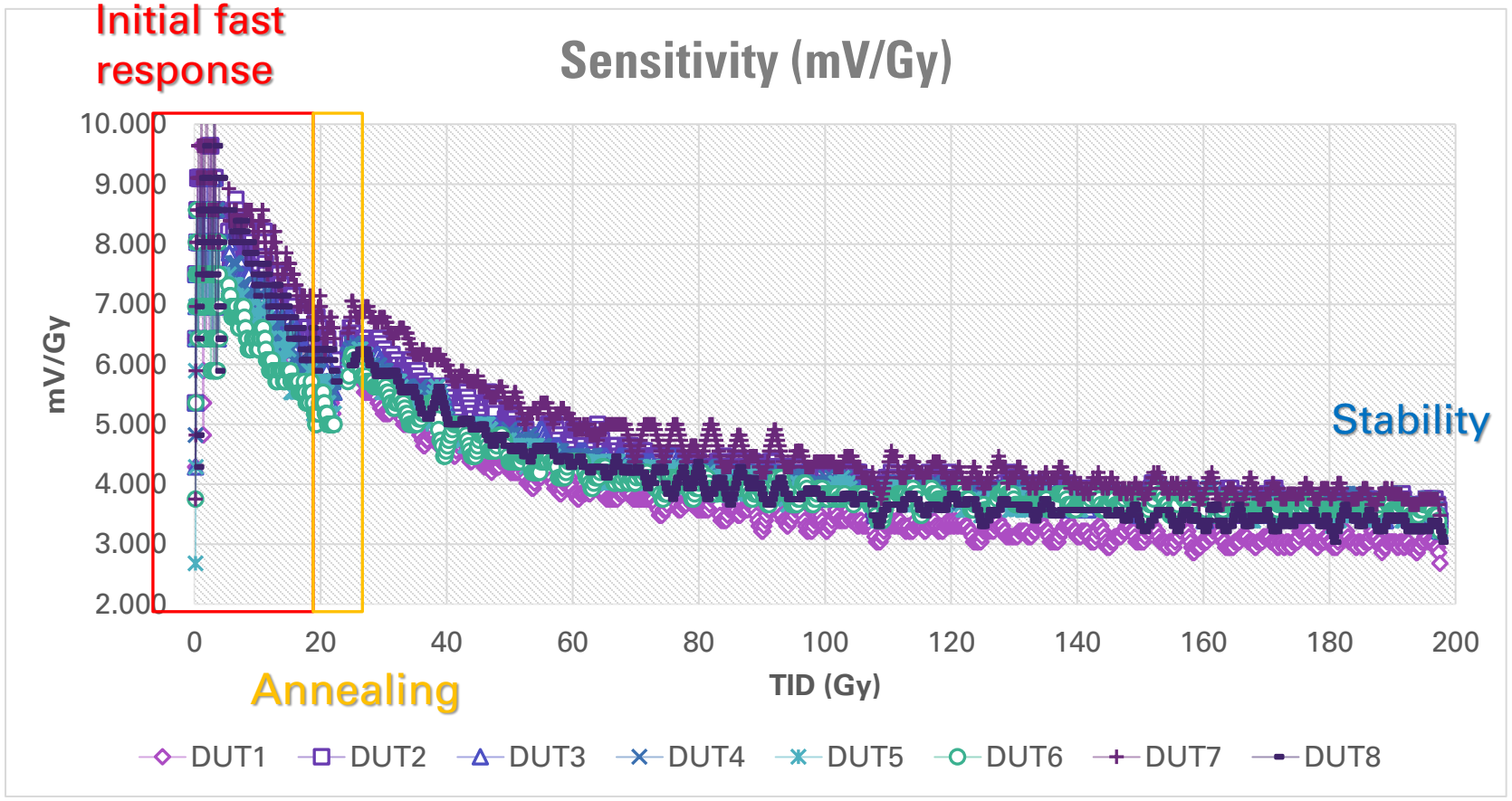

Power LV channel
TID
LV
250
200
150
100
50
0
TID (Gy)
12.025
12.02
12.015
12.01
12.005
Voltage (V)
0
200
400
600
800
1000
1200
Minutes (m)


HV channel
TID
HV
100
80
60
40
20
0
TID (Gy)
-416.7
-416.8
-416.9
-417
-417.1
-417.2
-417.3
-417.4
Voltage (V)
0
50
100
150
200
250
300
350
400
450
Minutes (m)



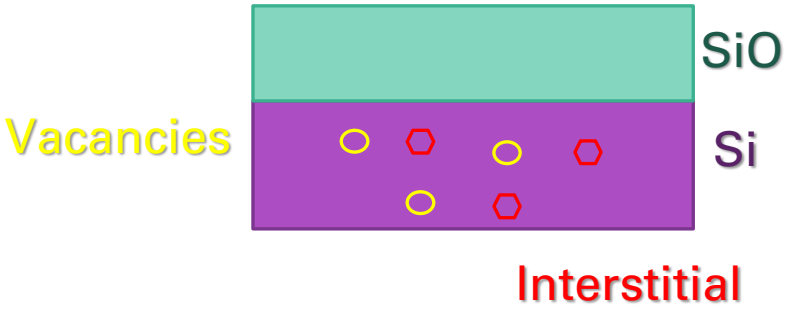
TID Radiation monitor

We tested 8 MOSFET to be used as radiation monitors. Their response is consistent, and the only caveat is to properly account for annealing (counter should only increase with time).



Displacement damage

Displacement damage happens when the **crystalline structure** of the silicon is **damaged**, i.e. an atom of the lattice is displaced somewhere else creating a vacancy where it was and an interstitial anomaly where it stops. We used neutrons at ENEA-FNG and NPI-CAS to investigate resilience to lattice damage.



BJT are affected by DD, decreasing their gain.

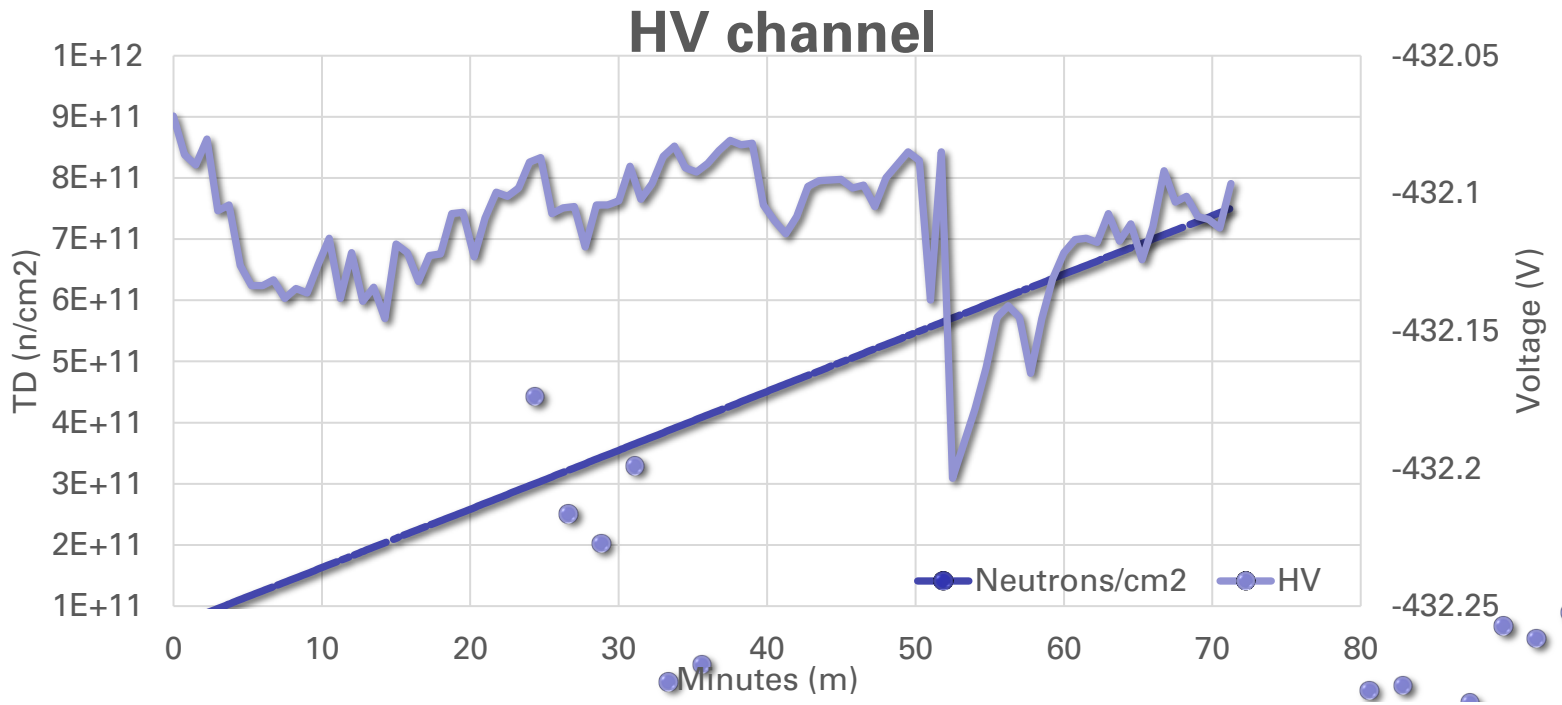
DD changes the characteristics of the lattice, facilitating the recombination of carriers/holes.

Moreover, neutron activation could be an issue as well.

Neutrons

Memory neutron resilience		
Error rate	2.2E-04	error/kB/Gn
MTBF (for neutrons)	1.1E+13	n/cm^2

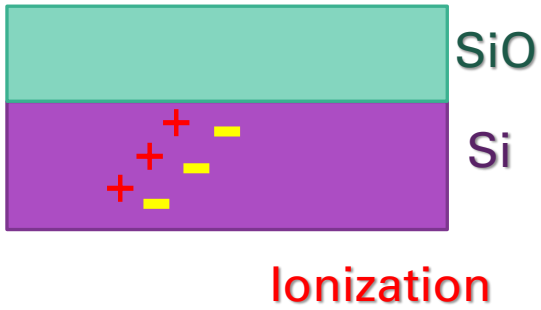
Bla



Single-Event Effects

They occur when a high energy particles ionizes a semiconductor. These events can be **temporary** like SEU (Single-Event Upset) or **permanent** like SEB (Single-Event induced Burnout).

We tested the robustness of our power supplies against SEE with protons at PSI and JYU.

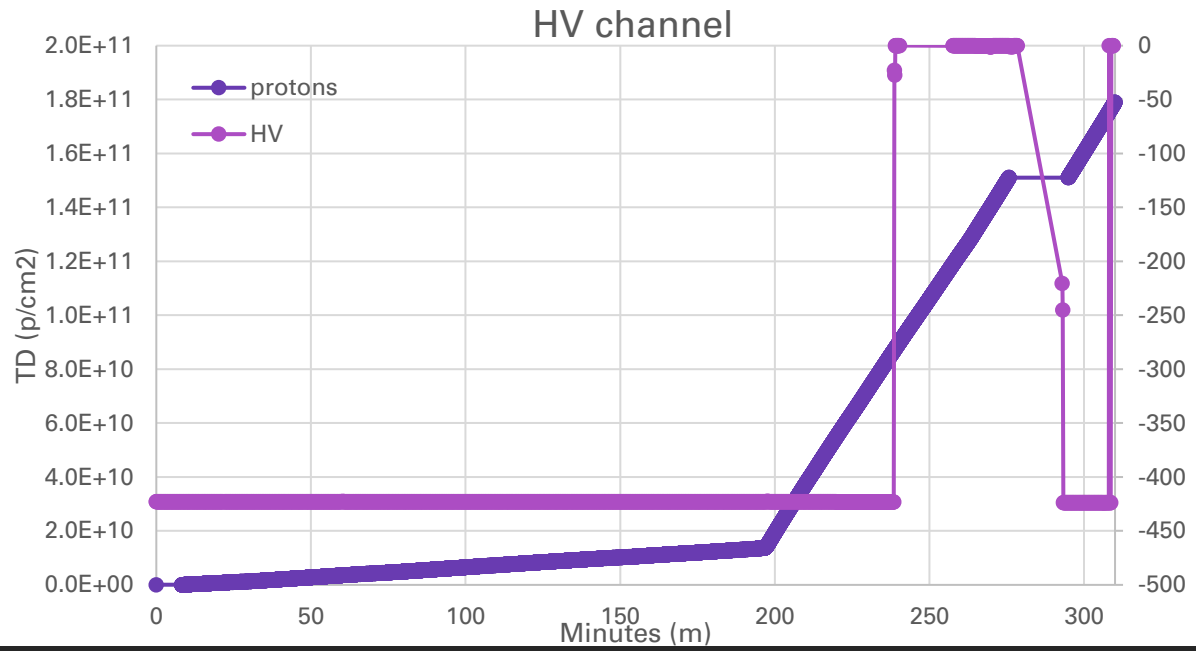


SEE can happen in both the control and the power parts of a power supply.

Protons

During our proton test we aimed at 10^{12} p/cm^2 as we saw that as a max value in the experimental cavern, and of course we wanted to include some safety factors in.

We did not notice any major issue during our irradiation a PSI, anyhow in Jyväskylä we noticed some failures before than expected.



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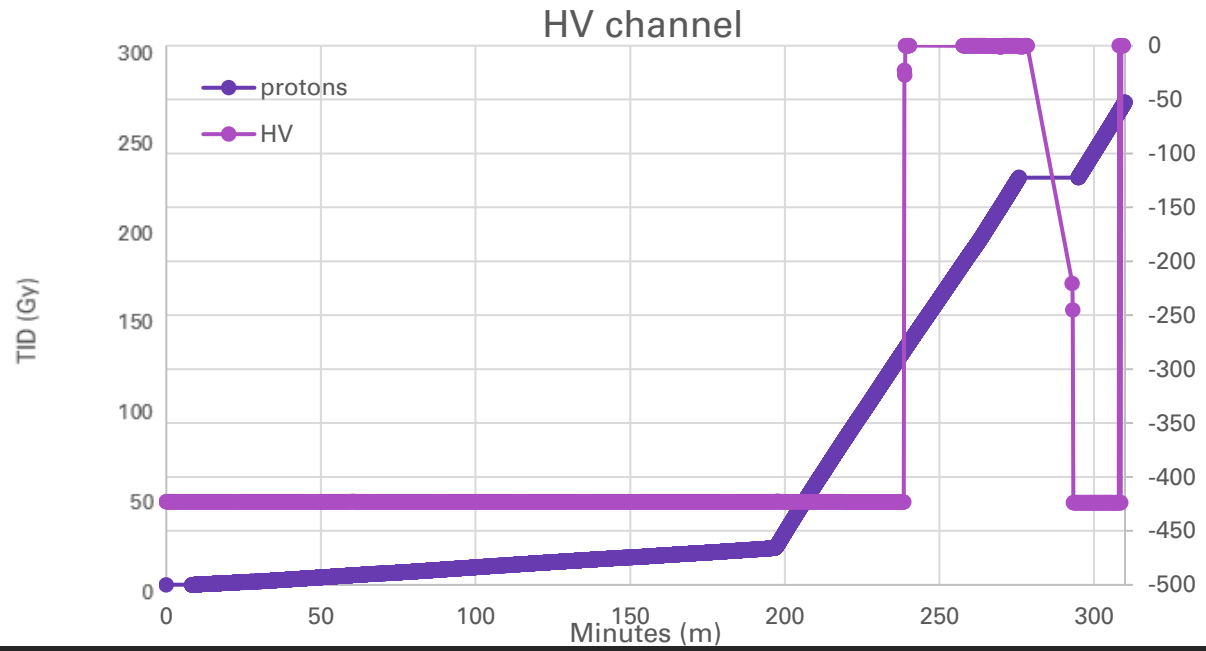
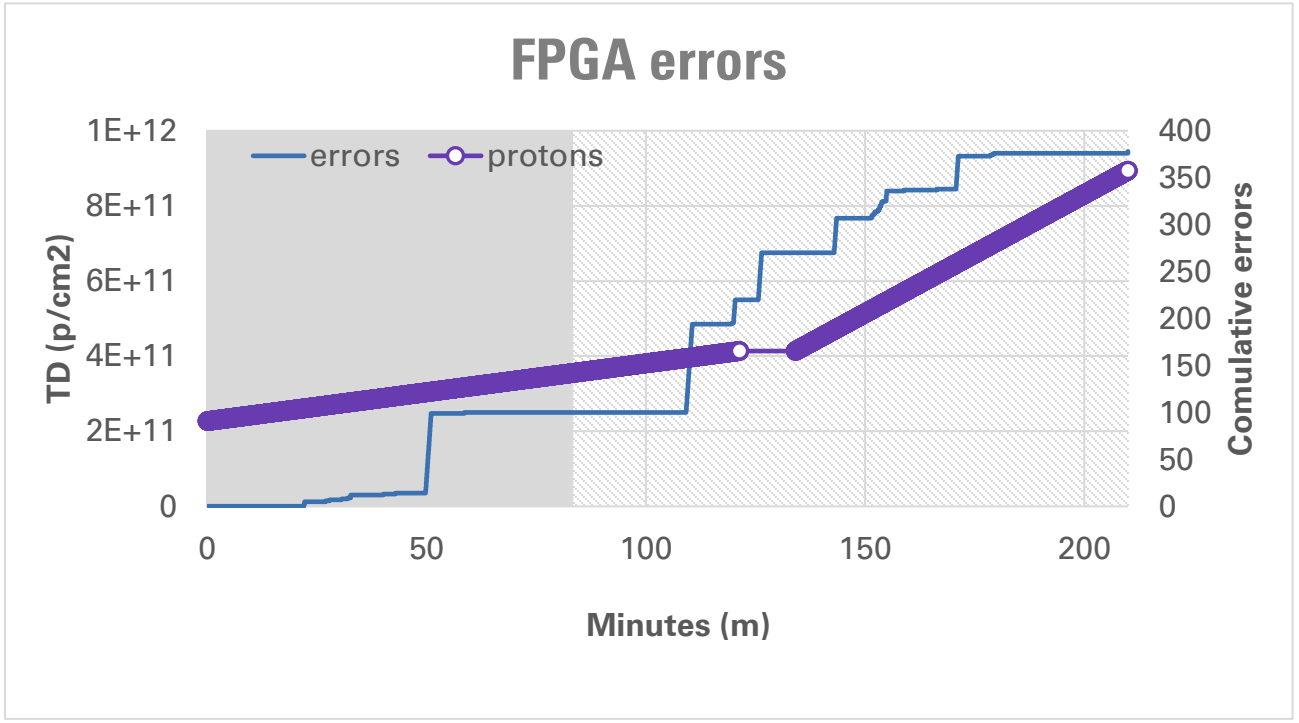
It turned our that the TID equivalent was rather high and some MOSFET started failing for that reason.



SEE in FPGA instantiated µC

We tested a known rad-tolerant FPGA, in details we wanted to use a **virtual micro-Controller** running withing the FPGA.

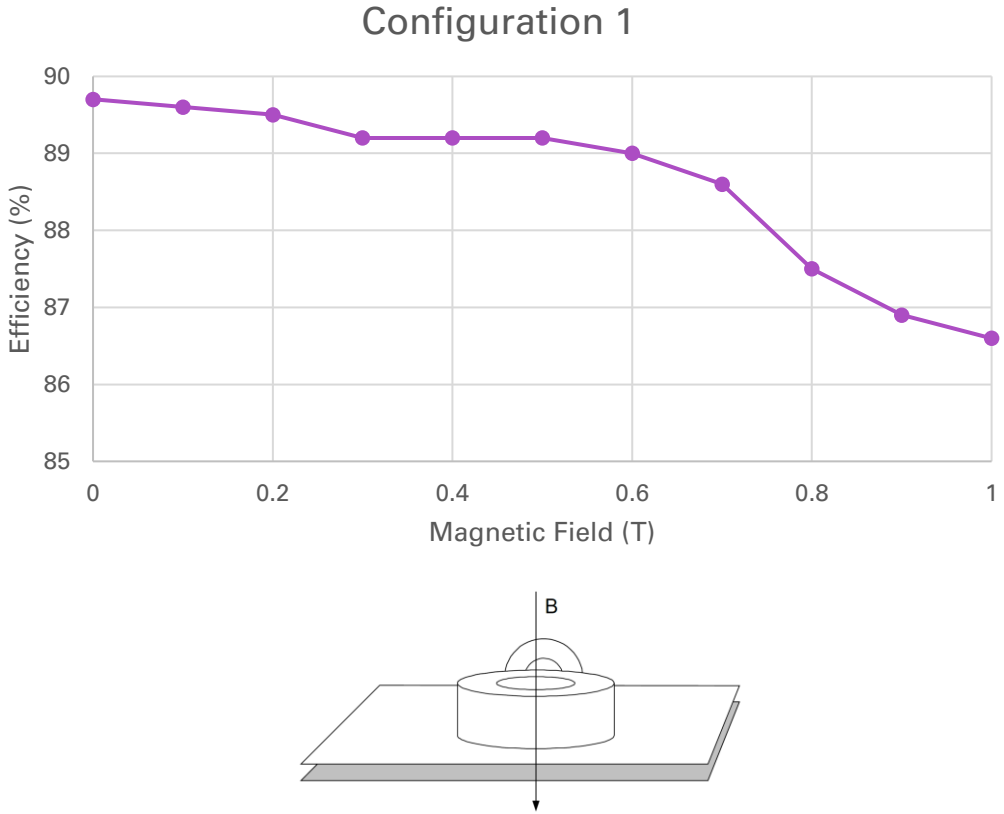
While the **FPGA itself was robust enough**, the **µC showed a lot of SEE since it runs on a SRAM** which is known to be susceptible to SEE like single event upsets.

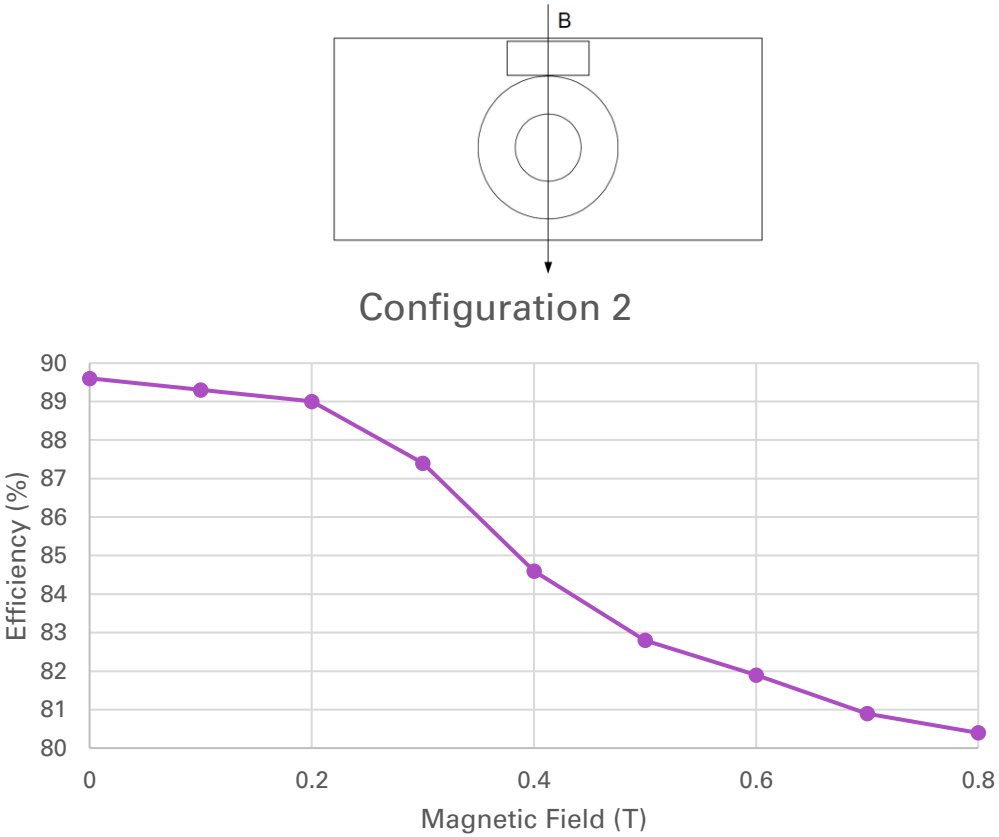


Mitigation Techniques

- **Hardware**
  - Less integrated circuits and more **discrete components**.
  - **Driving circuits** properly calibrated to offset for radiation damage in MOSFET.
  - Enhanced **safety features** to protect from SEE.
- **Firmware**
  - **Redundancy** of the variables (triplicated)
  - Proper **watchdog** techniques
  - Periodic initialization of **µC peripherals**
  - **Linear** and controlled coding

Magnetic field resilience





Conclusions 1/2

Testing electronics against radiation effects proves to be quite challenging, looking to only one type of damage at the time is impossible and extrapolating difficult.

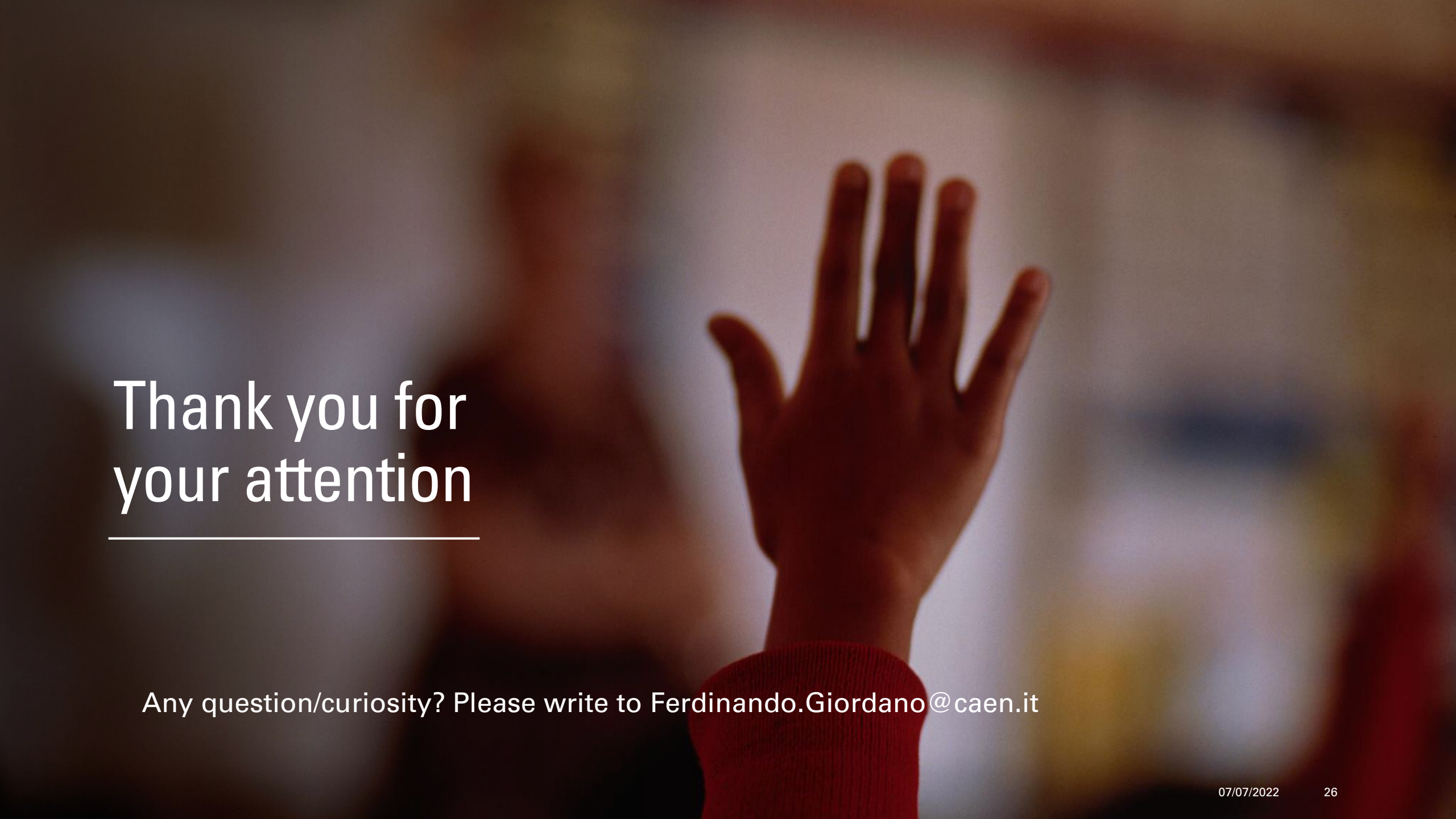
A careful choice of components, implementing mitigations since the electronics design and, eventually, testing with a realistic mixed field are paramount for successful development of hostile environment power supplies.

Of course, electric performance must be consistent with experimental requirements over the experiment lifetime, ensuring detector safety and data taking efficiency.

Conclusion 2/2

Thanks to all these tests CAEN has developed a power supply with unprecedented power and channel density: 32 channels packed in less than 5 U 19” rack, capable of delivering up to 6 kW to the detector.

The first LV/HV mixed board has been delivered for testing. Again, the design is unprecedented improving both channel and power density with respect to the boards deployed ad the beginning of LHC. Moreover, the new boards weight less and are easier to maintain.



Thank you for your attention

Any question/curiosity? Please write to Ferdinando.Giordano@caen.it