CMS

INFN Istituto Nazionale di Fisica Nucleare

UNIVERSITA DEGLI STUDI DI TORINO

The CMS MTD Endcap Timing Layer: Precision Timing with Low Gain Avalanche Detectors

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on behalf of CMS MTD group

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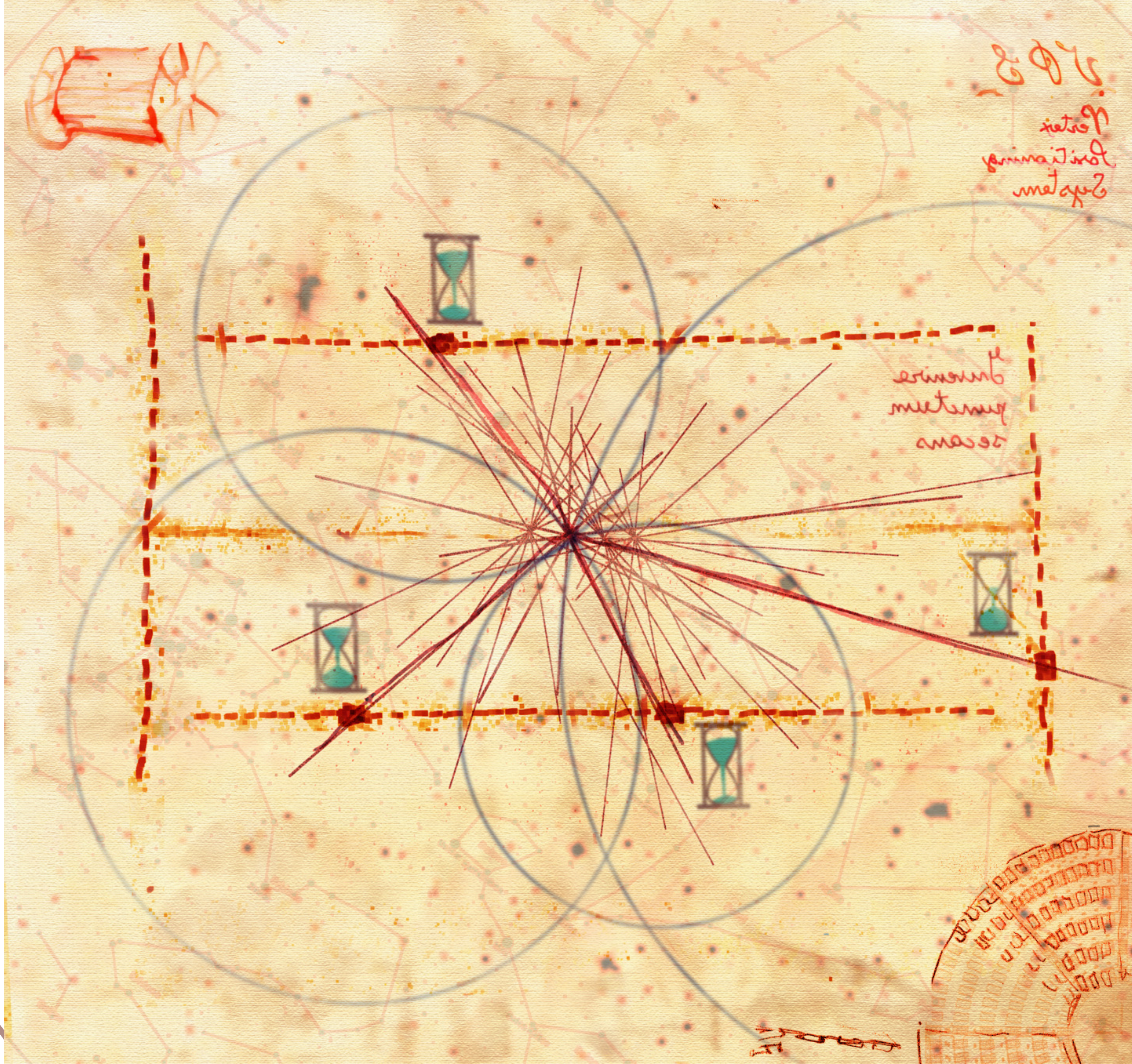
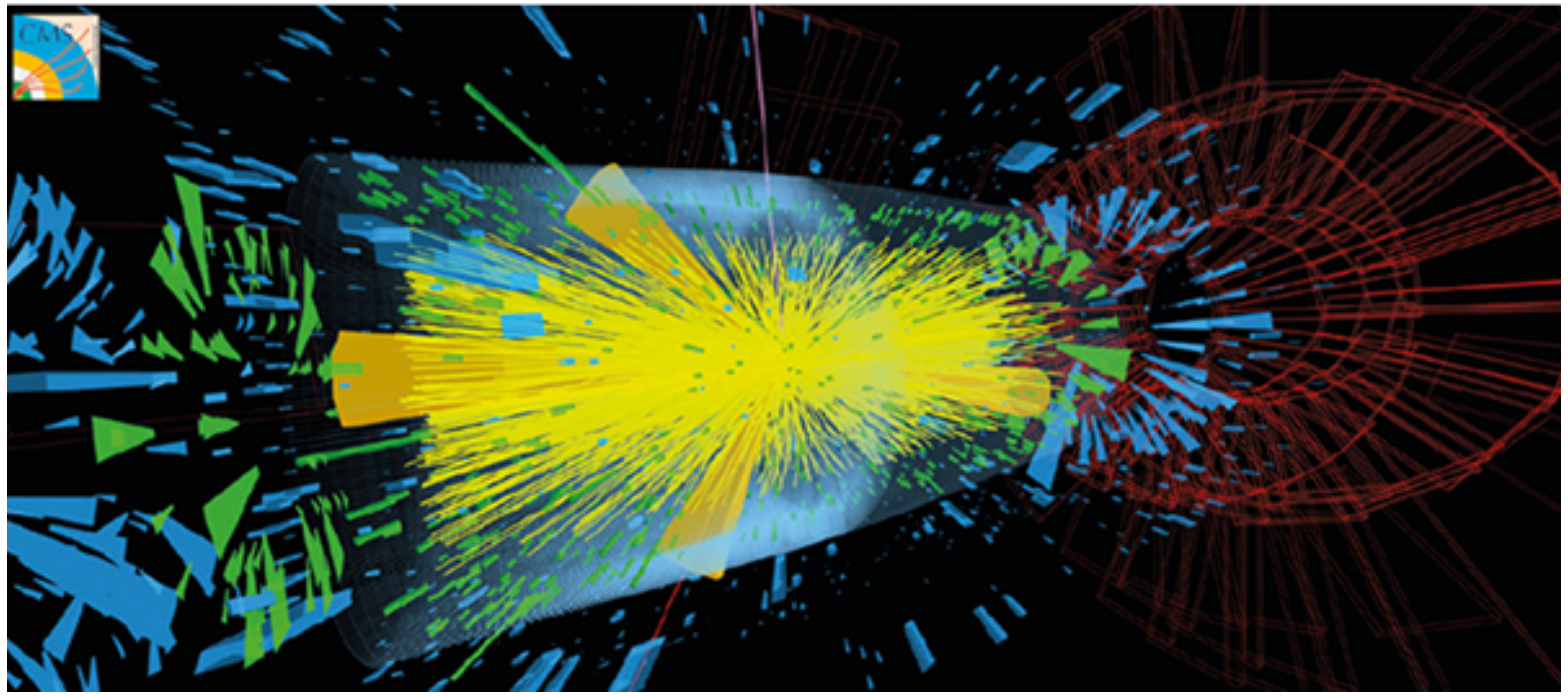
BOLOGNA

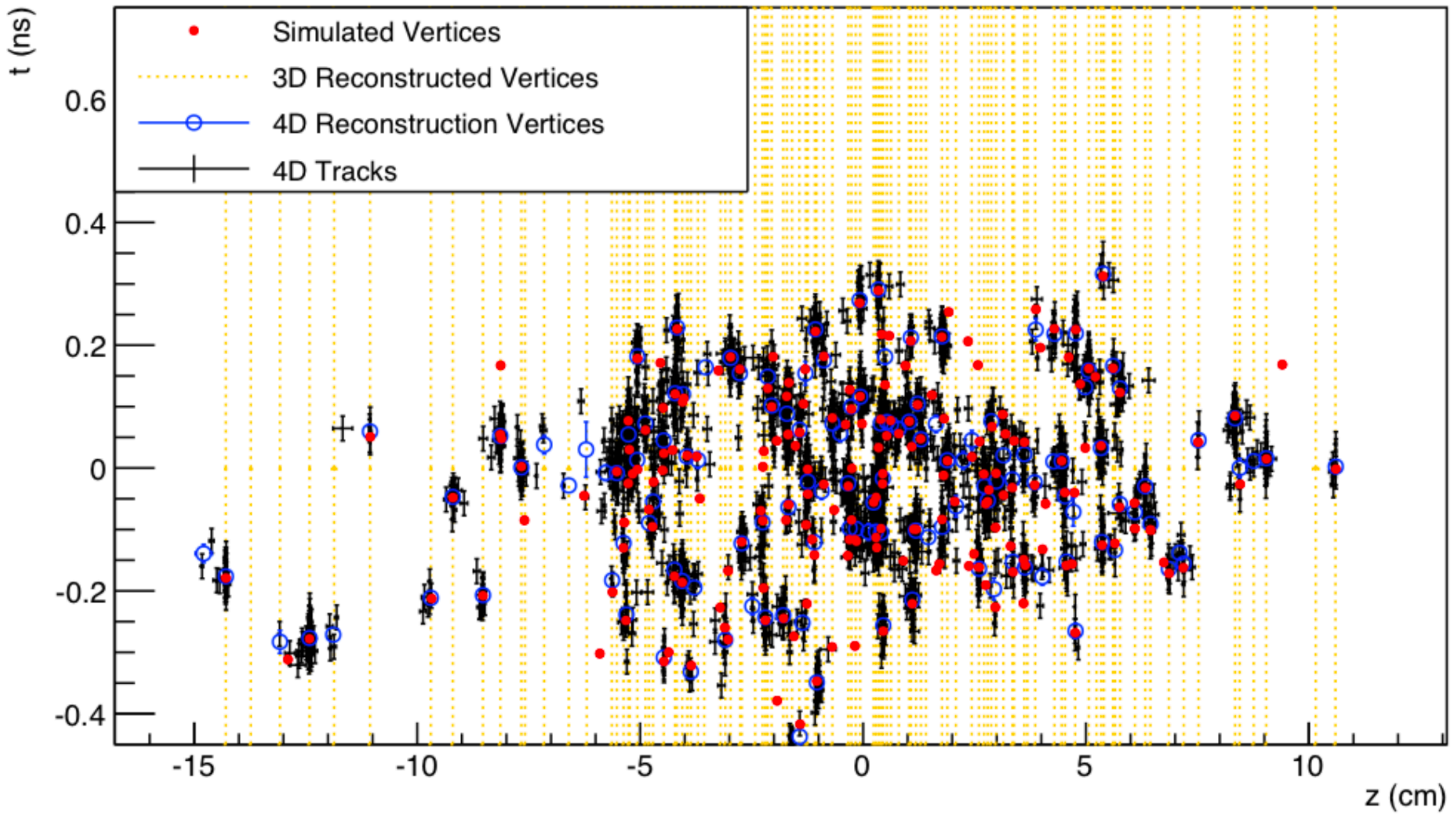


Precision timing at High Luminosity LHC

At **High Luminosity LHC** instantaneous luminosity will increase of a factor ~5
→ **140-200** proton-proton collisions in each bunch crossing
→ difficulties in object reconstruction and particle identification due to **tracks coming from nearby vertices**

Need to **add timing information** to separate events overlapped in space but happening at different times
→ Creation of timing detectors providing **4D tracking**
→ **Minimum Ionizing Particle Timing Detector** (MTD) for the CMS experiment

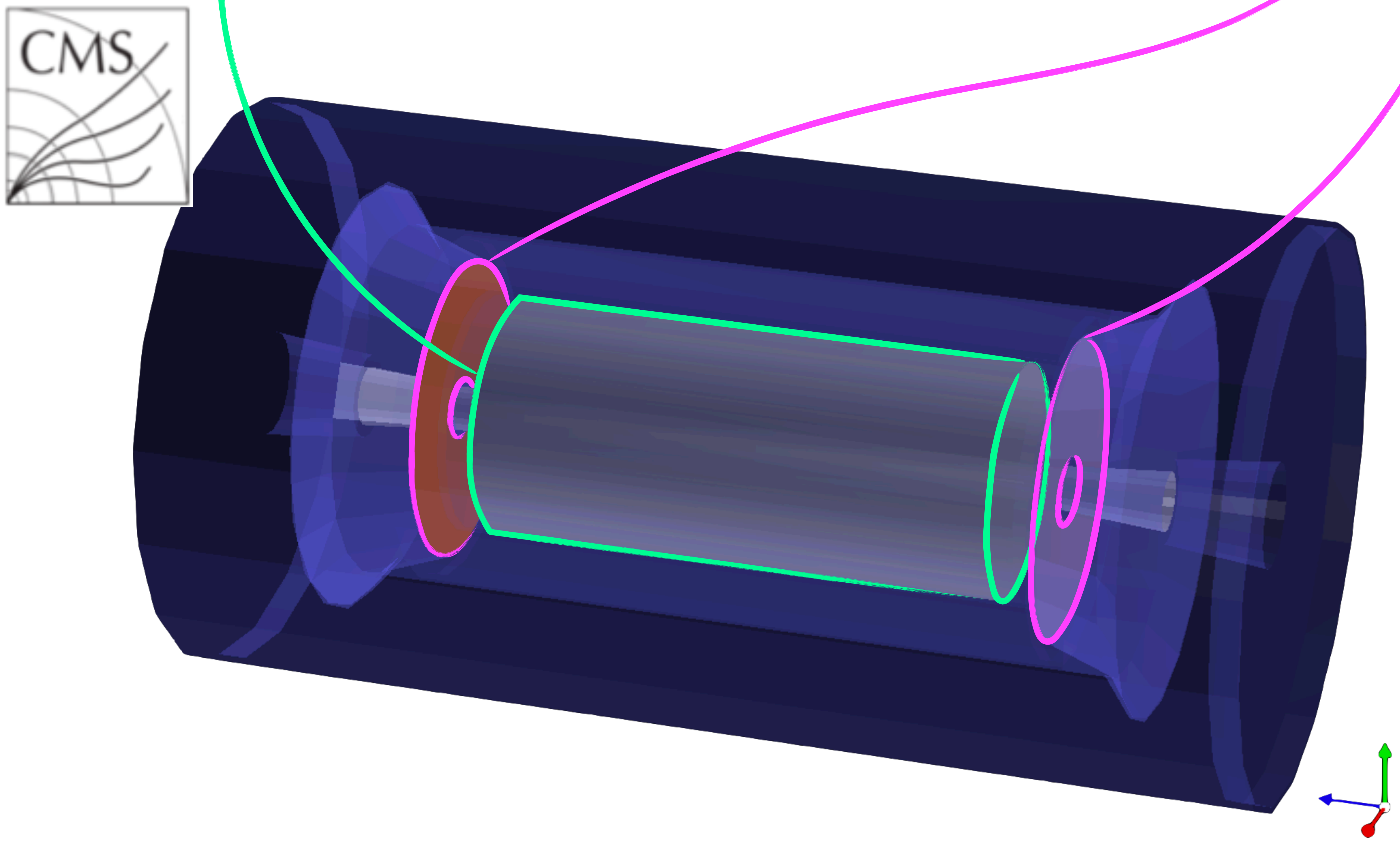




The CMS MIP Timing Detector

Barrel Timing Layer (BTL)
LYSO crystals read-out by **SiPMs**
Total surface 38 m^2
Hermetic coverage for $|\eta| < 1.45$

Endcap Timing Layer (ETL)
Low Gain Avalanche Diodes with ASIC readout
Total surface 14 m^2
Hermetic coverage for $1.6 < |\eta| < 3.0$



MTD will improve reconstruction by:

- Collecting timing information on charged particles
- Combining tracking with timing

Providing a **timing resolution** $\sigma_t \sim 30 - 40$ ps at the start of HL-LHC, barrel degrades to 50-60 ps at end of HL-LHC

→ **Mitigation of pile-up effect from HL-LHC**

The CMS Endcap Timing Layer

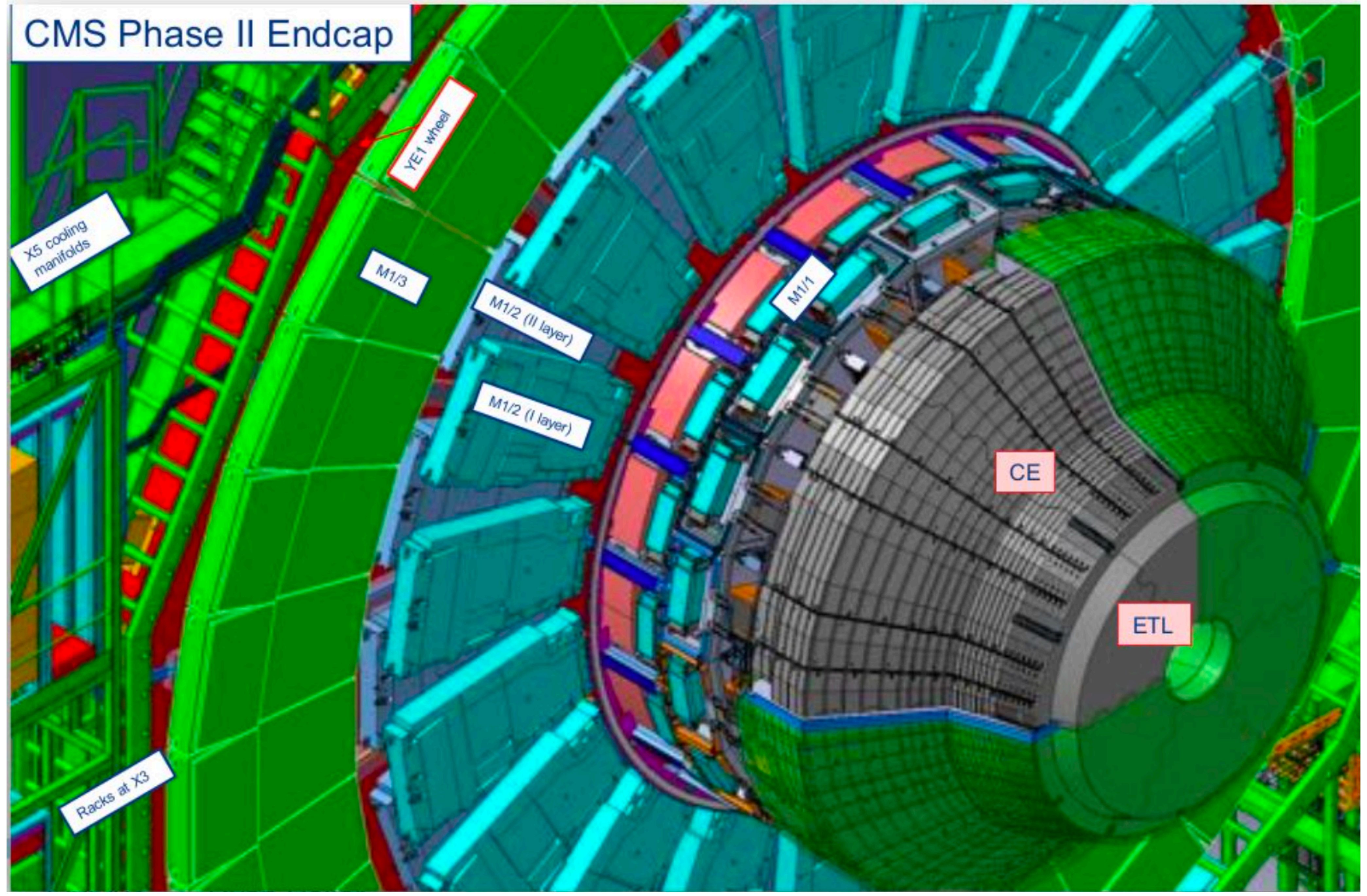
- ETL will be placed on the HGCAL nose
- **Two disks** for each endcap, covered in silicon sensors on **both sides**
- Hermetic coverage for $1.6 < |\eta| < 3.0$

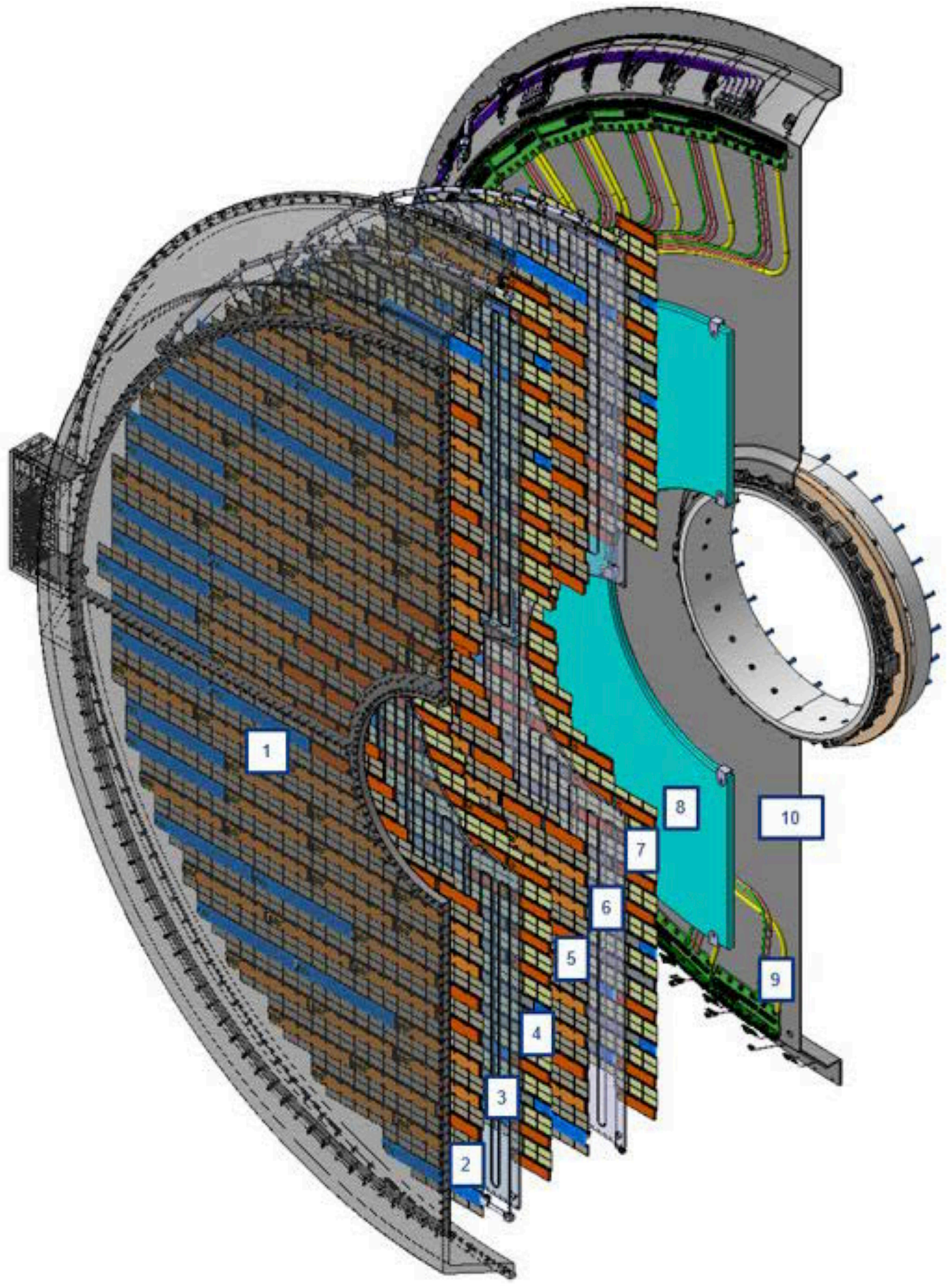
Ensure 2 hits for each track

Single-hit resolution <50 ps

$$\sigma_{single\ hit} = \sqrt{\sigma^2_{sensor} + \sigma^2_{readout}} \text{ with } \sigma_{sensor} \sim 30 - 40\ ps$$

Track resolution <35 ps





Element	
1	Thermal screen
	Gap between thermal screen and Face 1
2	Face 1 - active layer
3	Front disc
4	Face 2 - active layer
	Gap between Face 2 and Face 3
5	Face 3 - active layer
6	Back disc
7	Face 4 - active layer
	Gap between Face 4 and ETL front moderator
8+9	Patch panels 0 + cables [9] + ETL front moderator
10	ETL back support plate
	Gap between ETL back support plate and CE thermal screen

CMS requirements for ETL

ETL will contribute to **maintain CMS present performance also in HL-LHC environment**:

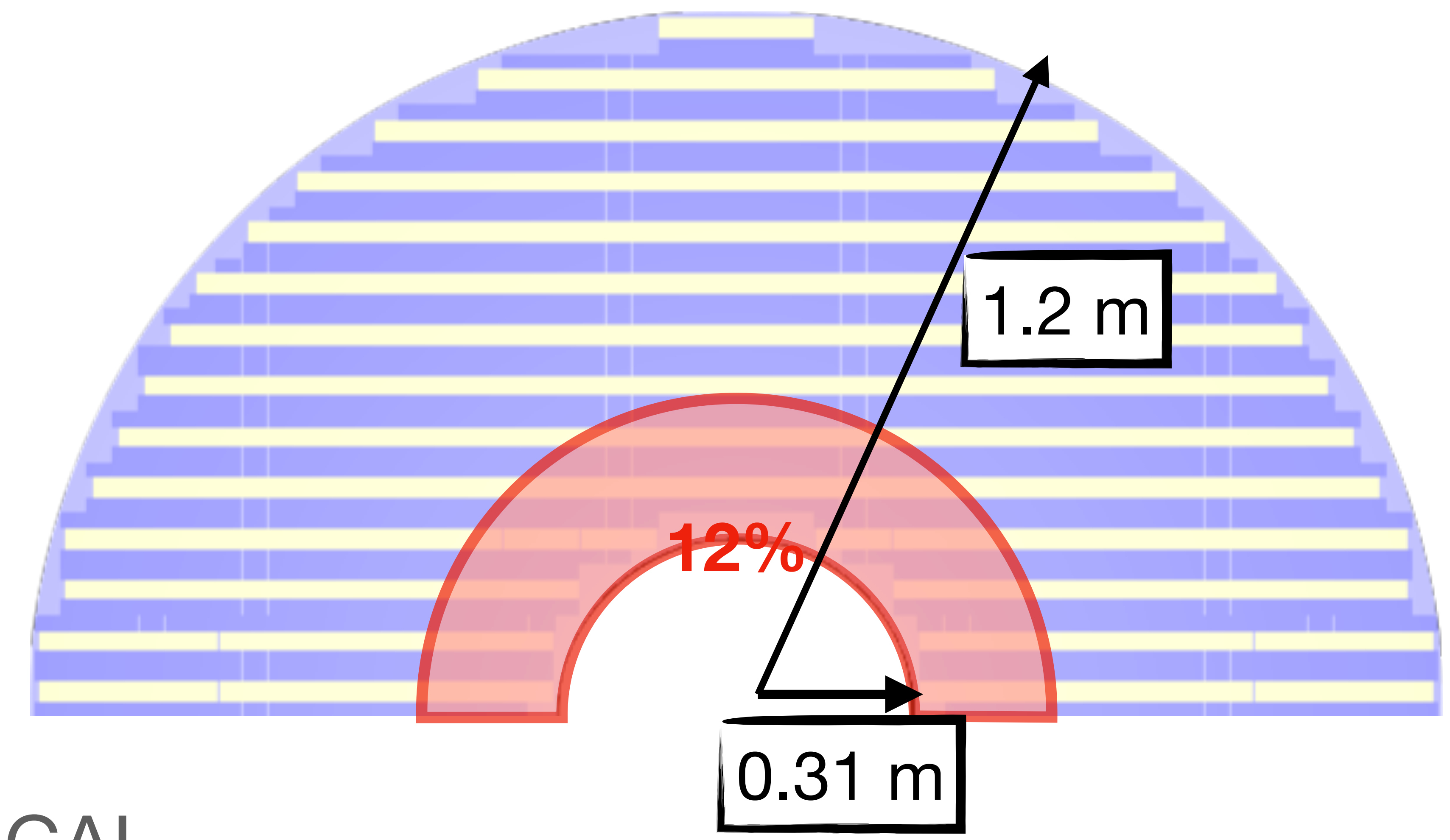
- **Fill-factor** (ratio between active and total detector area) **> 95%**
- **Low occupancy** (<0.1% low η, 1% highest η) to avoid double hits and ambiguous time assignment
- Radiation tolerance up to $\mathbf{1.7 \times 10^{15}\ n_{eq}/cm^2}$ at $|\eta| = 3.0$

  Large part of ETL will be exposed to less than $\mathbf{1 \times 10^{15}\ n_{eq}/cm^2}$

  → Only 12% of ETL surface will reach higher fluences

  Operating temperature below -25°C
- Design allowing to access the detector for maintenance

  → **Independent volume** isolated and operated separately from HGCAL



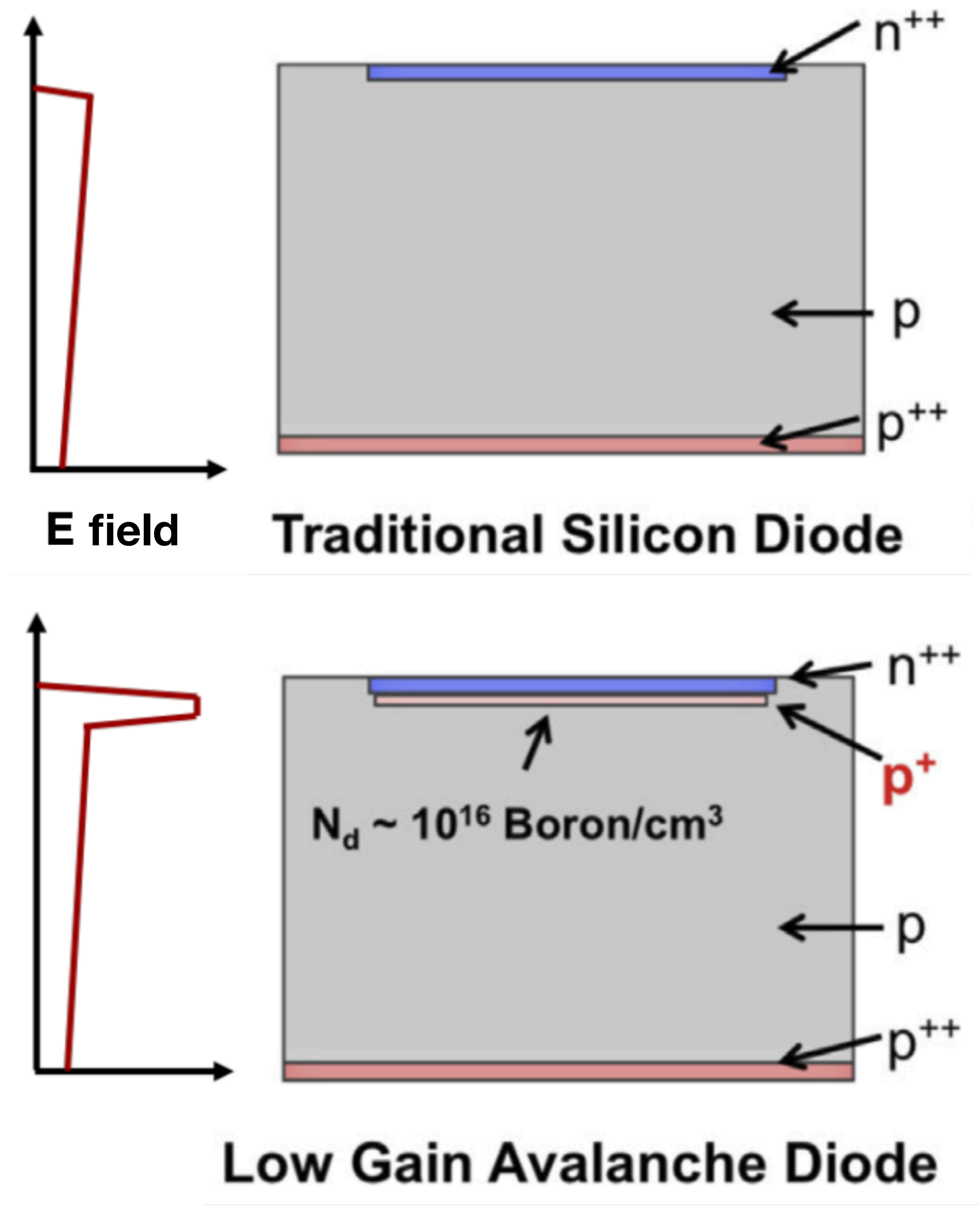
ETL sensors

ETL will be instrumented with **Low Gain Avalanche Diodes** (LGADs) optimized for timing measurements

LGADs are provided with a **gain layer**, a highly-doped thin layer near the p-n junction

→ High local electric field producing **charge multiplication**

→ **Moderate gain factor 10-30** to maximize signal/noise ratio



Sensor requirements:

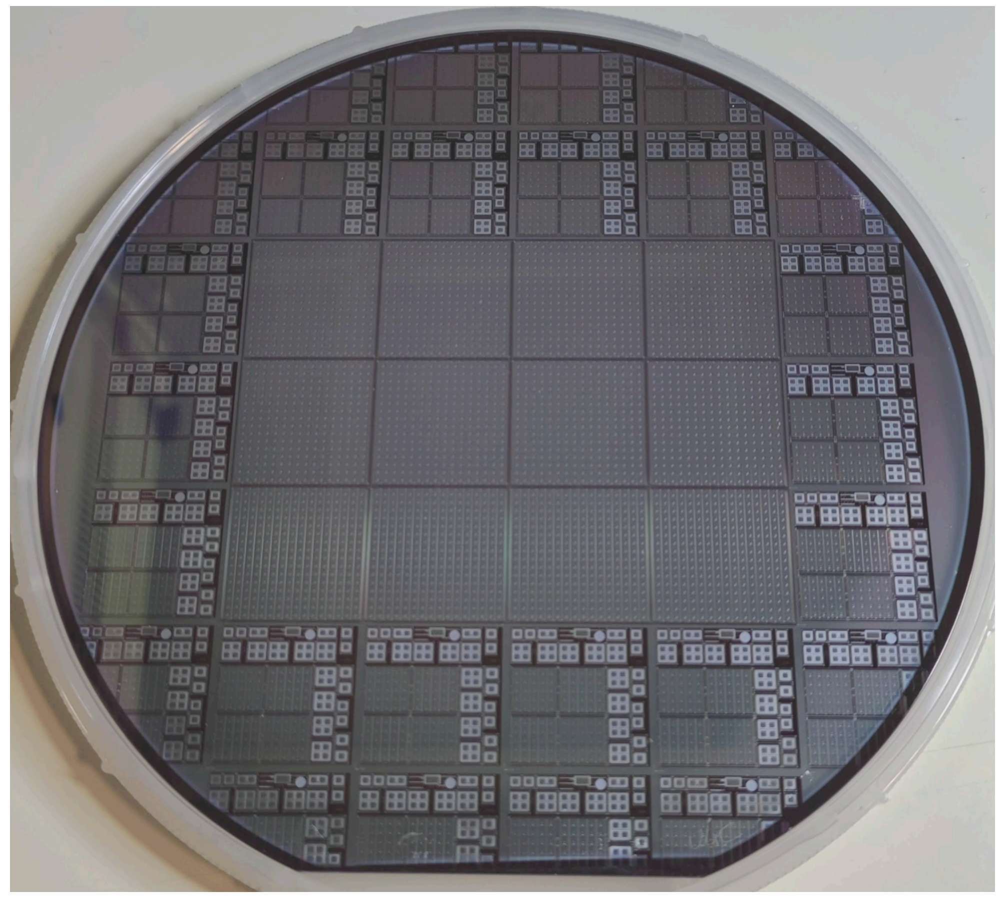
- **Pad size determined by occupancy and read-out electronics** (rather large capacitance, 3-4 pF)
- **Gain uniformity**
- **Low leakage current** to limit power consumption and noise
- Provide **large and uniform signals**, >8 fC when new, >5 fC after highest irradiation point
- Minimized "no-gain" area, **interpad distance < 50 µm**

The final sensor will be a 50 µm-thick 16×16 pad array with 1.3×1.3 mm^2 pads

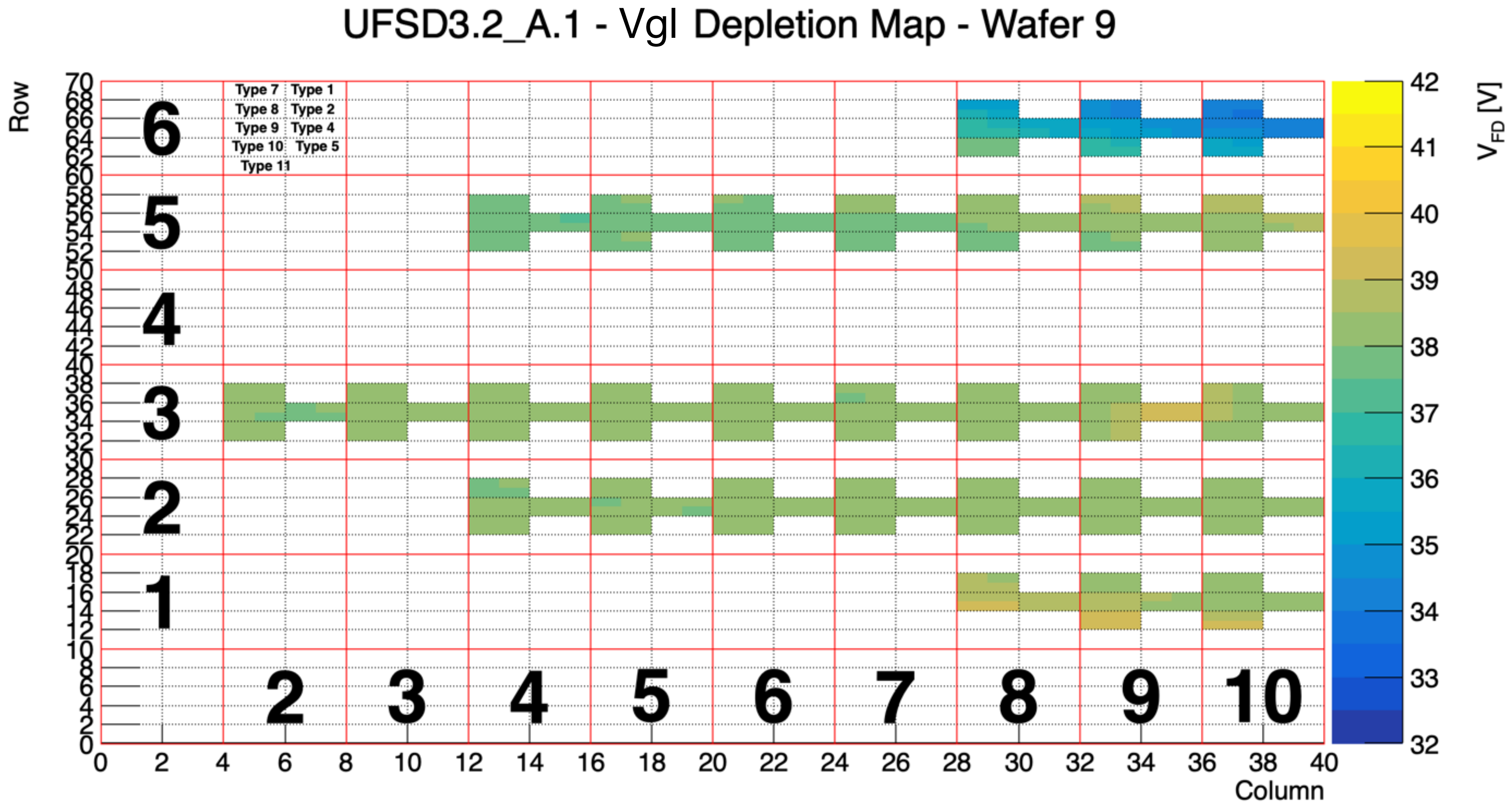
Finalizing the ETL sensor design

Prototyping studies to define the details for the final ETL sensor design are ongoing
Large size prototypes have been produced by different vendors: FBK, HPK, CNM, IHEP

Market Survey is in progress for the selection of vendors able to provide suitable sensors for ETL



HPK and FBK have been following R&D with us:



- ✓ **Latest LGAD productions have a high yield** and have low leakage current. 16x16 arrays yield is very good, >70%
- ✓ **Gain layer depletion disuniformity <1%**: representative of sensor response disuniformity

→ **well within required specifications**

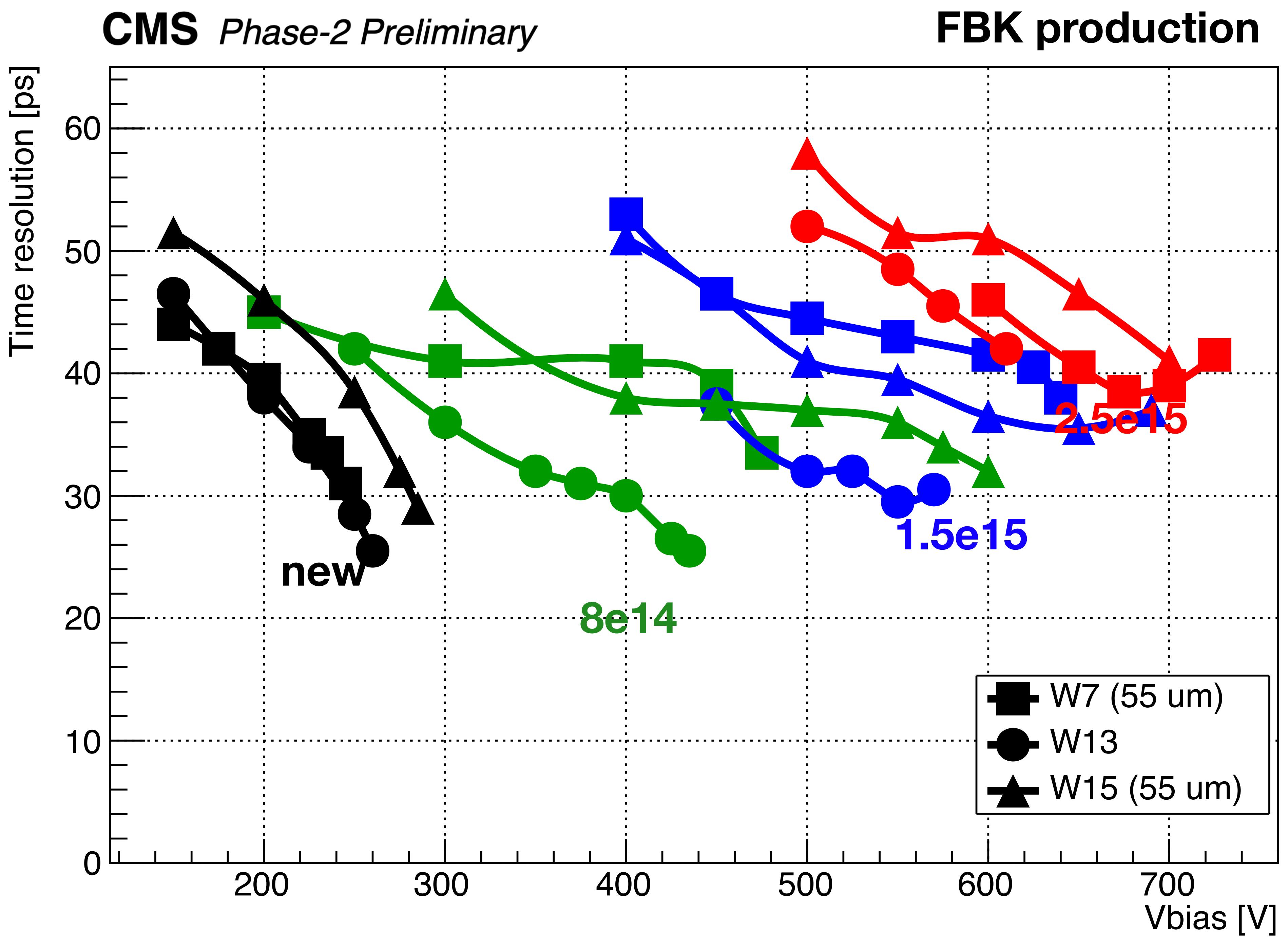
Timing resolution performances

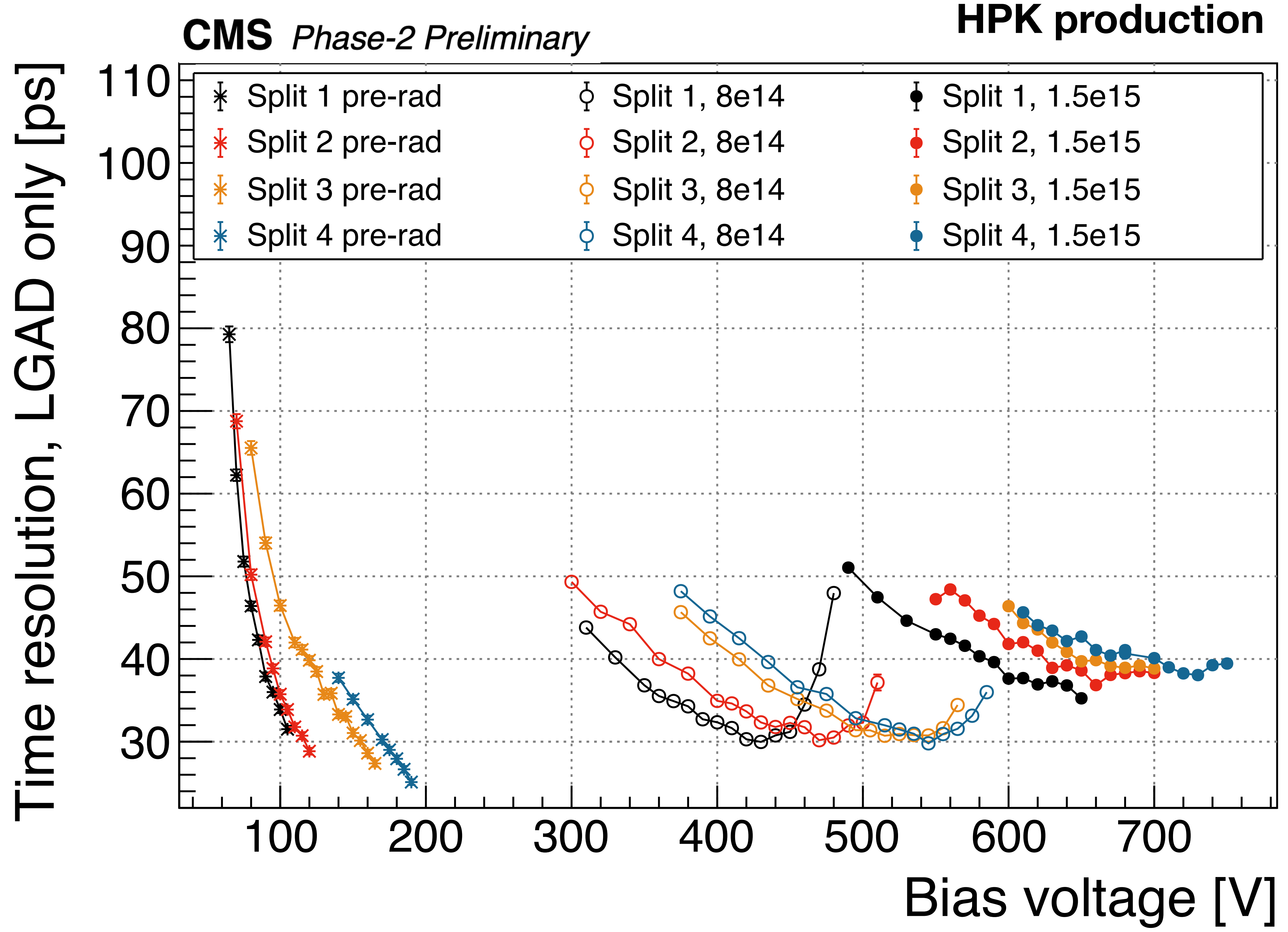
Sensor performances are benchmarked using very fast low noise electronics

→ results might be different with the ETL ASIC

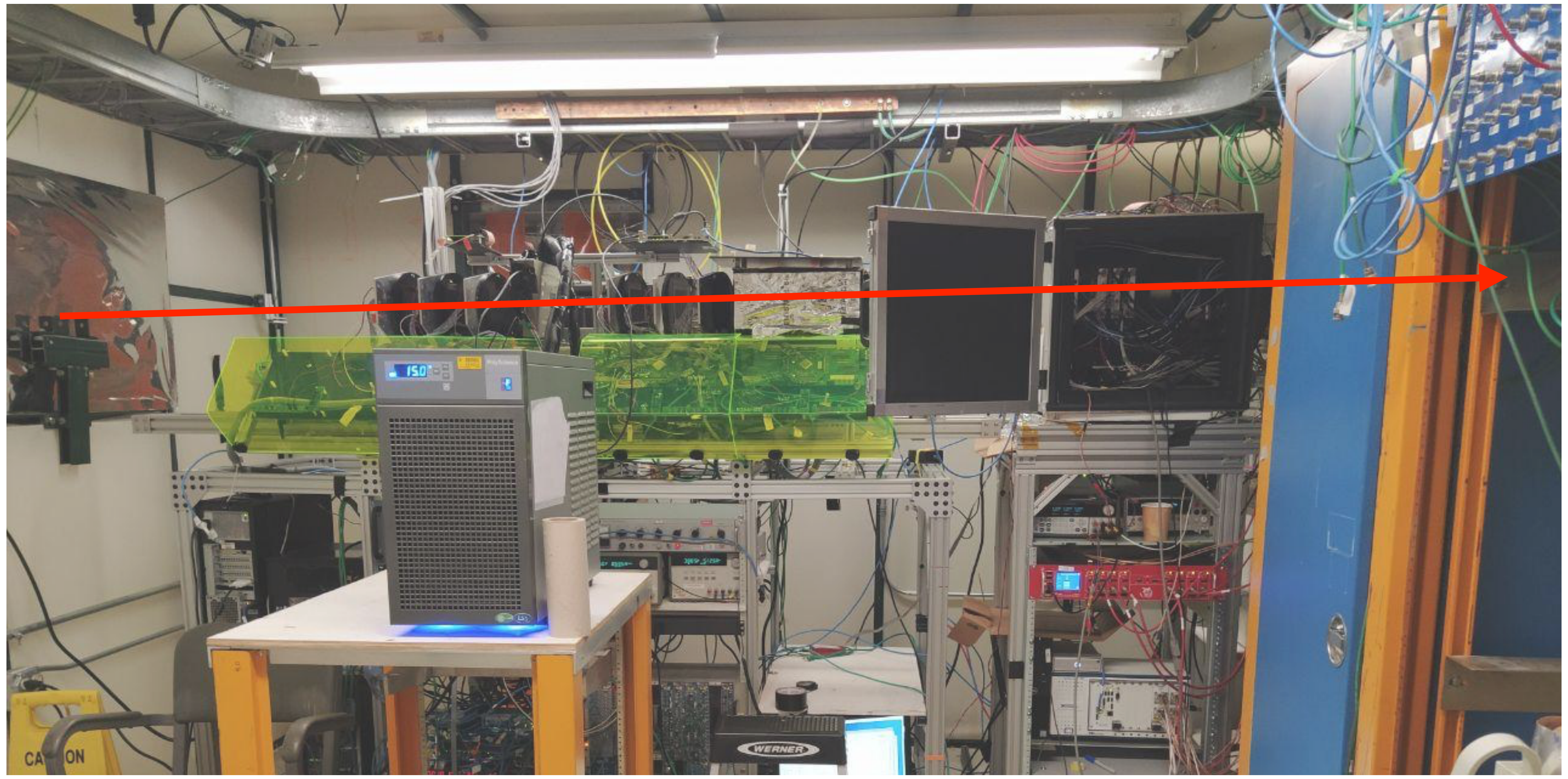
Measurements performed with **Beta-source setups** based on **Sr90 sources** in Torino and at Fermilab

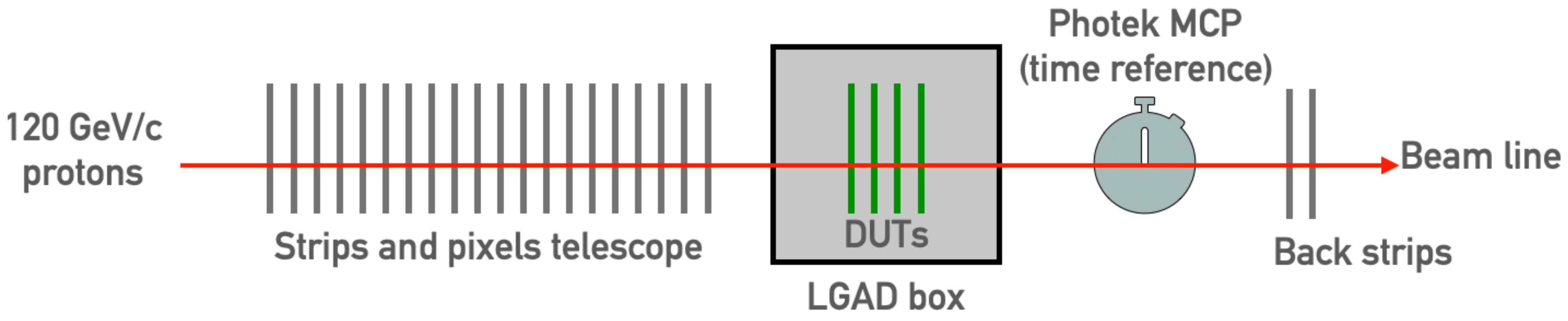
Most performing prototypes can reach a **timing resolution <40 ps** up to fluences of **2.5e15 n_{eq}/cm^2**





Test beam @ FermiLab





Fermilab test beam facility:

- **120 GeV/c proton beam**
- Trigger provided by independent **scintillator**
- **Precise tracking** performed with strips and pixels telescope
- Timing resolution measurements with high speed Photek Micro-Channel Plate as reference providing **timestamp with 10 ps resolution**
- **Cold box** with LGADs under test

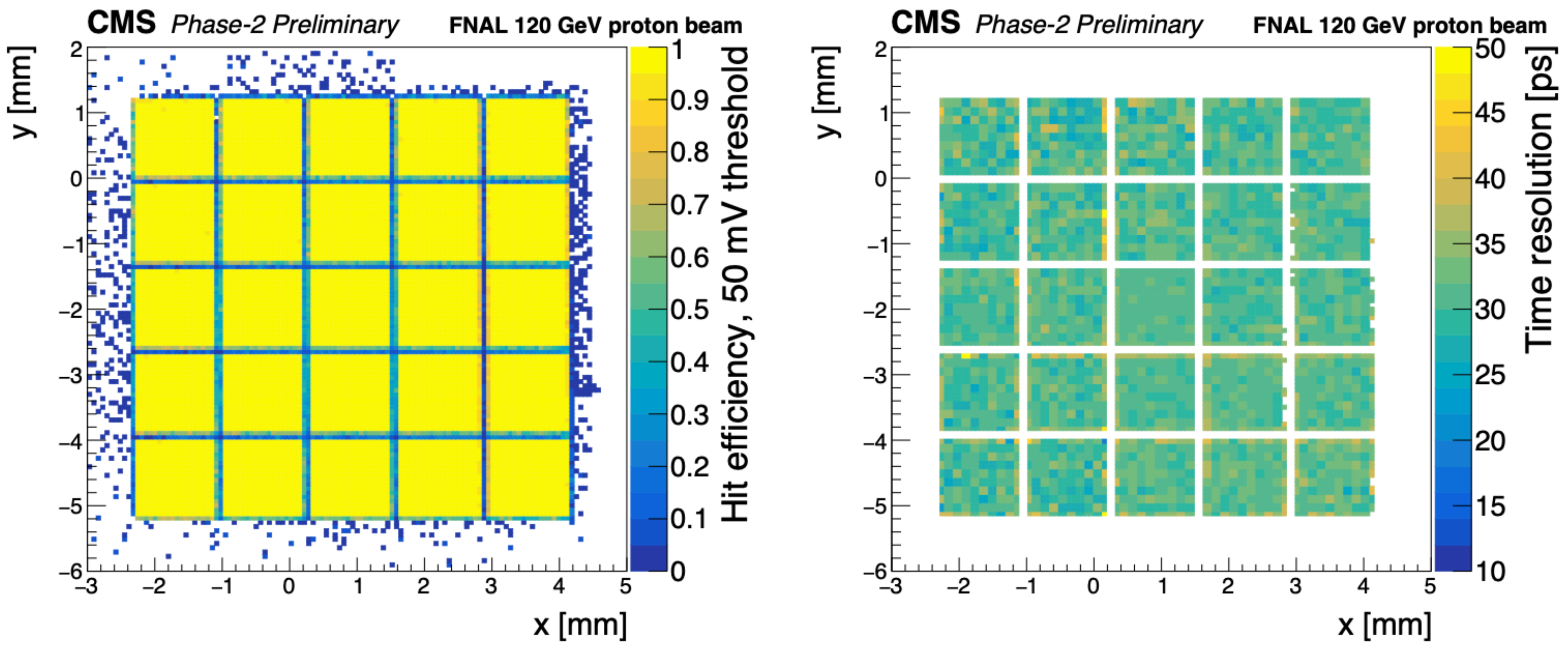
→ **Study of a limited number of sensors with high precision**

Test beam results

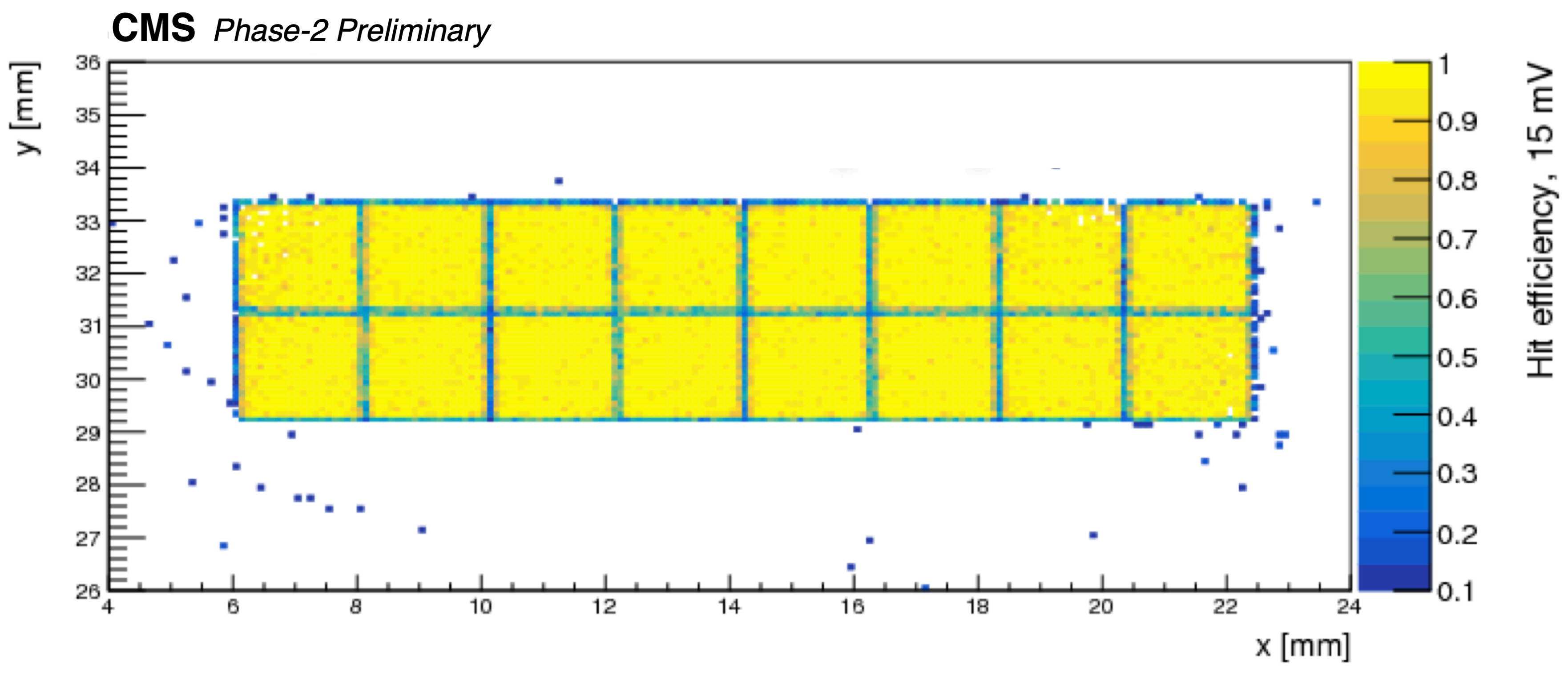
Uniform **timing resolution** map with $\sigma_t \sim 30$ **ps** for new devices

Uniform **hit efficiency** reaching **~100%** in new sensors and **~99%** after irradiation

→ **LGADs are highly uniform and efficient, able to reach target resolution on large multi-pad arrays**

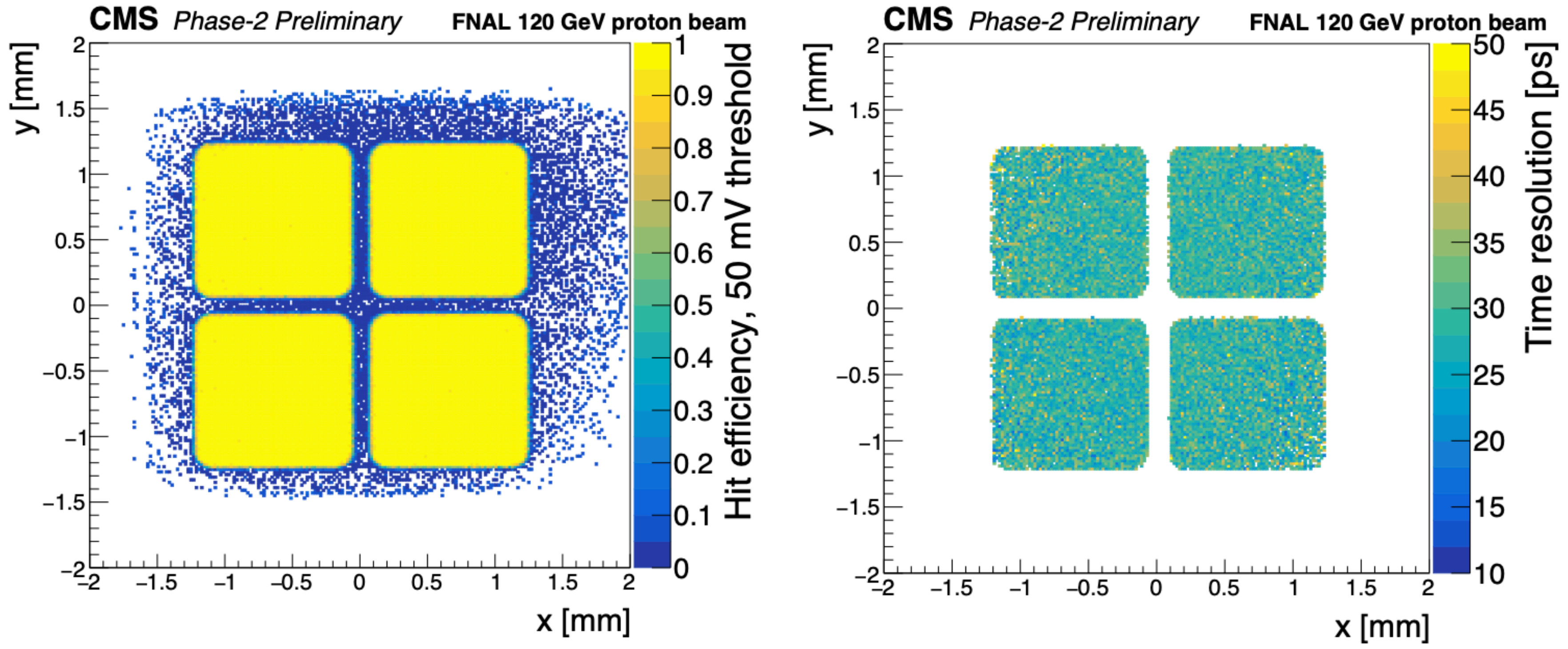


New FBK 5×5 array



FBK 2×8 array (first prototype sensor production)

Irradiated 8e14 n_{eq}/cm^2



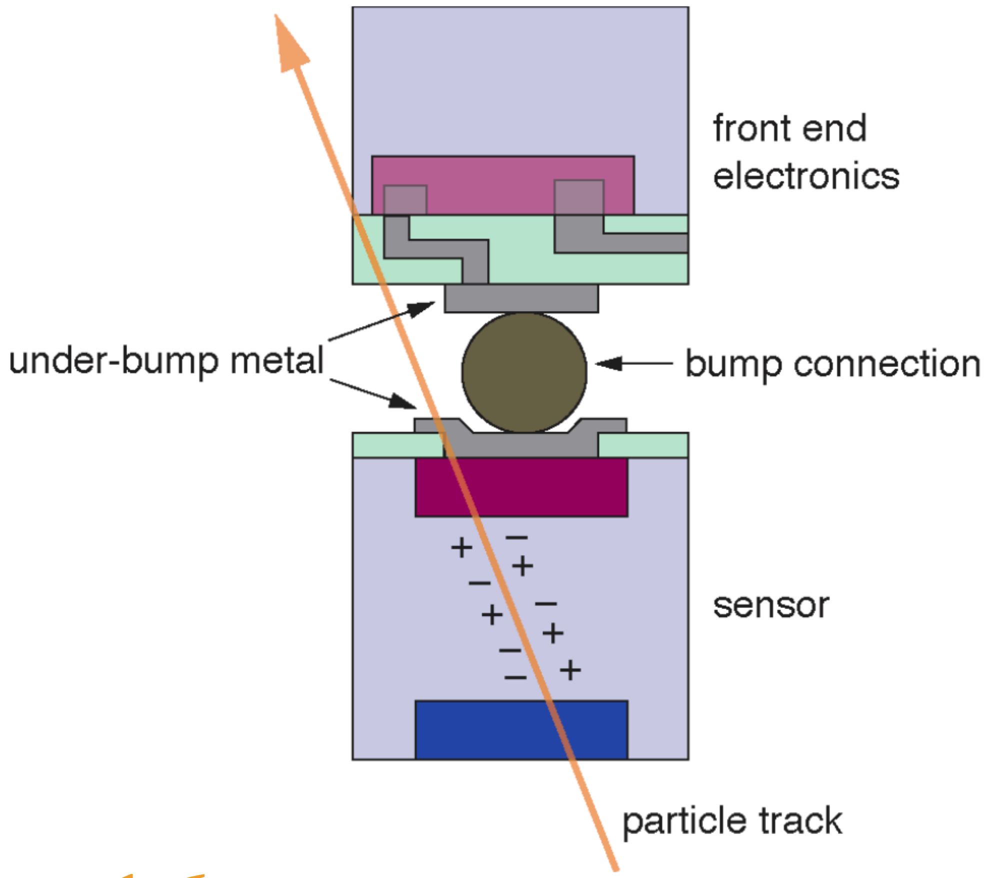
New IHEP IME 2×2 array

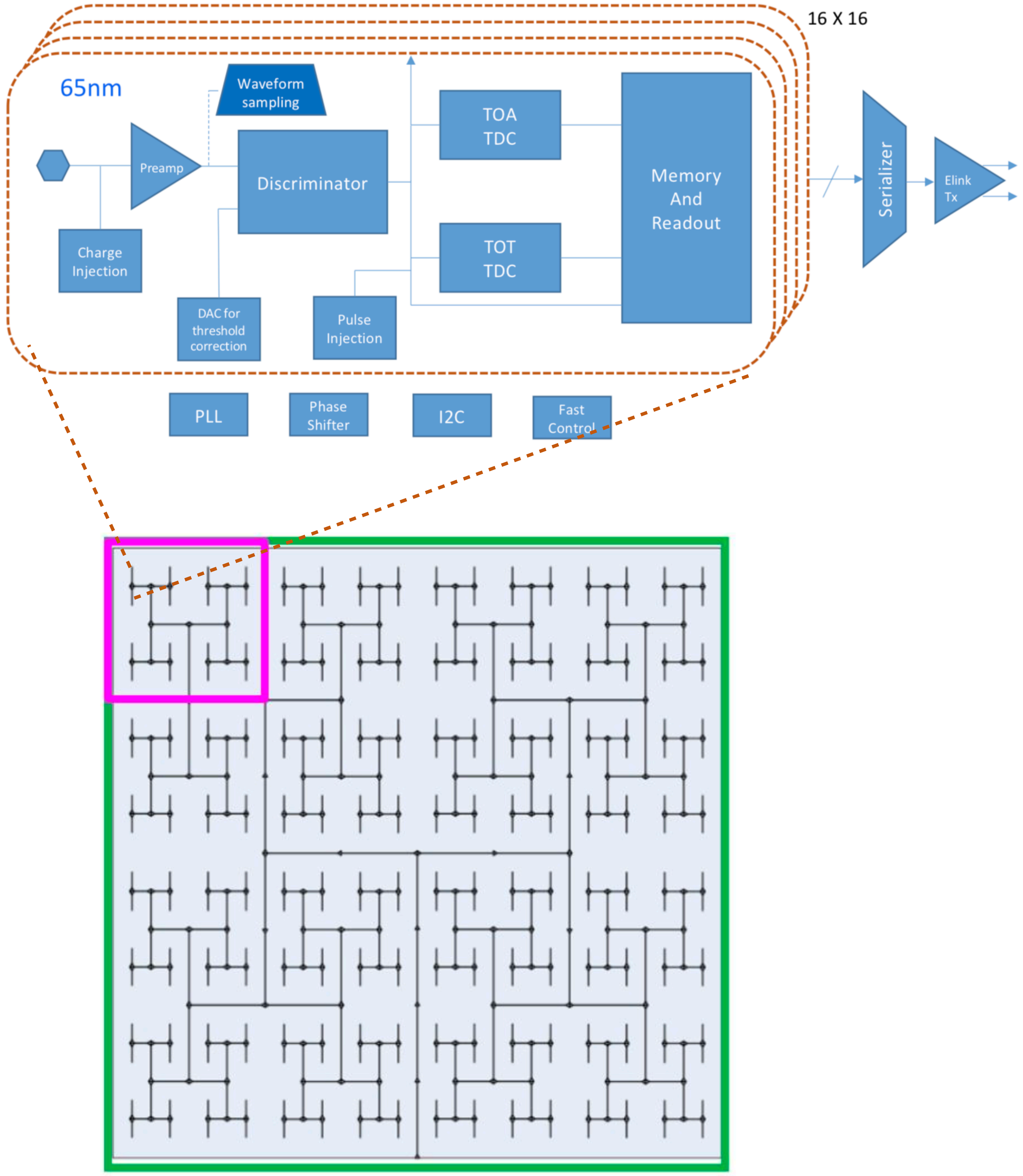
ETROC: ETL Read-Out Chip

The **Endcap Timing Layer Read-Out Chip** (ETROC) is the ETL read-out ASIC

Goal: reach time resolution $\sigma_t < 50$ ps per single hit

- Low noise and fast rise time
- Power budget: 1 W/chip, 3 mW/channel





Three prototype versions before the **final full-size 16×16 chip**:

✓ETROC0 and ETROC1 produced and tested

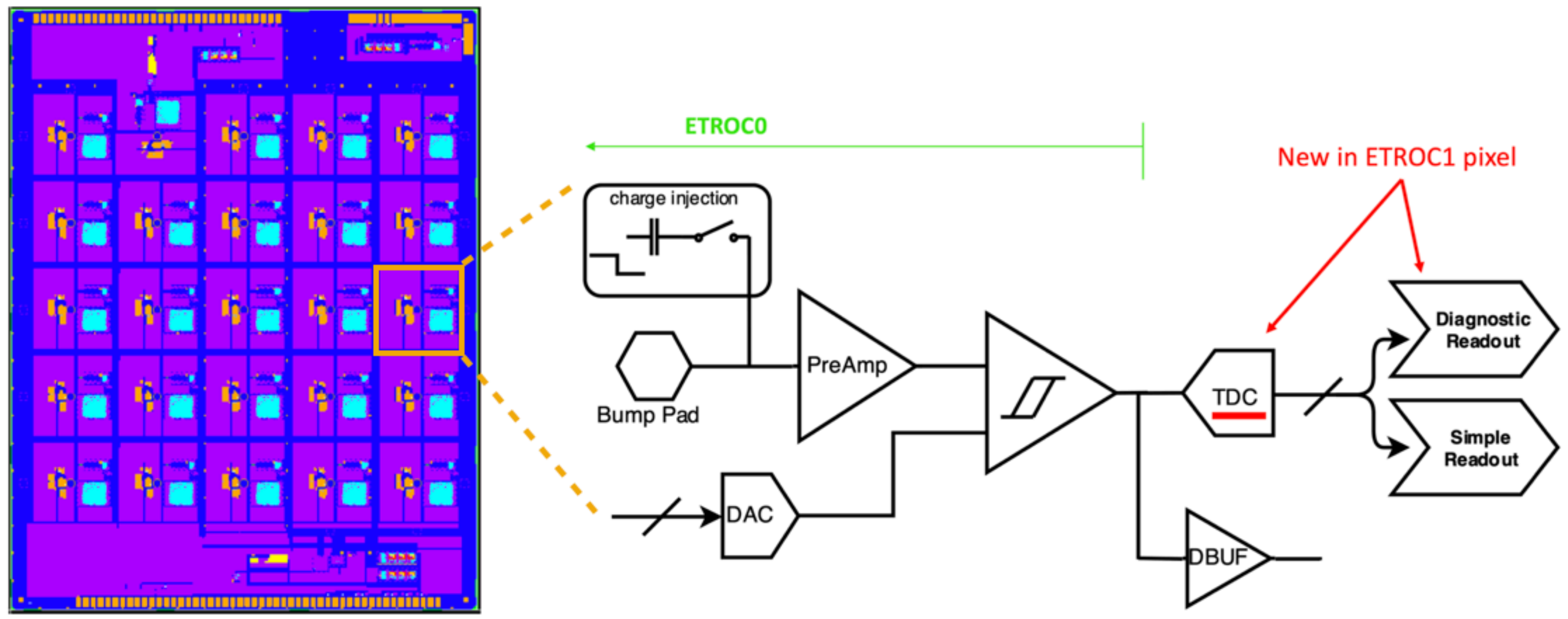
  ✓ **ETROC0: single analog channel**

  ✓ **ETROC1: full front-end with TDC and 4×4 clock tree**

➡ **ETROC2 design in progress: full functionality + full size**

➡ **ETROC3:** submission in March 2024, pre-production chip

ETROC1 @ test beam



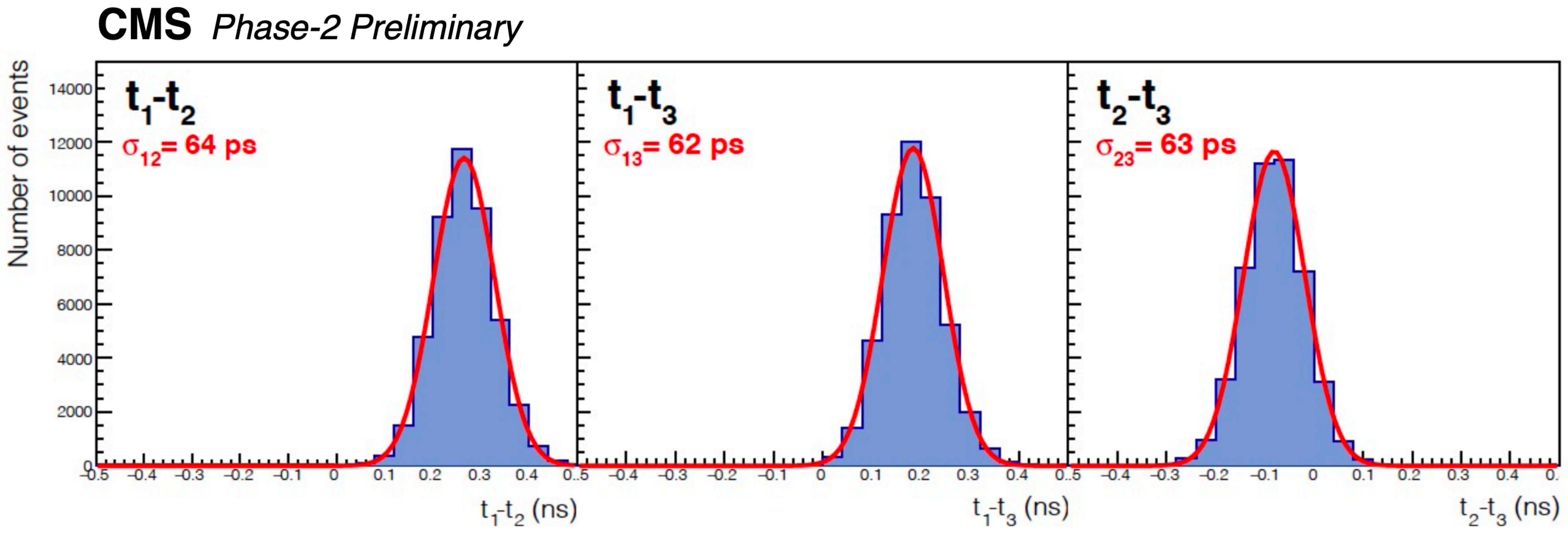
ETROC1 is the second prototype version: **4x4 pixels + TDC**

- Uses ETROC0 front-end
- ETROC **TDC brand new design optimized for low power**
- Low power (~0.1mW/pixel) achieved using simple delay cells with **self-calibration**
- Achieved **TDC resolution ~6 ps**

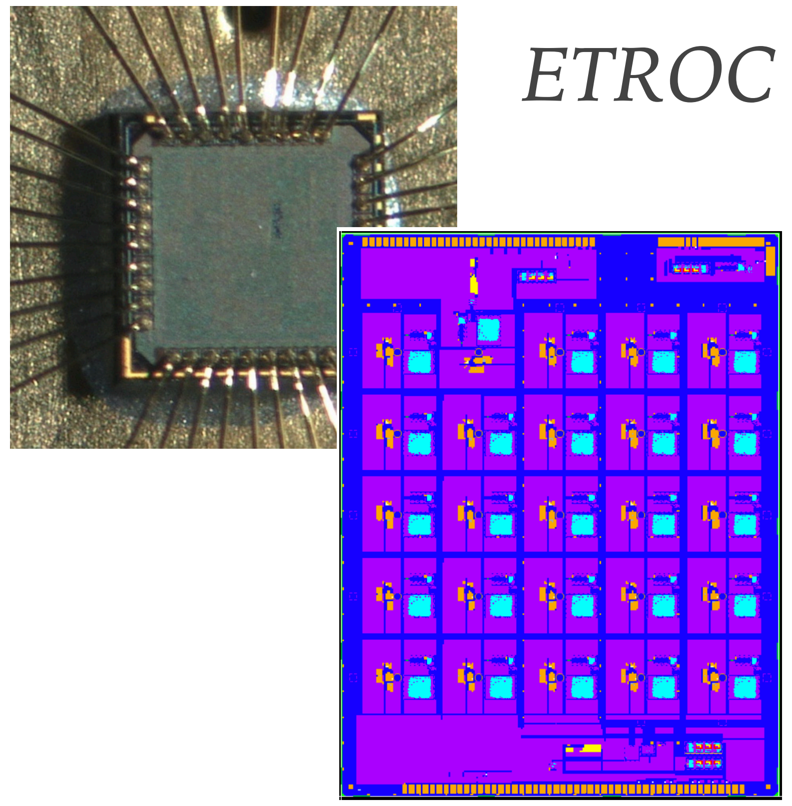
ETROC1 beam telescope at FNAL test beam facility

From preliminary analysis of the data from ongoing beam test at FNAL, **the total time resolution per hit** for each LGAD+ETROC1 layer has reached:

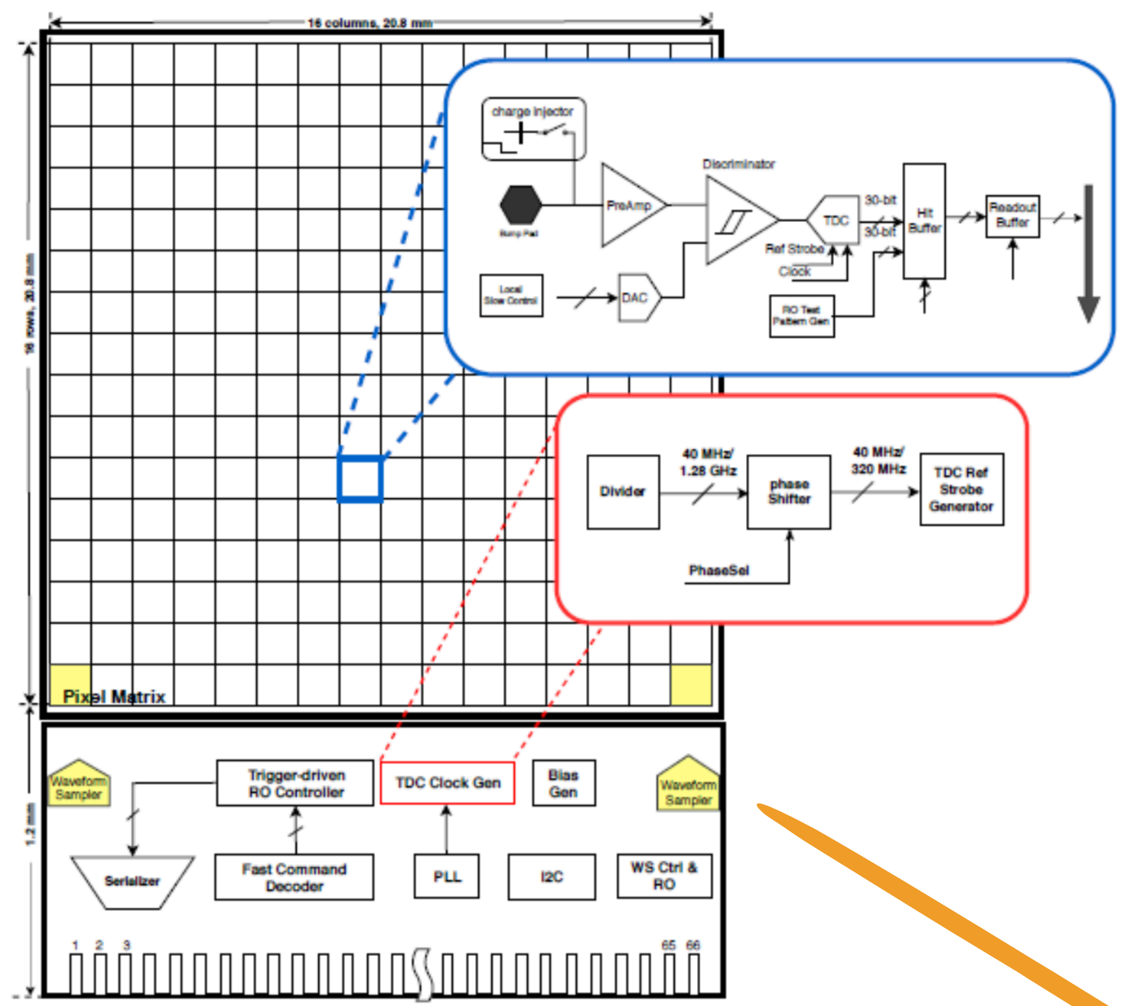
$$\sigma_i \sim 42 - 46 \text{ ps}$$



From R&D to the final detector



ETROC

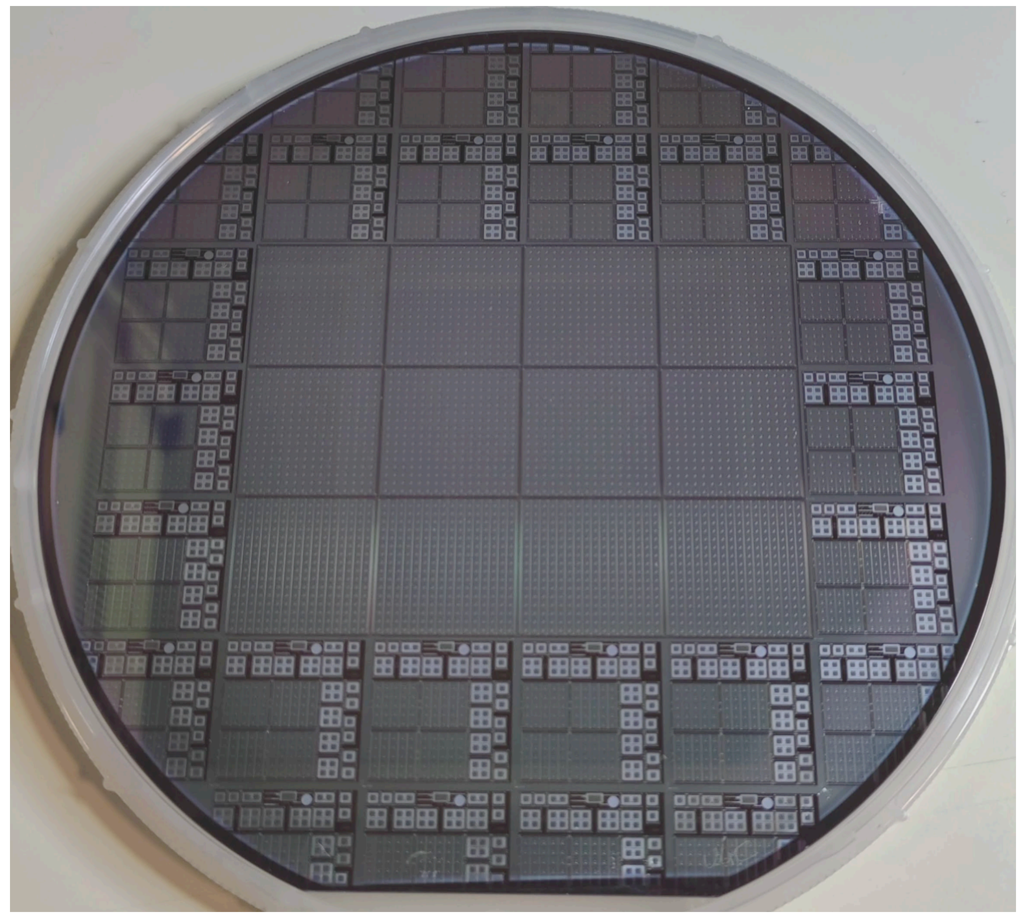


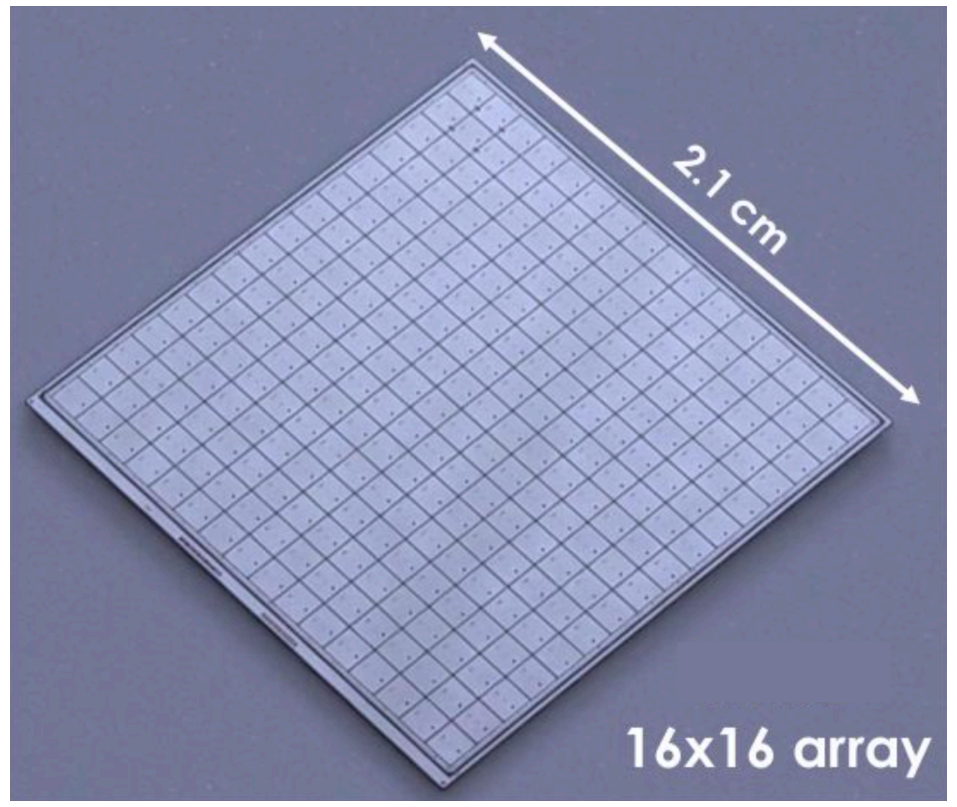
R&D productions

Strong effort to combine inputs from studies into a complete detector design and layout: **~8000 modules** (4 sensors each) on 2 endcaps

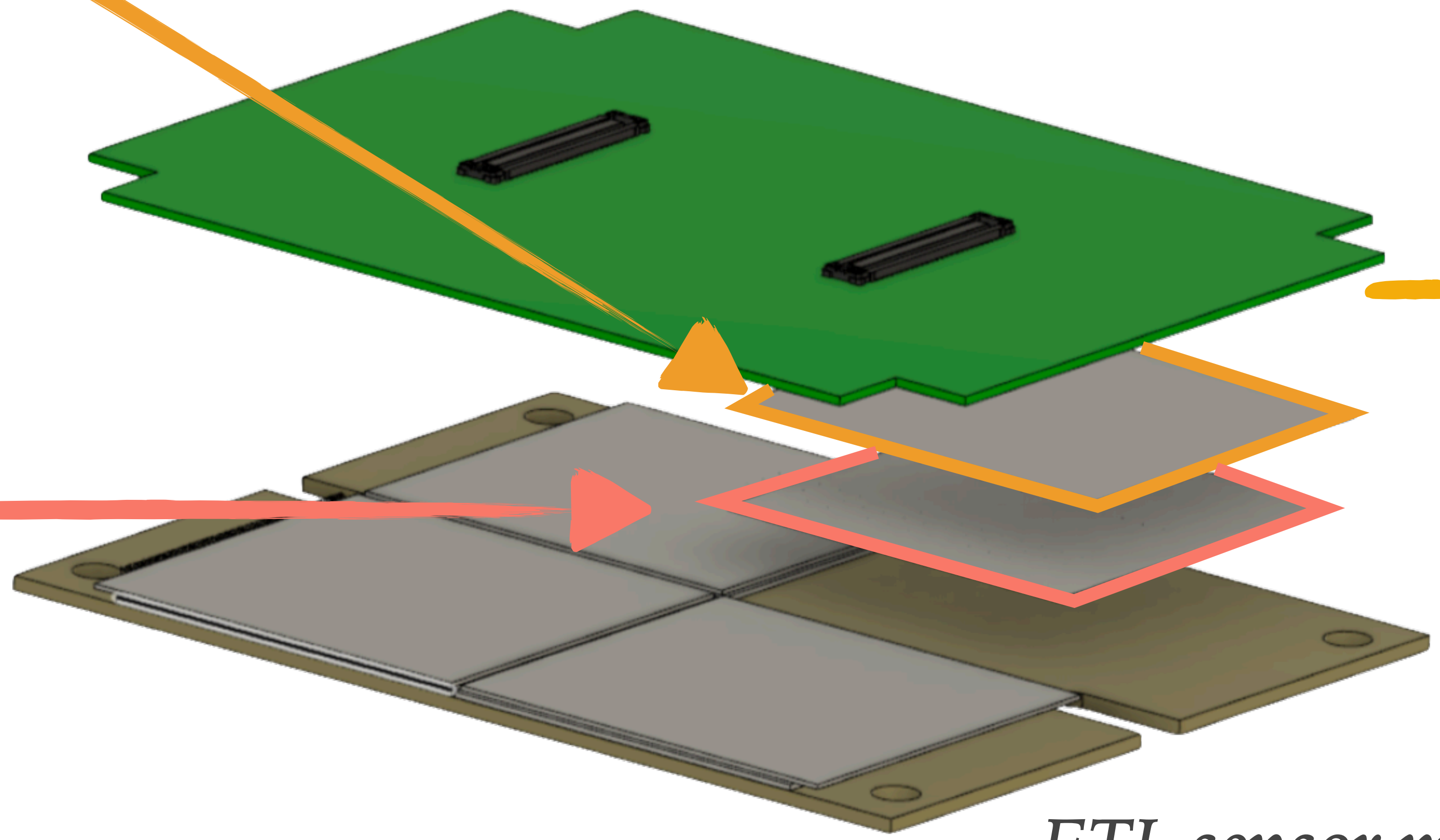
Each detector consists of **2 disks** with front and back face instrumented

Modules + front end electronics and services need to fit in **very tight mechanical envelope**

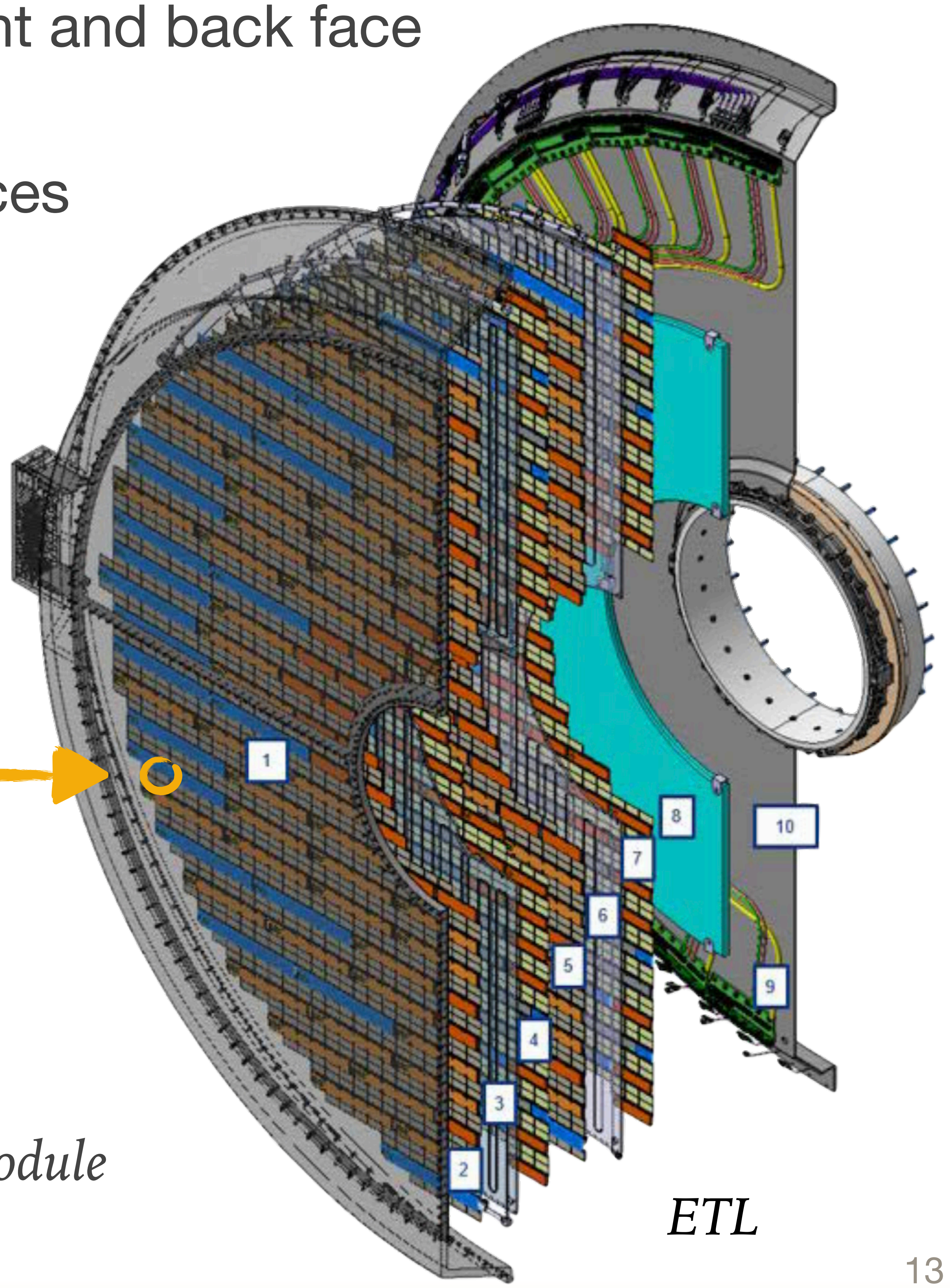




ETL sensors



ETL sensor module



ETL

ETL modules

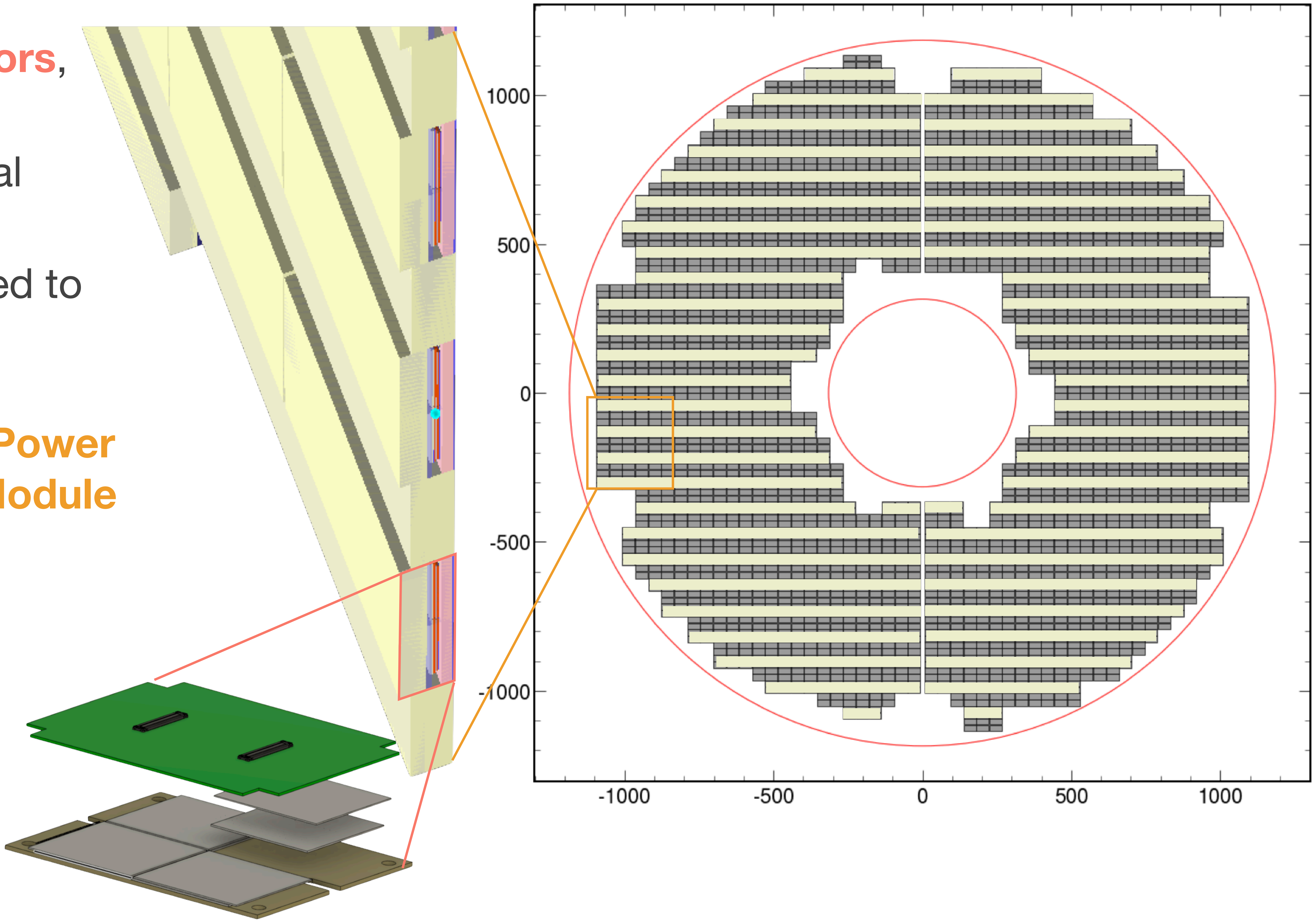
Modules are based on **4 16x16 pixel LGAD sensors**, bump bonded to **one ETROC each**

Sensors are glued on AlN baseplate and in thermal contact with the cooling

Wire bonds to PCB Modules are directly connected to multi-module readout board that sits on top disk

Readout board based on **CERNs rad-hard Low Power Gigabit Transceiver (lpGBT) and Optical Link Module (VTRx+)**

Prototype v1 (first in realistic form factor) works with ETROC2 emulator, **can test full readout chain**



Conclusions

The **CMS Endcap Timing Layer** will perform precise timing measurements of charged particles with single-hit **timing resolution <50 ps**, allowing the CMS detector to maintain its excellent performances in the very challenging environment of the HL-LHC

- ETL will be instrumented with thin **Low-Gain Avalanche Diodes** (LGADs) read-out by **ETROC ASIC**

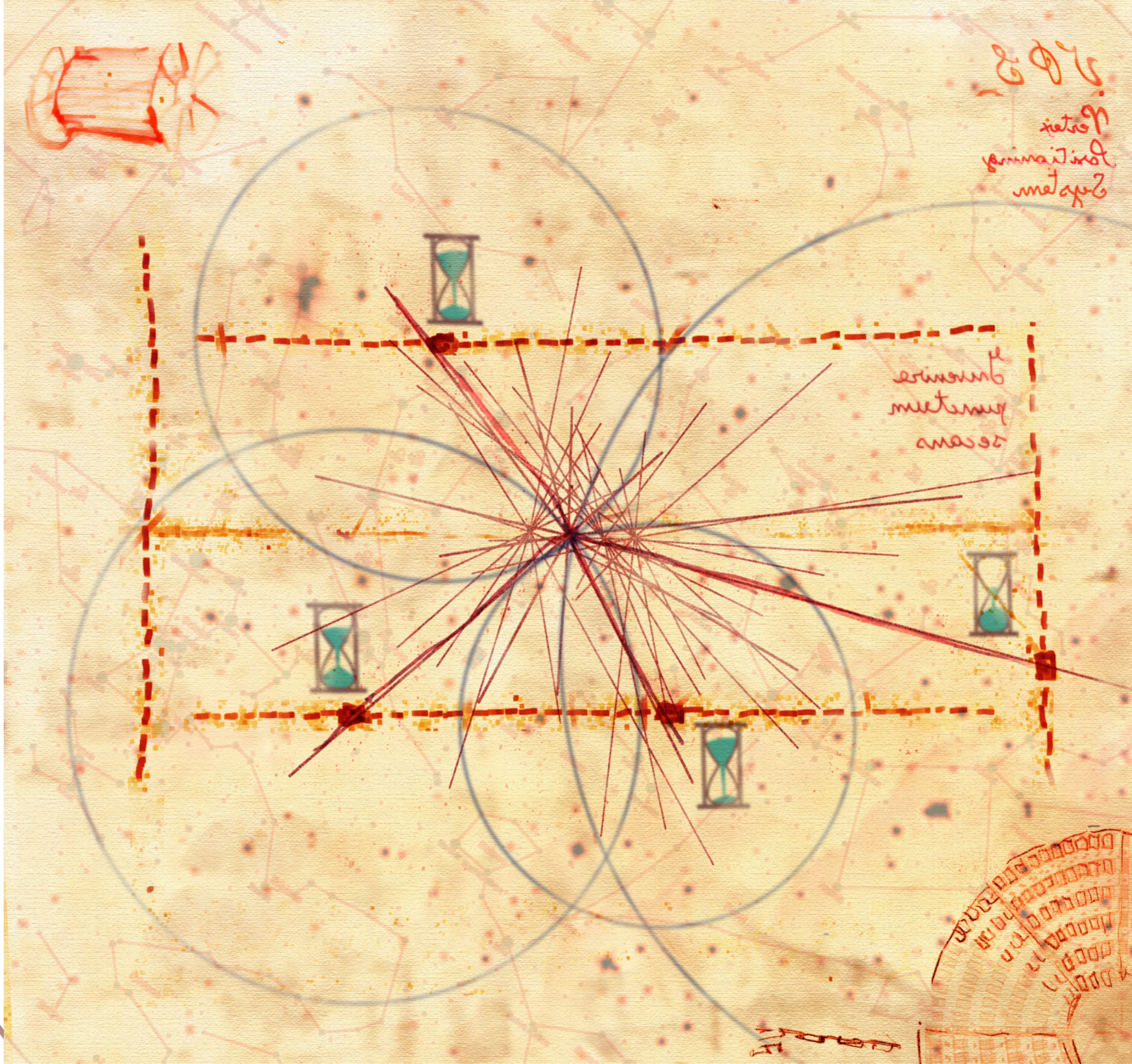
  The latest LGAD productions have been measured both in the laboratory and at test beams, to ensure they meet all the specifications: **high yield and uniformity, timing resolution <40 ps** up to the end of lifetime, **100% efficiency** and **uniform timing resolution** across the whole active area of large LGAD arrays at test beams

- The **Endcap Timing Layer Read-Out Chip** (ETROC) is required to consume low power while providing excellent timing performances
  - ❖ **ETROC1** reaches **42-46 ps time resolution**, measured at FNAL beam test
  - ❖ **ETROC2 submission soon, ETROC3 design in progress** (submission in March 2024)

- **Modules** will include 4 LGAD sensors, bonded to an ETROC each, and provided with a dedicated readout board

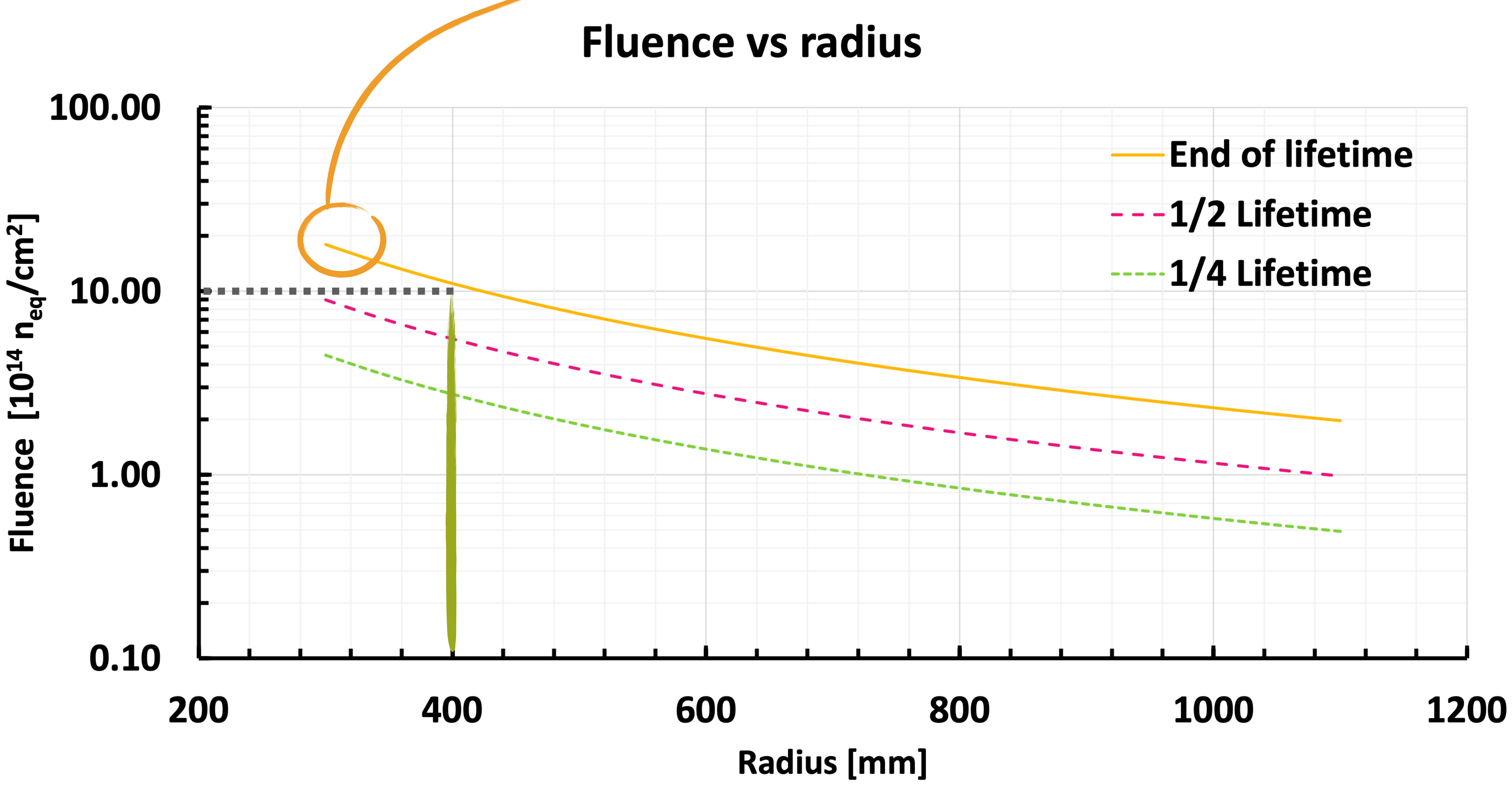
  First prototype tested with the full readout chain

BACKUP



Radiation levels for ETL

ETL will reach fluences $1.7 \times 10^{15}\ \mathrm{n_{eq}/cm^2}$ in its inner region ($|\eta| = 3.0$) at the end of the HL-LHC program



Maximum fluence reaches $2.5 \times 10^{15}\ \mathrm{n_{eq}/cm^2}$ when a 50% safety factor is applied

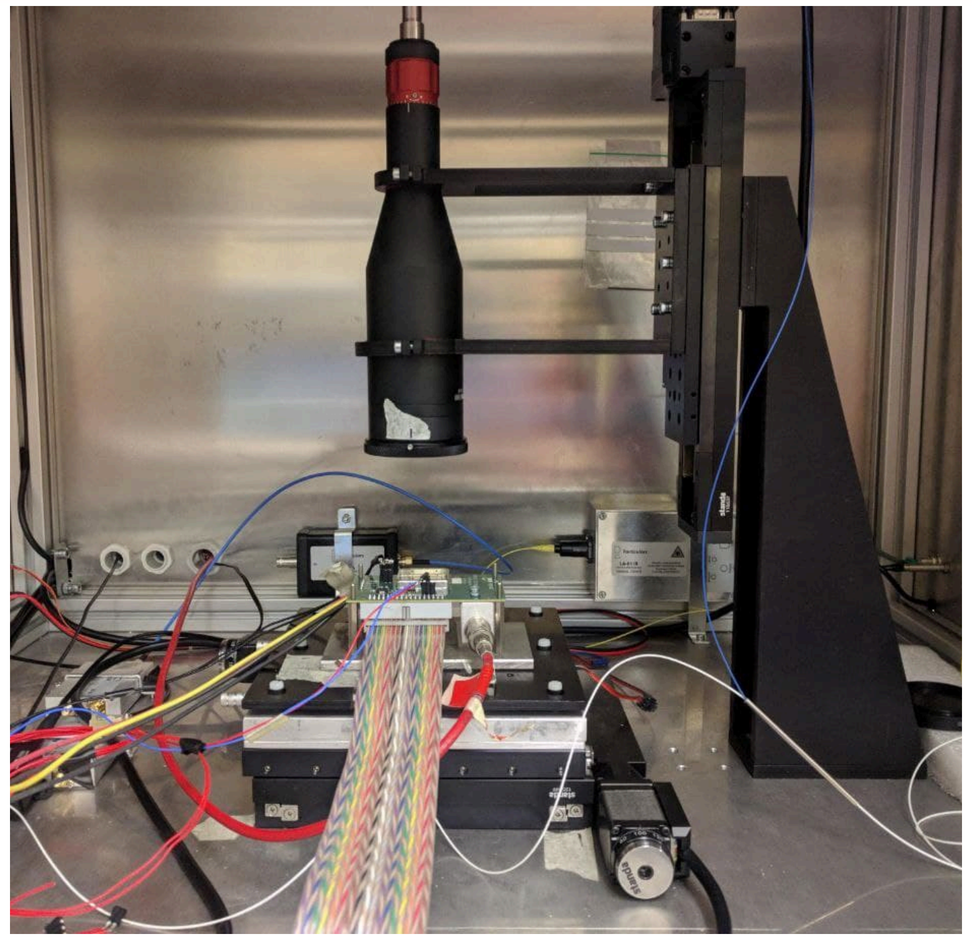
Only a small fraction of the detector surface will reach fluences higher than $1 \times 10^{15}\ \mathrm{n_{eq}/cm^2}$ after 1/2 lifetime

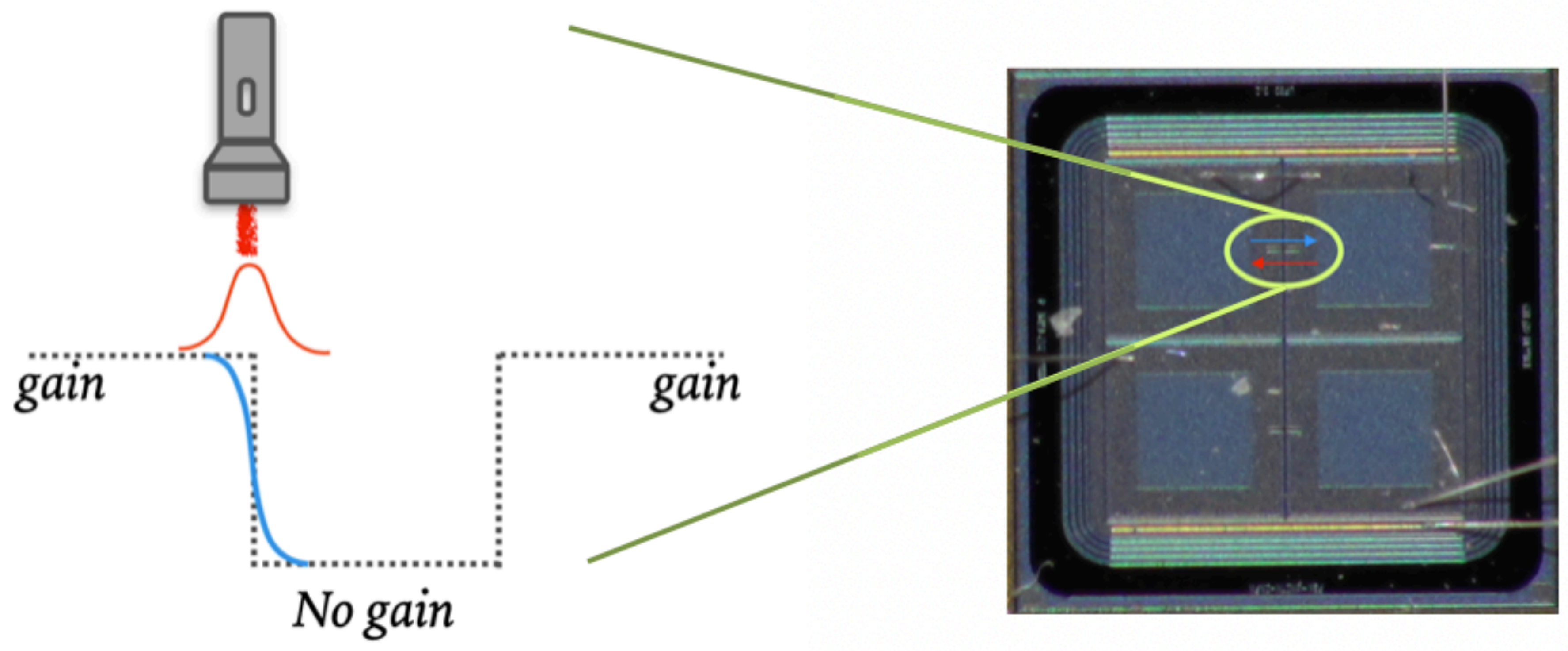
Laboratory measurements: TCT setup

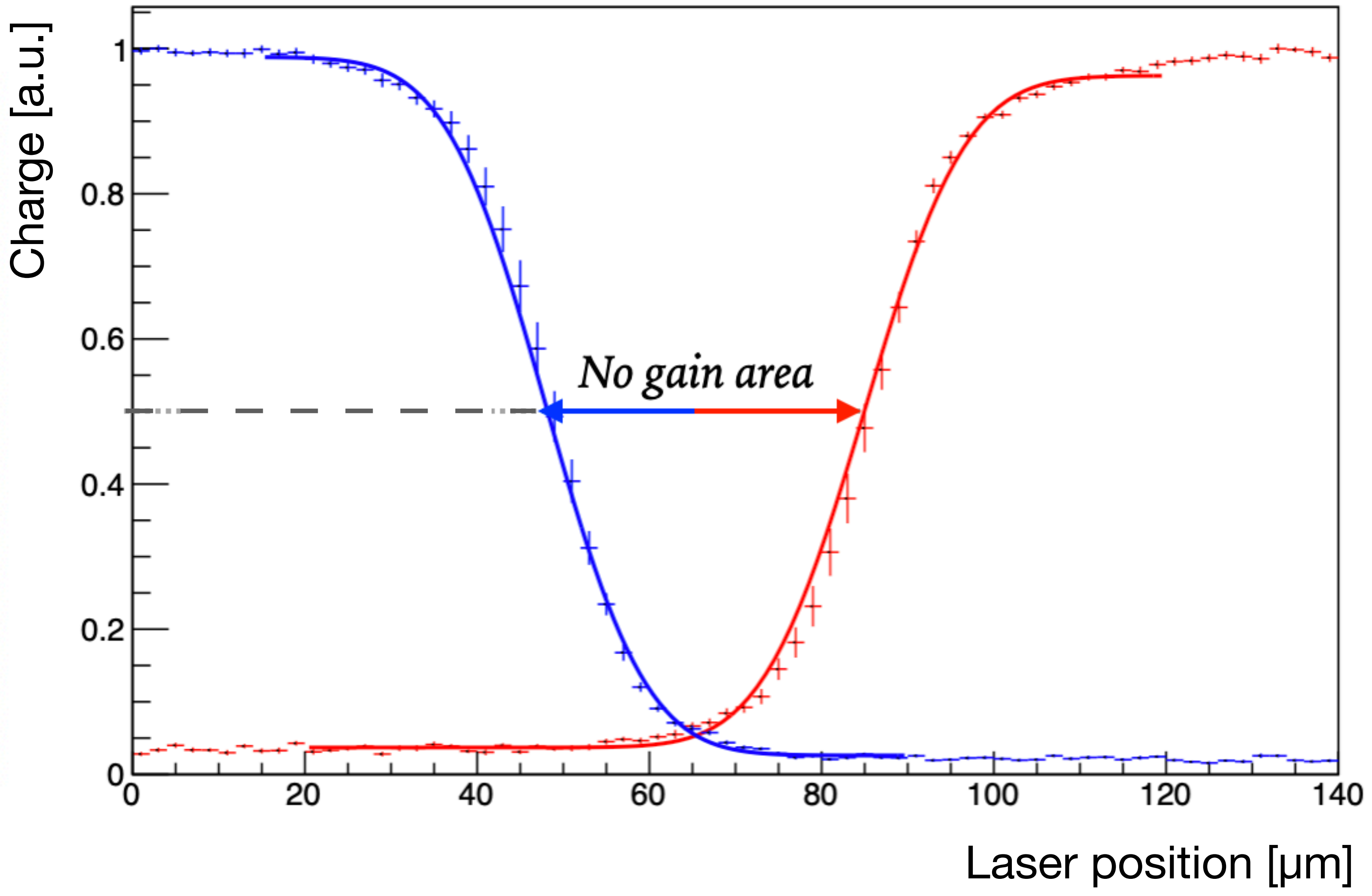
"No-gain" width measured with Particulars **Transient Current Technique** setup

→ 1D scan with a **1060 nm picosecond laser** with **~10 μm spot** along the optical window between two pads

→ Charge vs laser position fitted with an **S-curve**: convolution of **gain layer step function** and laser **gaussian beam profile**





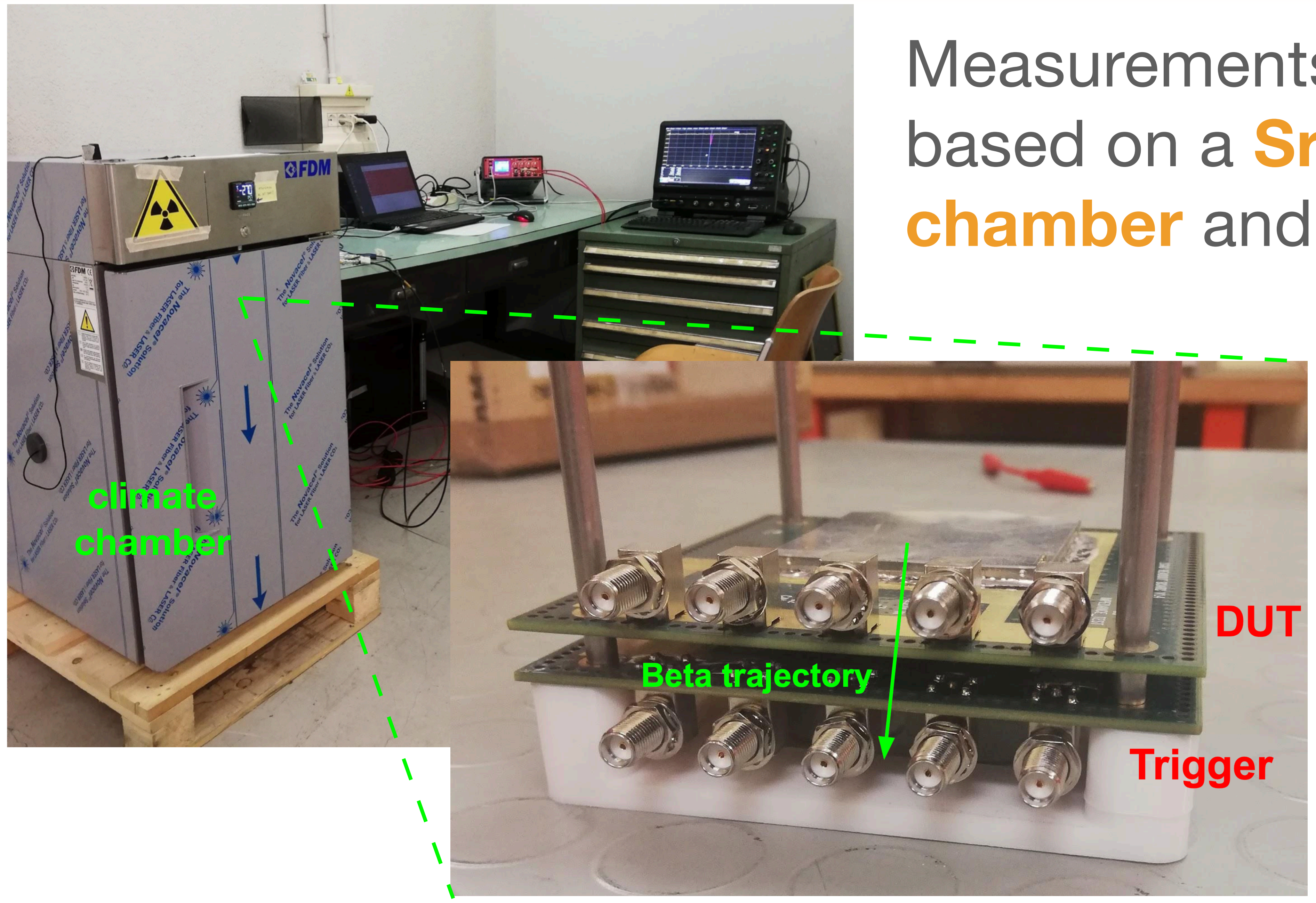


Interpad area is evaluated as the **distance between the points at 50% of the S-curve maximum** for the two measured pads

The results obtained with laser have been confirmed at test beam

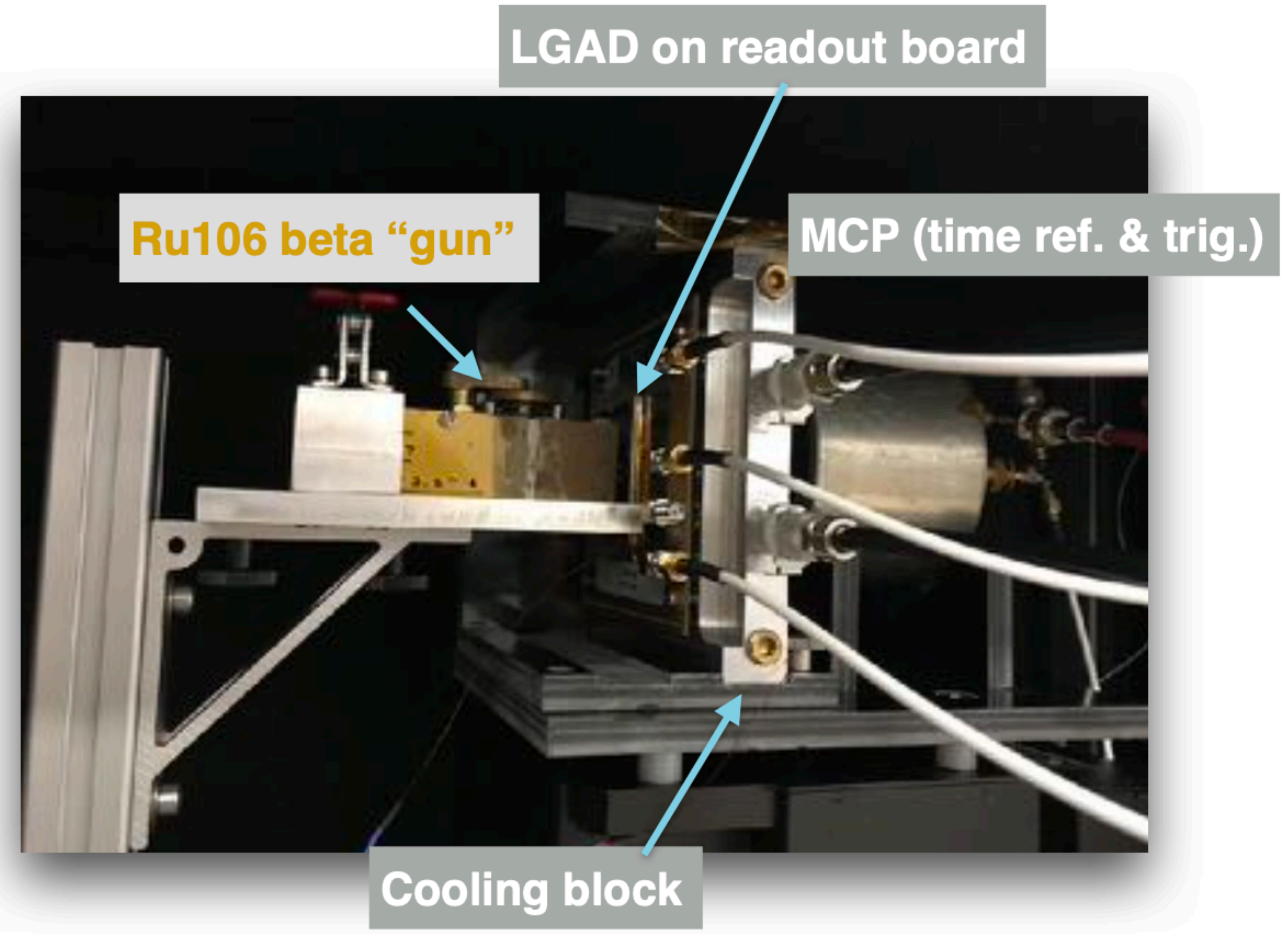
Study of interpad-gap of HPK 3.1 production LGADs with Transient Current Technique, S. Bharthuar et al., NIM A 979 (2020) 164494, DOI: 10.1016/j.nima.2020.164494

Laboratory measurements: time resolution setup



Measurements on FBK production performed with the **Torino Beta-source setup** based on a **Sr90 source** and provided with a **DUT+trigger telescope** in a **climate chamber** and an automated DAQ and analysis system

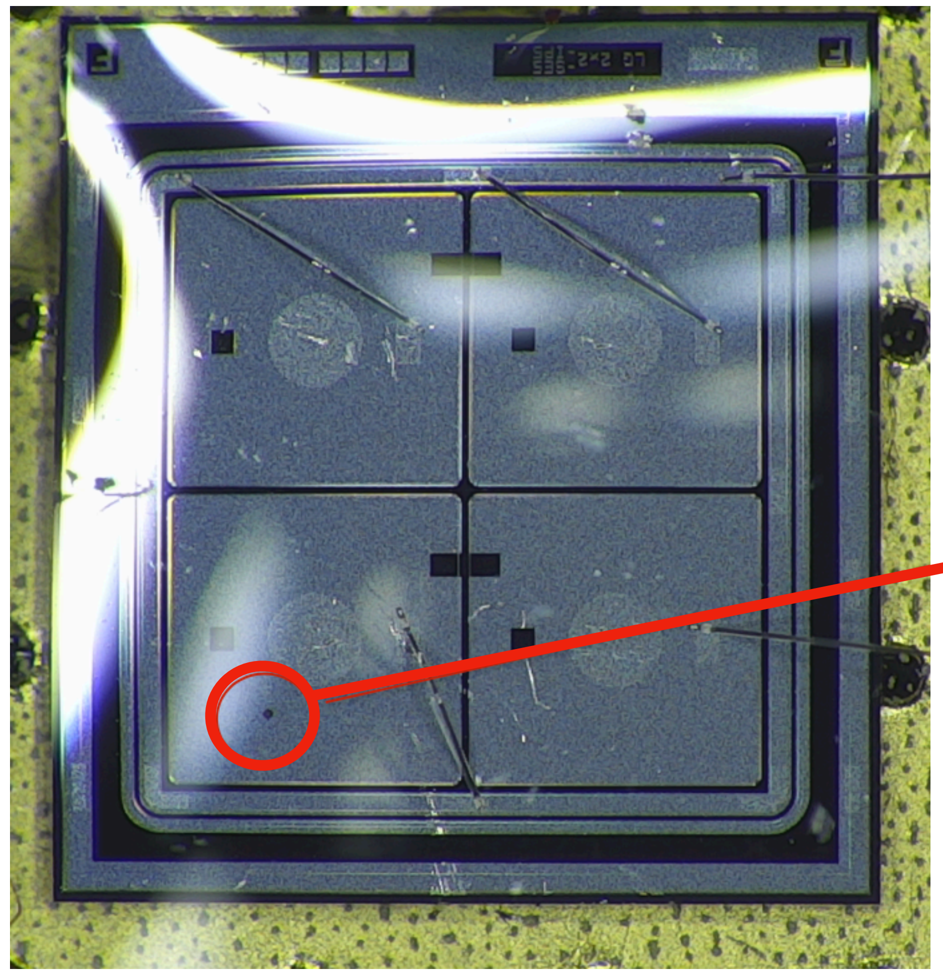
Results on FBK production obtained at **Fermilab SiDet Laboratory** with a setup equipped with a **Sr90 source, DUT** mounted on a **cooling block** and an **MCP** used as time reference and trigger

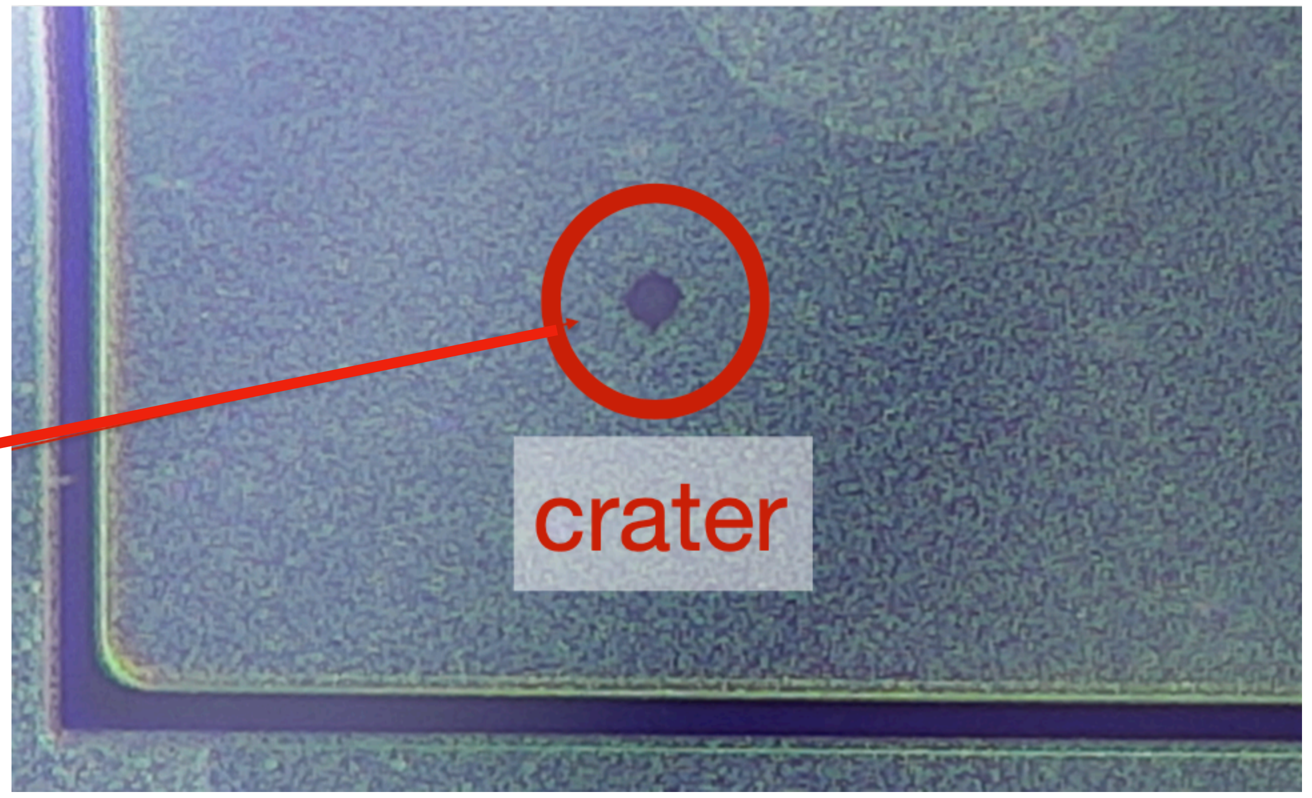


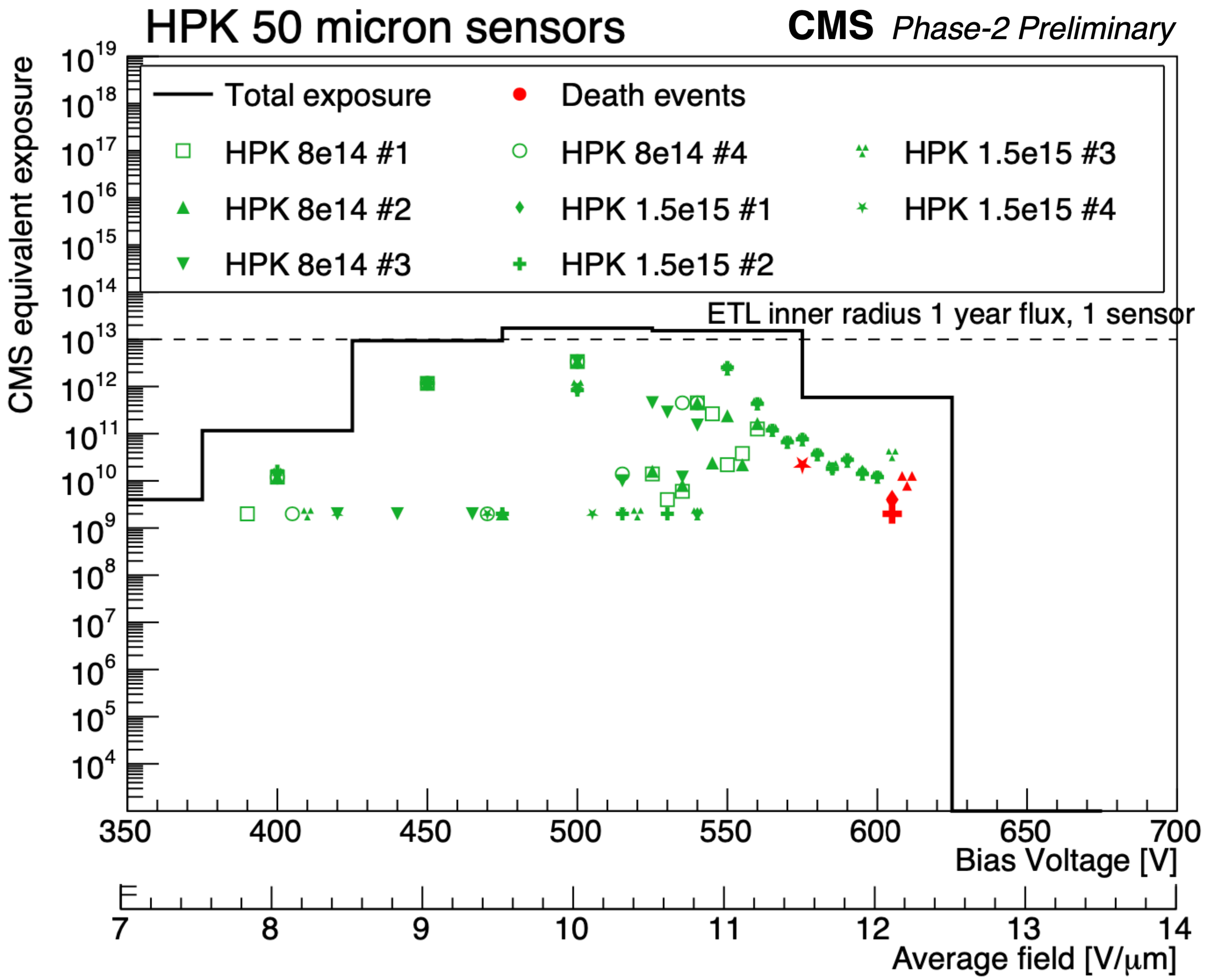
Test beam results

Irradiated LGAD sensors found to be susceptible to sudden death when operated with BV corresponding to ≥ 12V/µm

Caused by **"single event burnout"** from rare, large ionizing events (HIP) where excess charge leads to highly localized conductive path

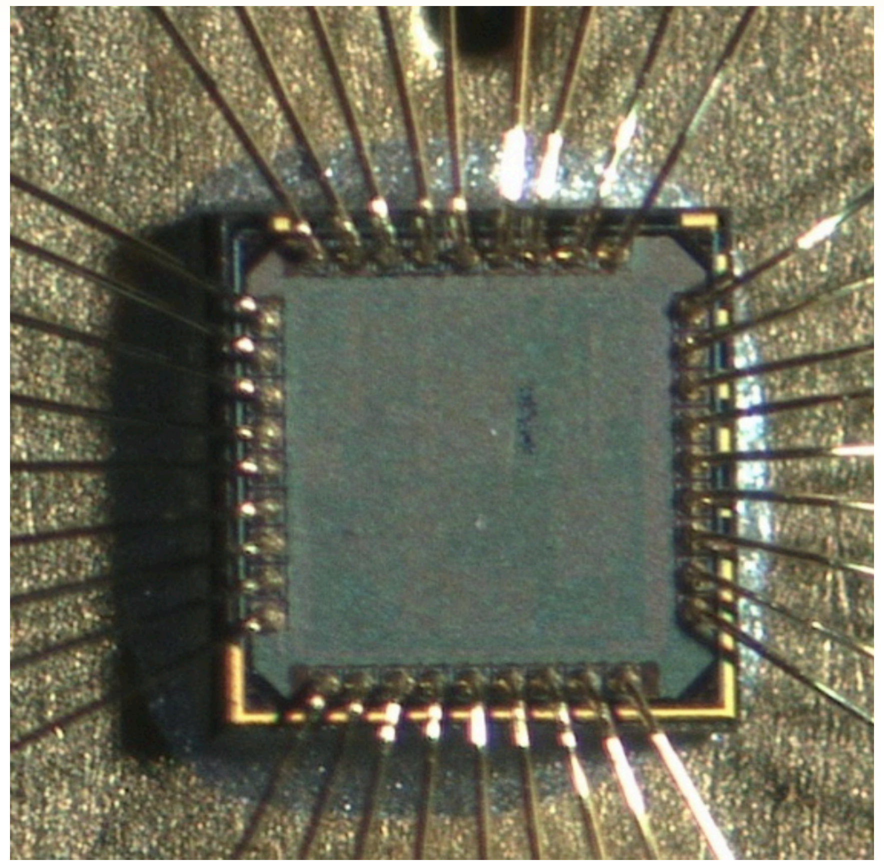






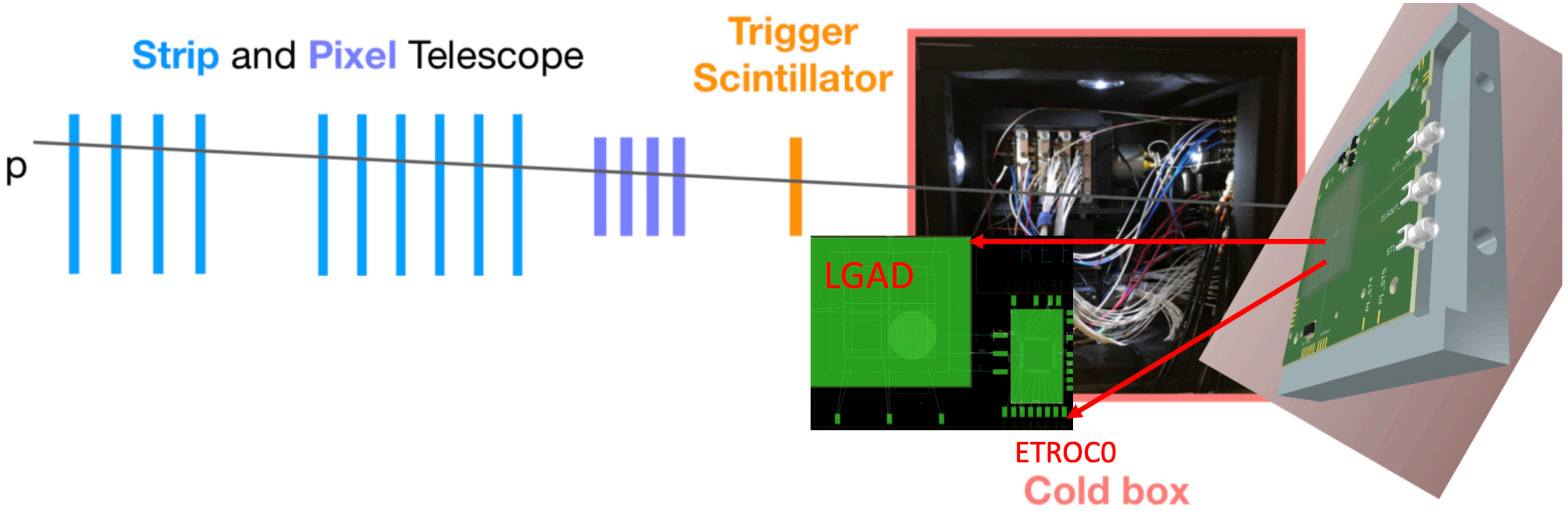
High-rate test beam at FNAL demonstrate **survival of irradiated LGADs at <12V/µm** under a flux corresponding to ~1 year running for the sensors in ETL inner region

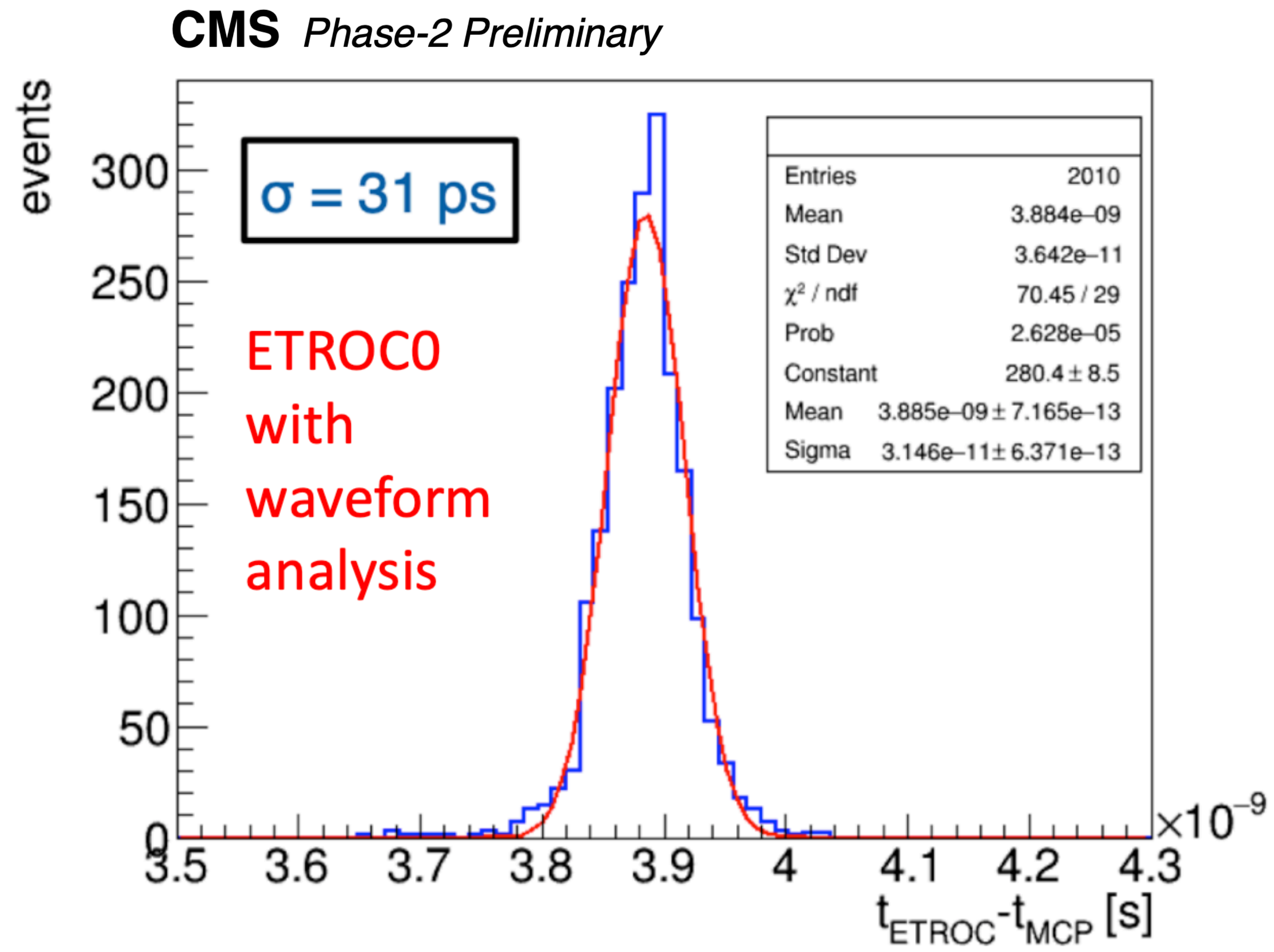
ETROC0



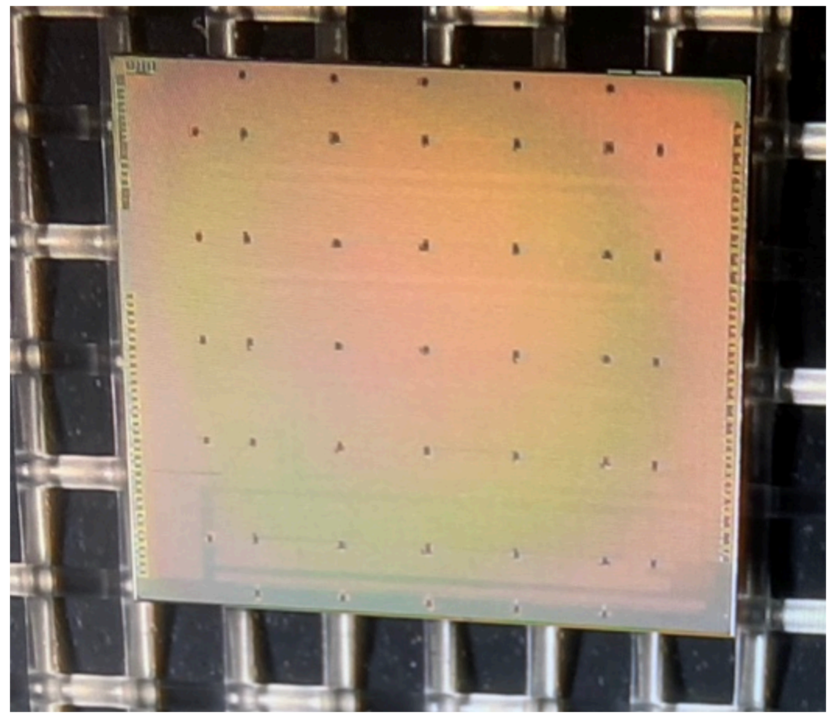
Goal: **measure core front-end analog performance**

- Jitter measurements agree with chip post-layout simulation
- Power consumption for preamp and discriminator consistent with expectation
- **31 ps timing resolution** achieved at FNAL test beam with ETROC0+LGAD



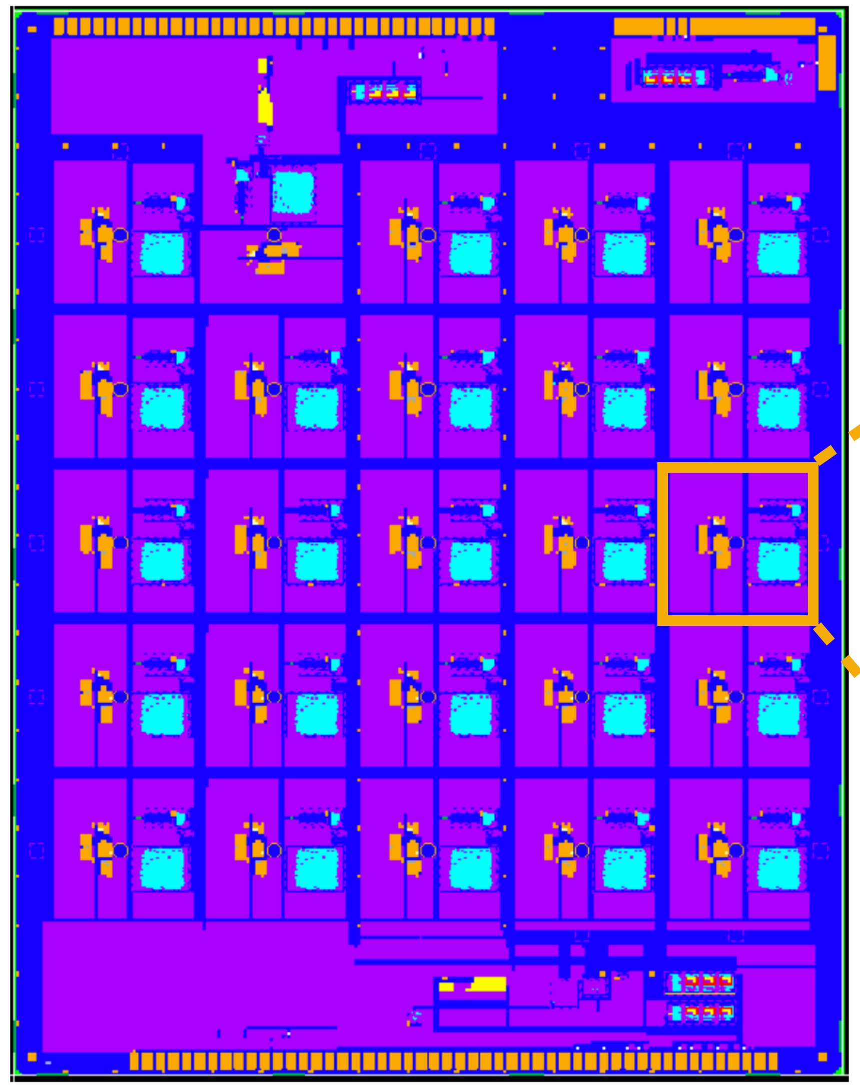


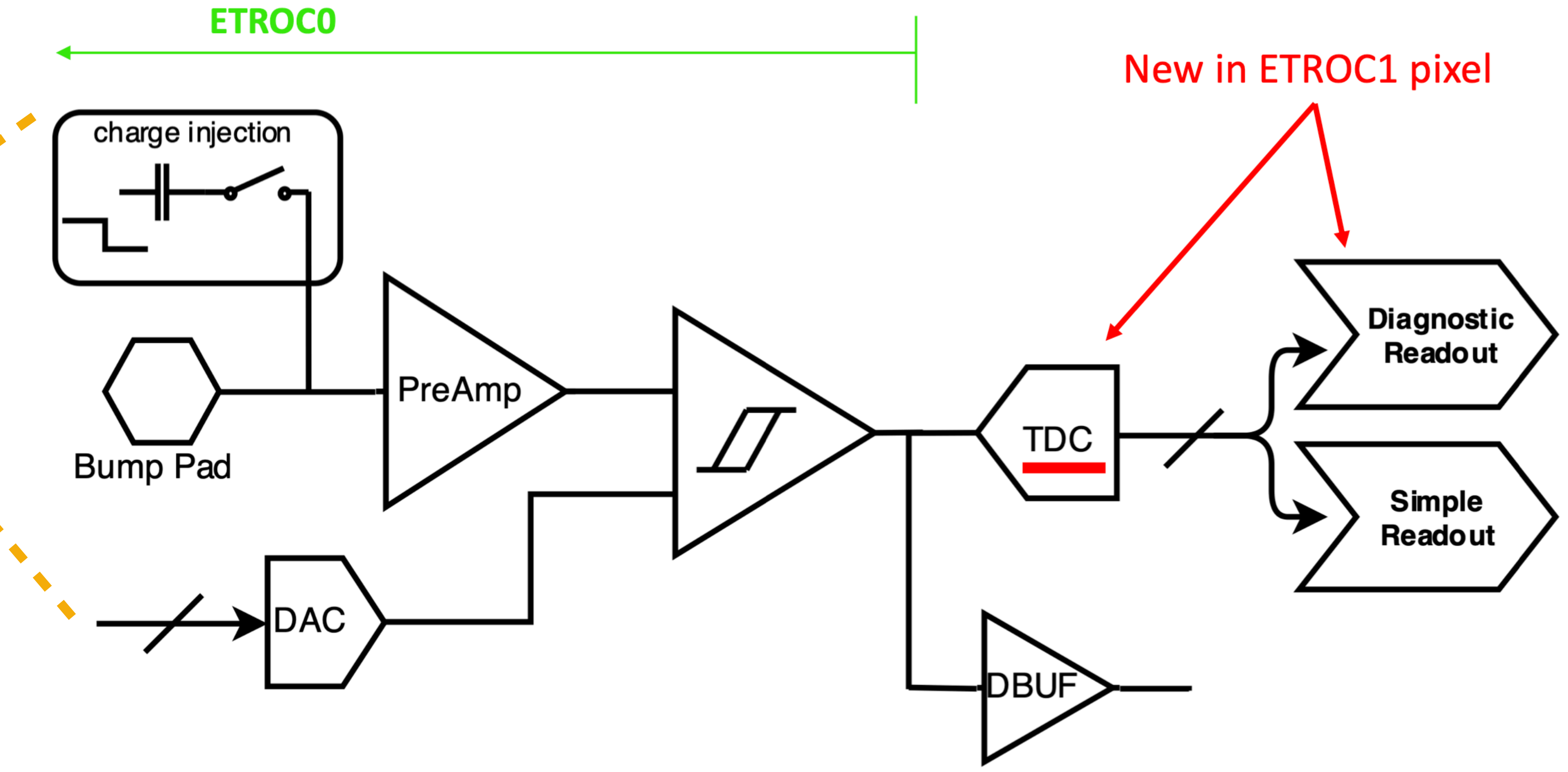
ETROC1



ETROC1 is the second prototype version: **4x4 pixels + TDC**

- Uses ETROC0 front-end
- ETROC **TDC brand new design optimized for low power**
- Low power achieved using simple delay cells with **self-calibration**
- Achieved **TDC resolution ~6 ps**





40 MHz noise observed on bump-bonded ETROC1 + LGAD

- Coupled through the sensor due to 40MHz clock activity in the circular buffer memory
- The noise is very high and is suppressed by a discriminator threshold of ~8 fC
  - → Understood and mitigated in new designs

ETL services