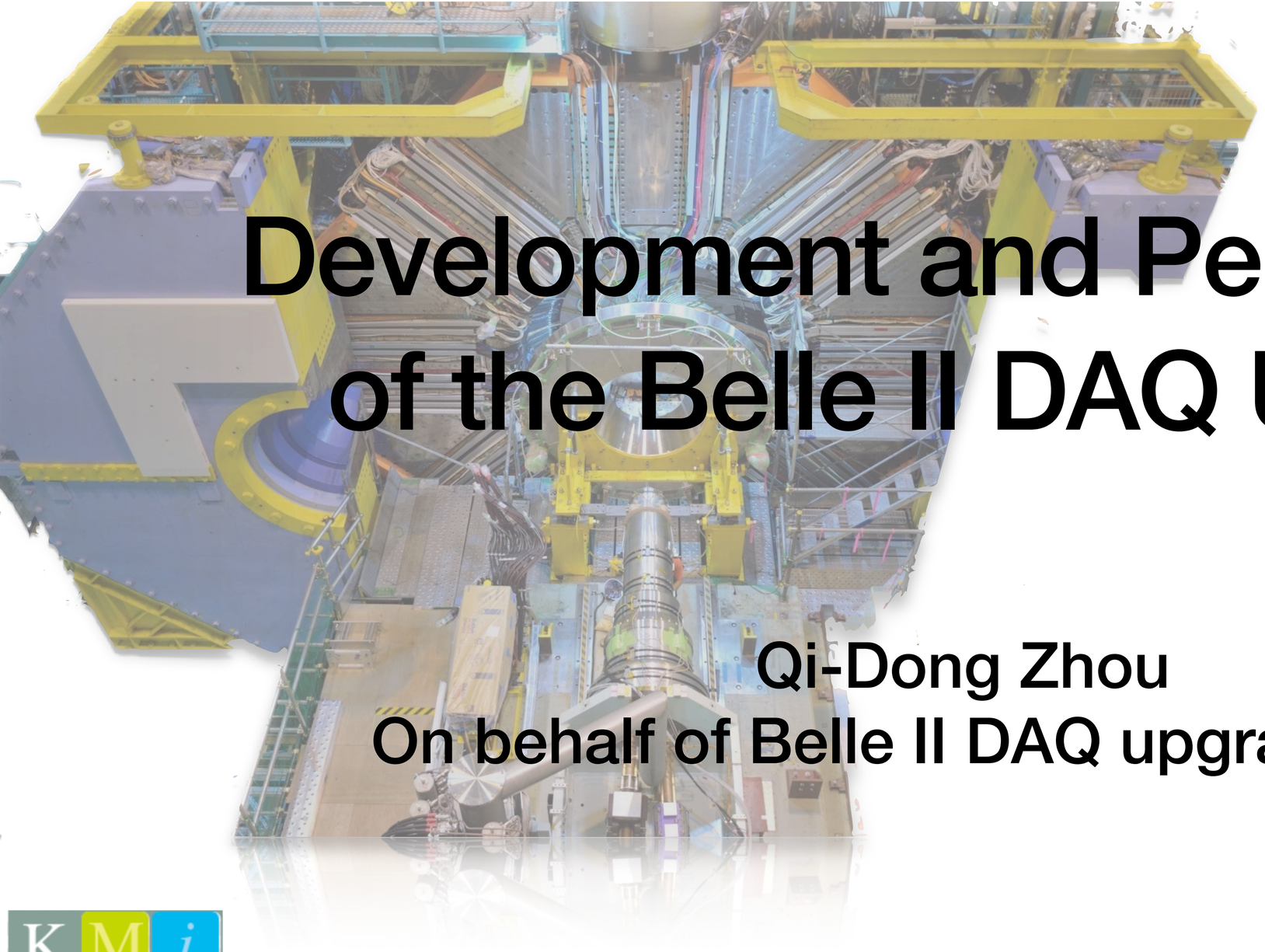
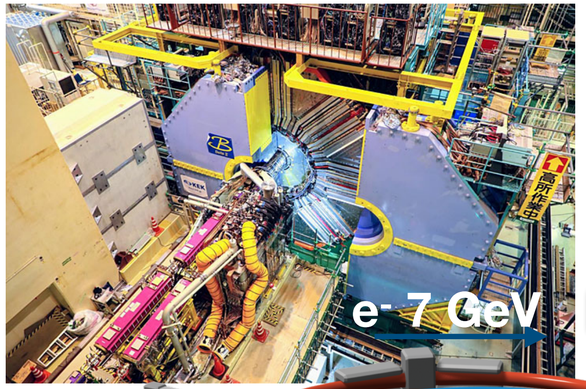


Development and Performance of the Belle II DAQ Upgrade

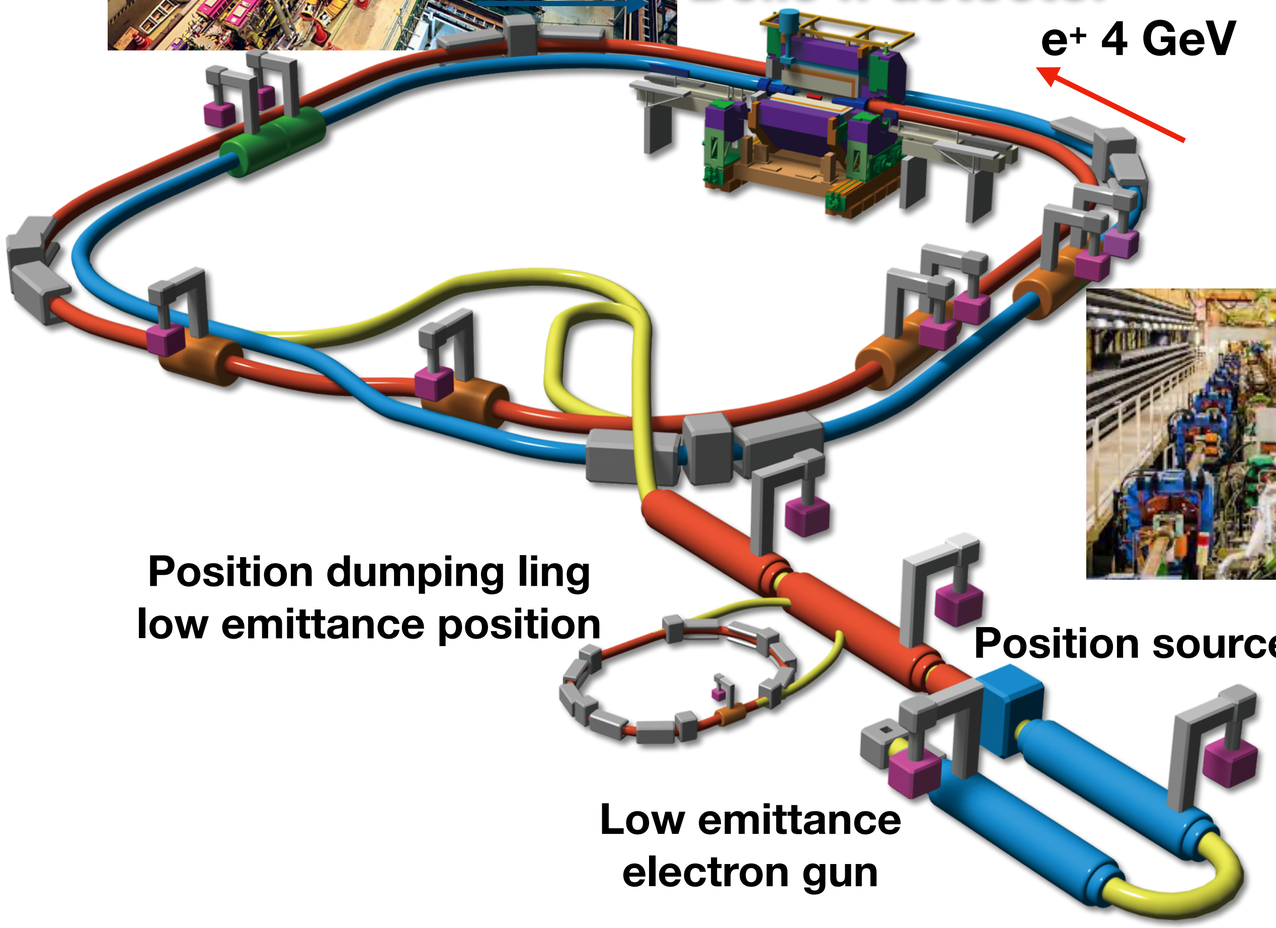
Qi-Dong Zhou
On behalf of Belle II DAQ upgrade group

Jul. 6-14, 2022, Bologna, Italy
International Conference on High Energy Physics (ICHEP2022)

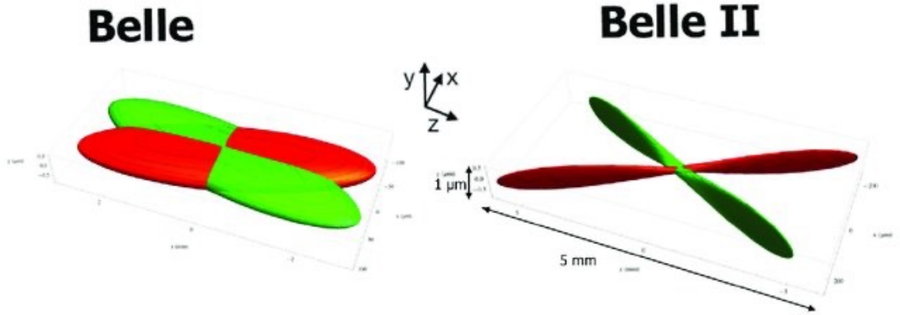
Luminosity frontier: SuperKEKB/Belle II



- Asymmetric e^+e^- collider operating at $\Upsilon(4S)$ resonance
- Squeeze the beam σ_y^*~50 nm
- Large crossing angle



Nano beam scheme



Beam current: KEKB x 1.7

$$L = \frac{\gamma_\pm}{2er_e}\left(1+\frac{\sigma_y^*}{\sigma_x^*}\right)\frac{I_\pm \xi_{\pm y}}{\beta_y^*}\left(\frac{R_L}{R_y}\right)$$

Beam squeeze: KEKB / 20

World's highest instantaneous luminosity:

$\mathcal{L}$ = 4.65 x 10^{34} cm^{-2} s^{-1}

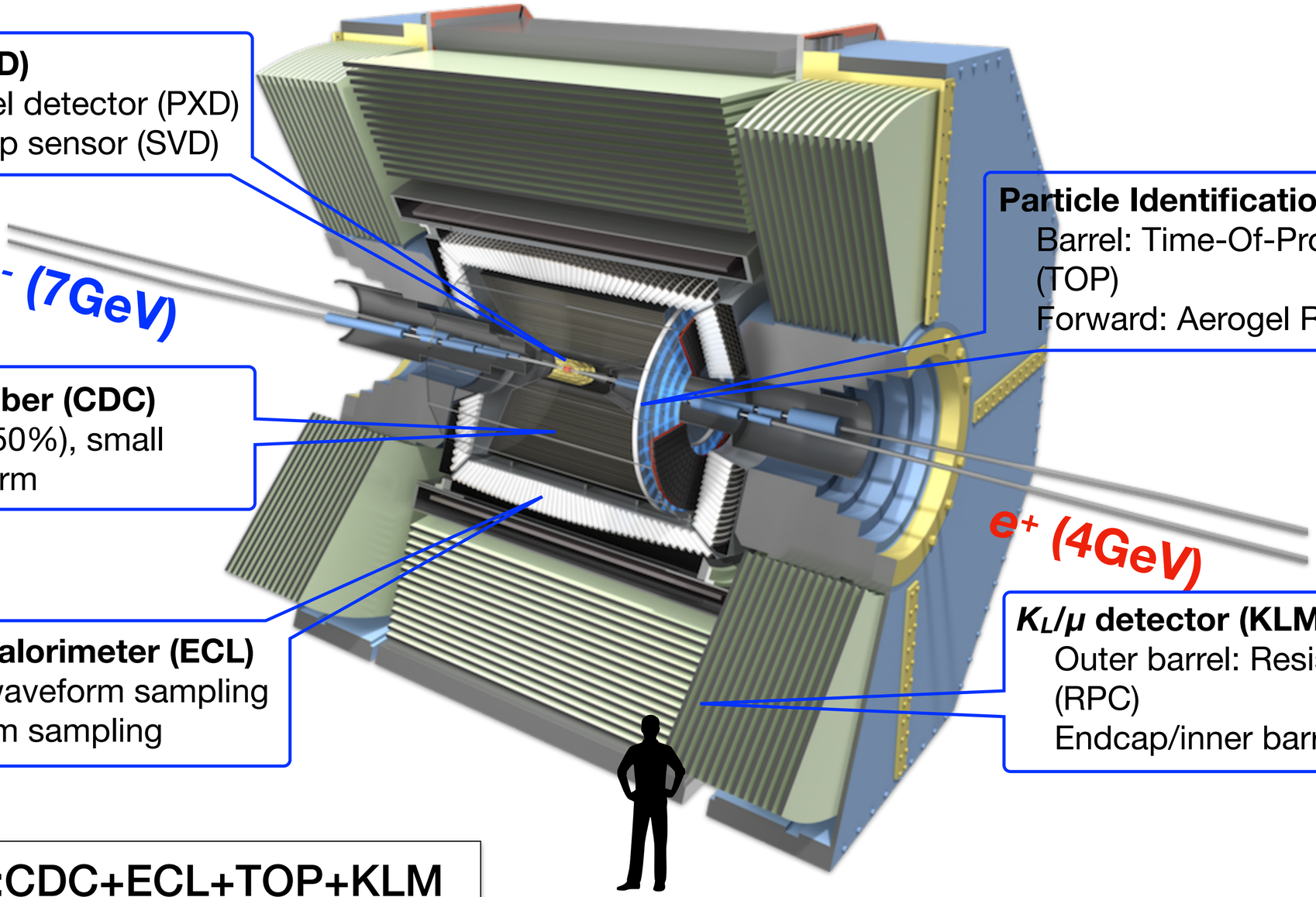
KEKB record: 2.1 x 10^{34} cm^{-2} s^{-1}

The Belle II detector

Vertex detector (VXD)
Inner 2 layers: pixel detector (PXD)
Outer 4 layers: strip sensor (SVD)

Central Drift Chamber (CDC)
He (50%), C_2H_6 (50%), small cells, long lever arm

ElectroMagnetic Calorimeter (ECL)
Barrel: CsI(Tl) + waveform sampling
Endcap: waveform sampling



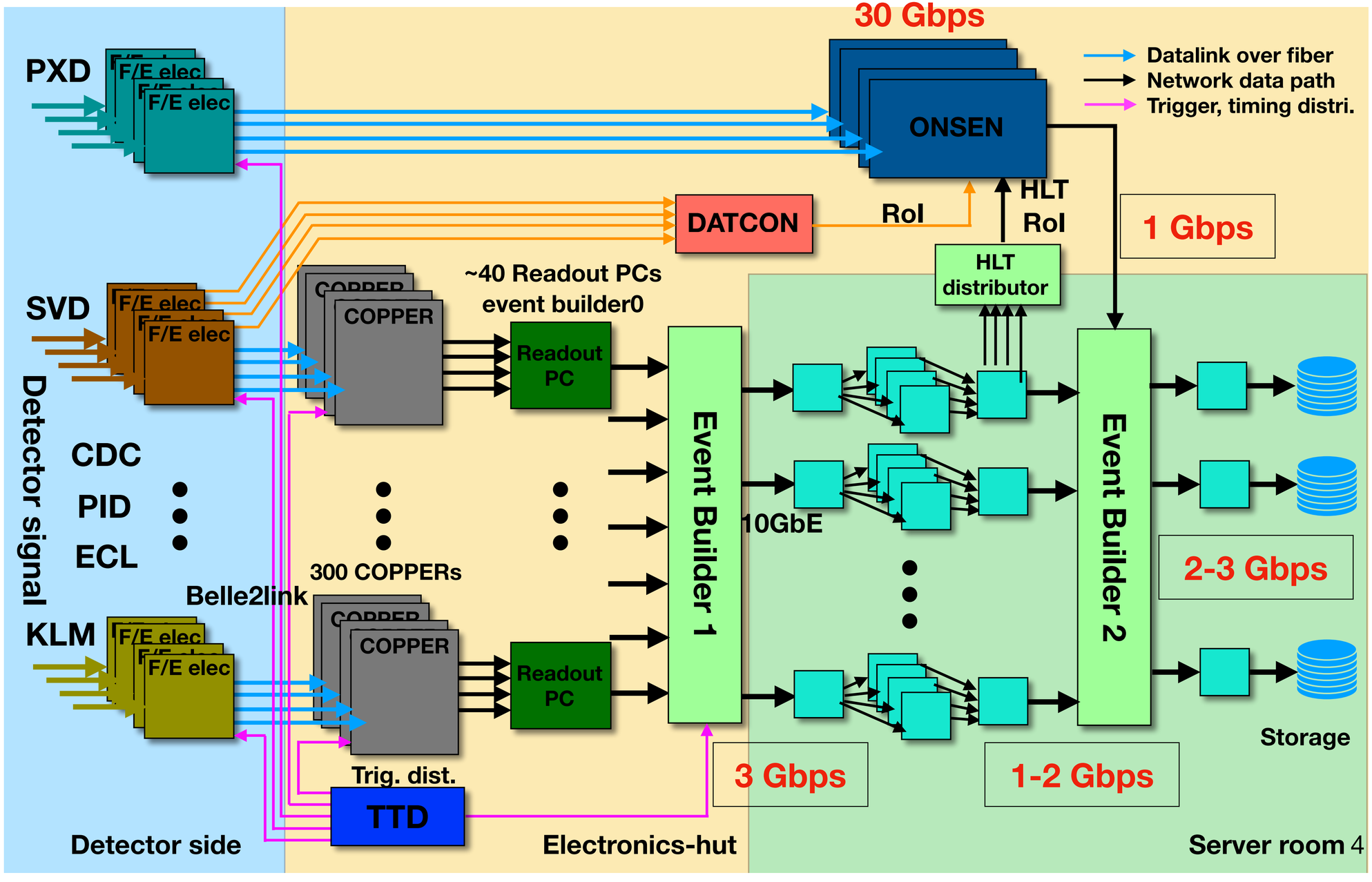
Particle Identification
Barrel: Time-Of-Propagation counters (TOP)
Forward: Aerogel RICH (ARICH)

K_L/μ detector (KLM)
Outer barrel: Resistive Plate Counter (RPC)
Endcap/inner barrel: Scintillator

Level-1 trigger :CDC+ECL+TOP+KLM
DAQ: Maximum 30 kHz L1 trigger

Belle II DAQ system

- Unified common readout system (except for PXD)
- Unified timing and trigger distribution (TTD) system
- A pipeline readout
- To handle 30 kHz level 1 trigger with O 1% dead time under raw event size of 1 MB



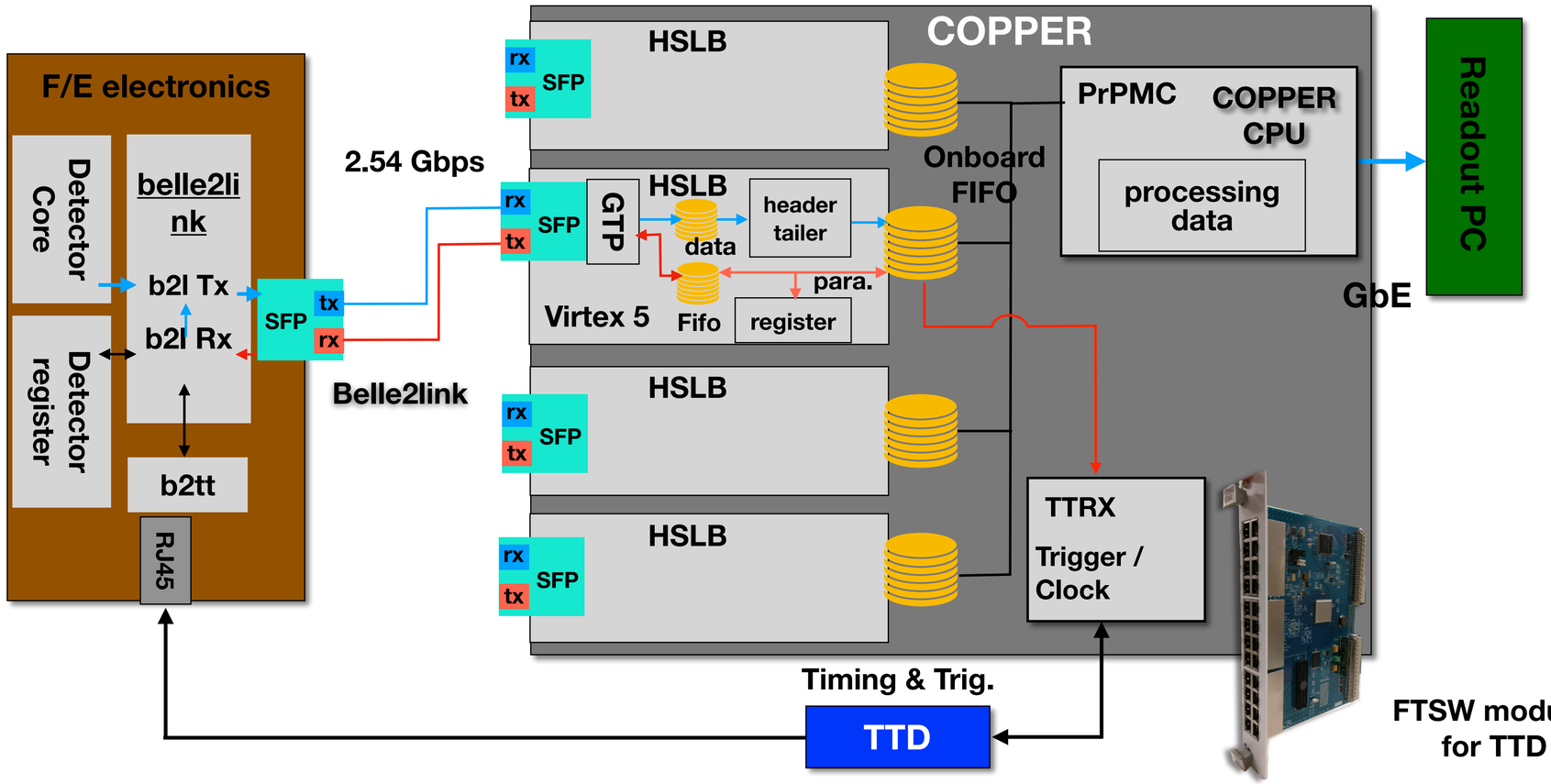
Belle II DAQ readout system

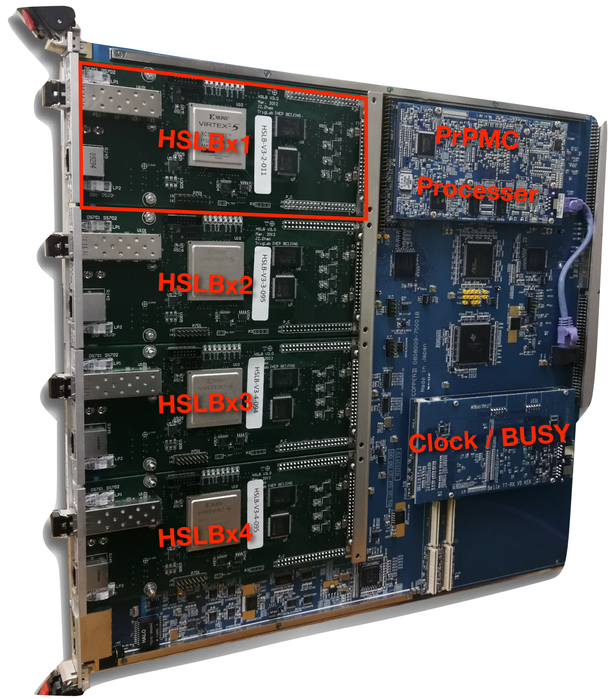
Belle2link:

Unified high speed optical link (2.54Gbps) connected Front-End Electronics and DAQ readout board (COPPER-HSLB), data transmission based on Rocket I/O.

Functionalities of readout system

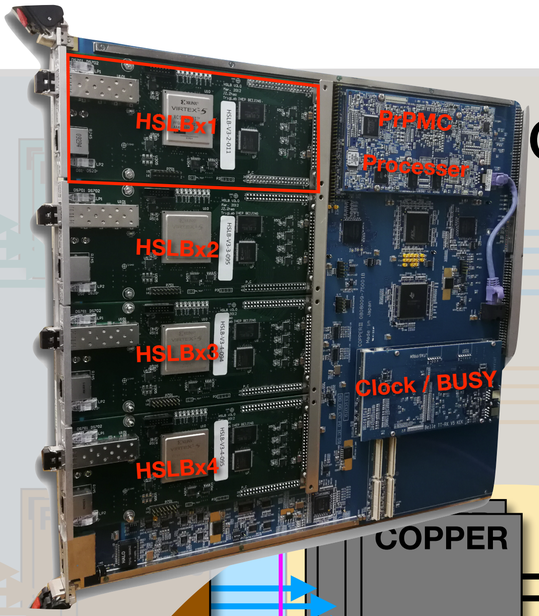
- Belle2link,
- TTD interface,
- slow control
- pre event-building, GbE
- Data-formatting
- Data-check





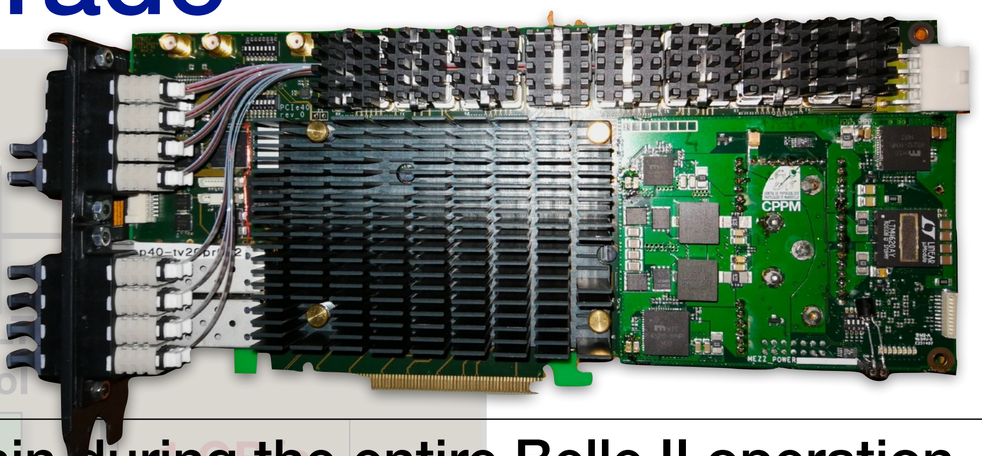
FTSW module for TTD

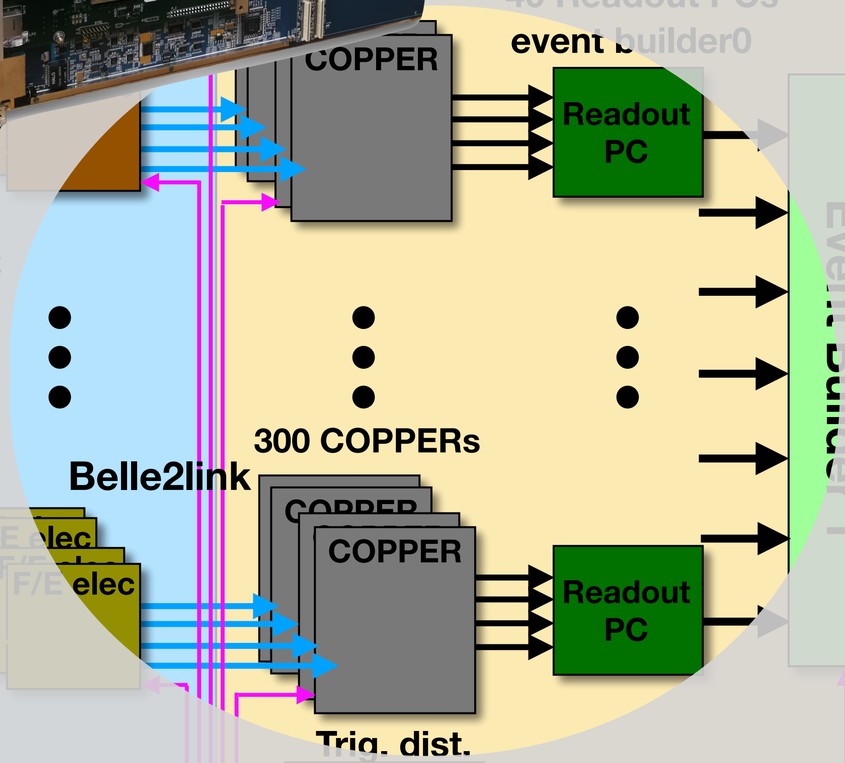
Belle II DAQ upgrade



COPPER

PCIe40
(LHCb, ALICE)

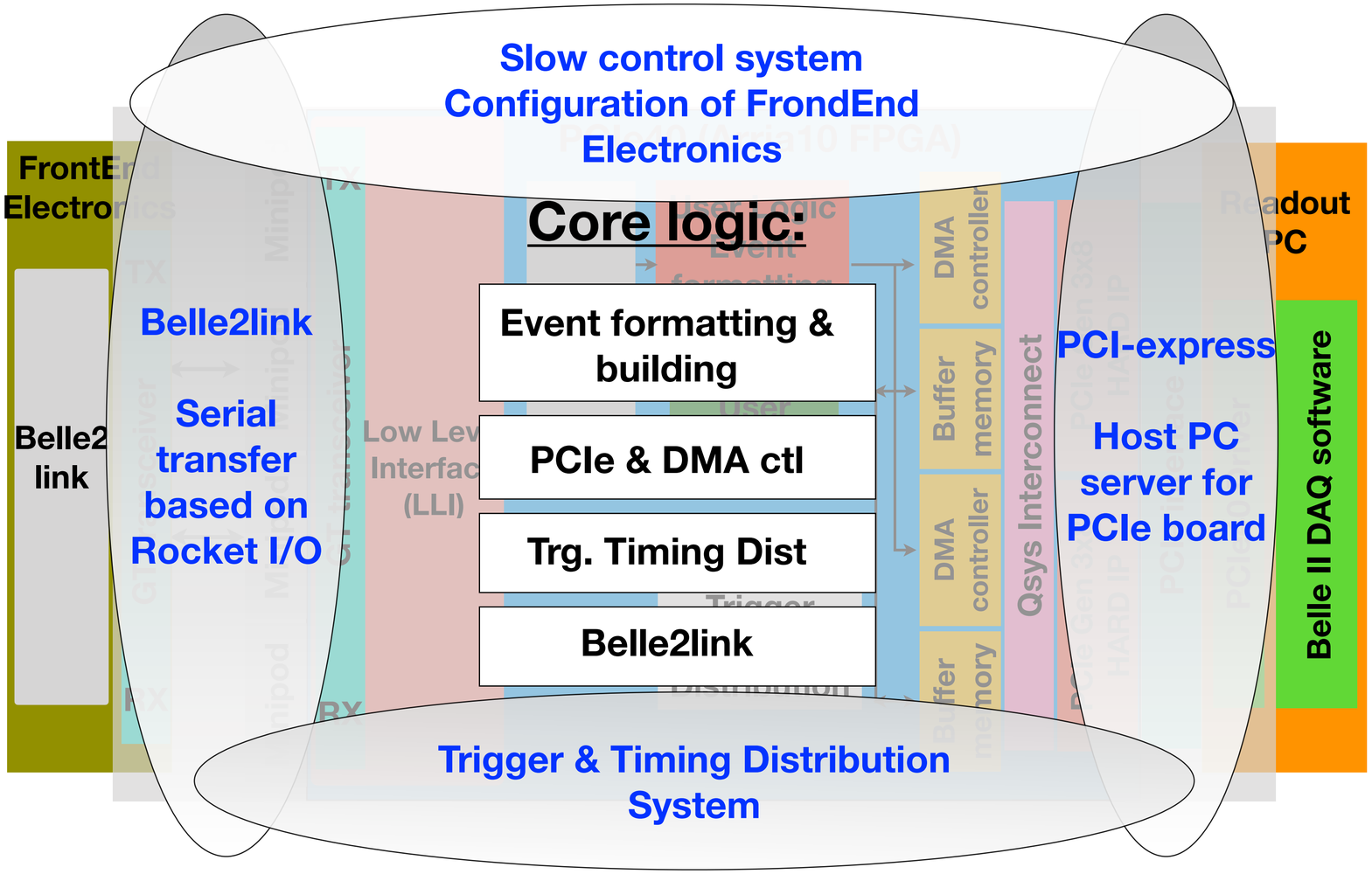




- ✦Difficult to maintain during the entire Belle II operation period, COPPER has been used for Belle experiment
  - Four different boards
  - Broken parts are increasing (PrPMC CPU, chipset,…)
- ✦Limitation to improve DAQ performance
  - Bottlenecks of COPPER
    - CPU usage
    - Data transfer speed (1 Gbps)
  - Bottleneck of network output of ROPC (1 Gbps)
- ✦Future possibility
  - Luminosity & background situation changed
  - For a trigger-less DAQ

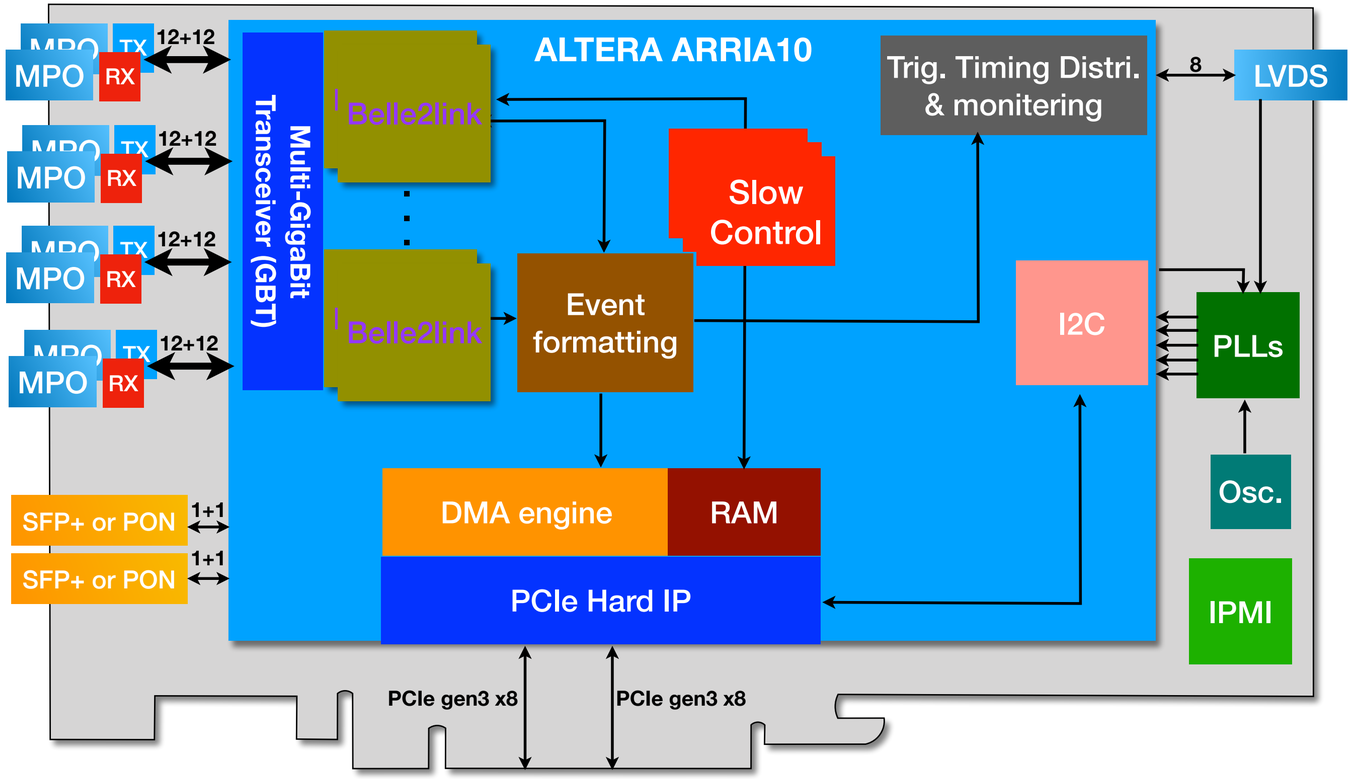
PCIe40 based readout now being used for 3 Belle II detectors

PCIe40 based new readout system for Belle II



- A upgrade of current COPPER based readout system with PCIe40 board
- Upgrade of readout system will keep the modification as less as possible, for the system connected.
- No major modification required for hardware and firmware of the sub-detectors' systems.
- Software for slow control and data readout need some upgrades

Features of Belle II PCIe40 readout system

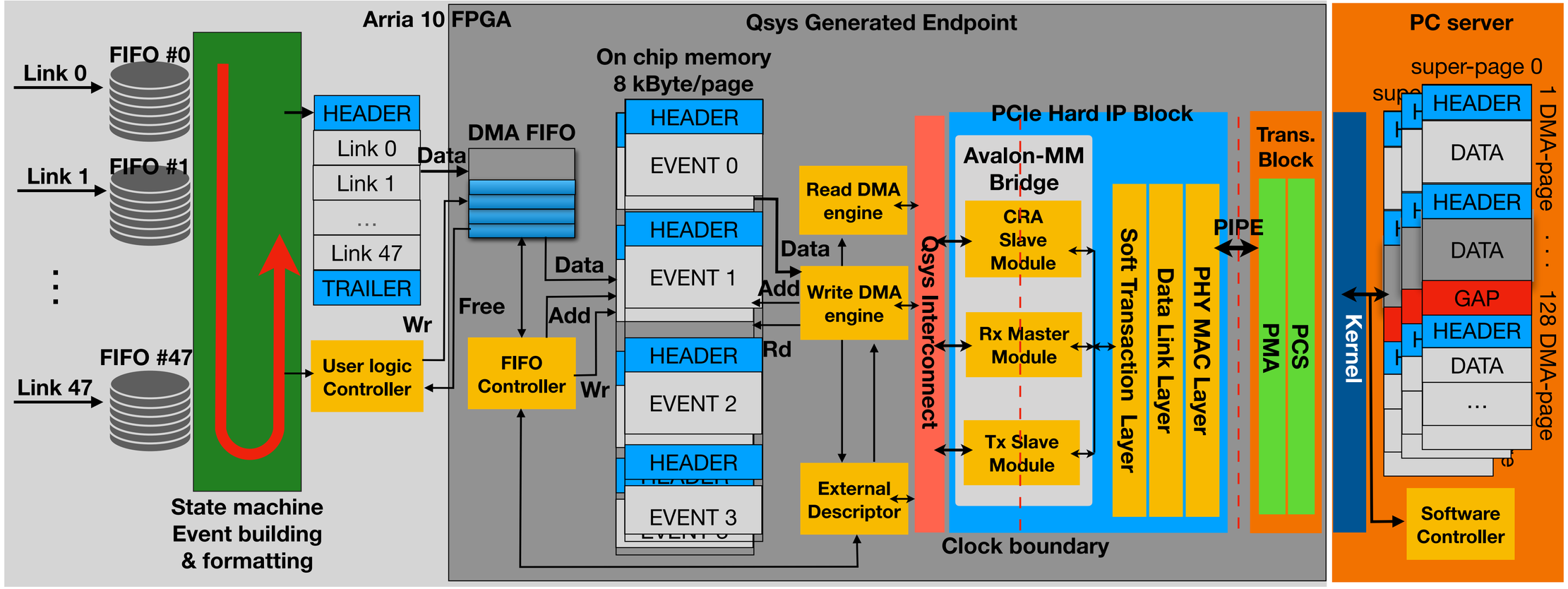


Board	FPGA family	Optical links	PC interface	Experiment
PCIe40	ALTERA Arria10	48	2 PCIe Gen3 x 8	LHCb, ALICE

21 PCIe40 boards to replace 203 COPPERs
A compact system can be achieved

- Belle2link protocol: kept as same functionality, but from Xilinx FPGA port to Intel Arria10 FPGA
- Event building and formatting: newly added based on the FPGA logic (on board CPU for COPPER)
- Slow control: protocol part moved to software
- b2tt link(connect to TTD): new design to handle 48 links
- PCIe based DMA: external DMA descriptor controller apart from DMA engine (based on Qsys).

Data processing



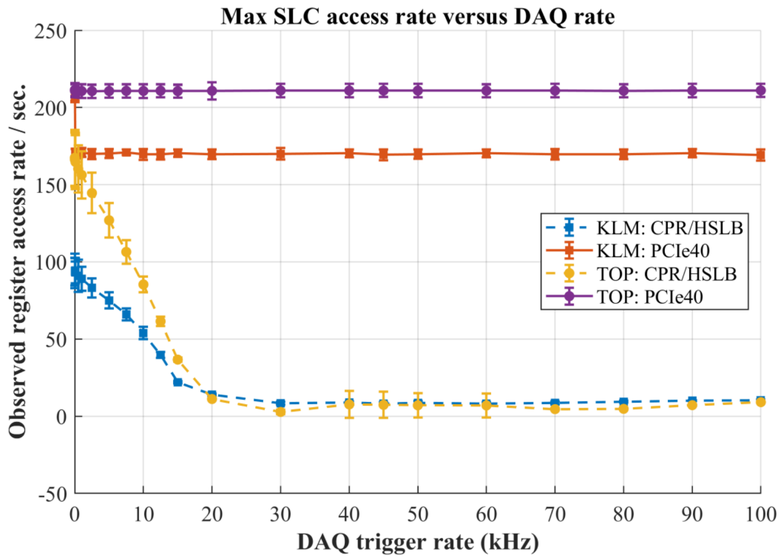
- Event-building
  - Reduction of header and trailer info of each link
  - Data check
    - CRC calculation, mismatch headers among different links
  - Add error-bit flag to the builded event
- Pulse trigger rate: 470 kHz (times 8 kBytes)
  - Data transmission rate: 31 Gbits/s <—>
  - 10% of event detect back-pressure.
- Pulse trigger rate: 260 kHz, 21 Gbits/s, no event lost.

Theoretical maximum data rate is 50 Gb/s
can eventually be increased to 100 Gb/s

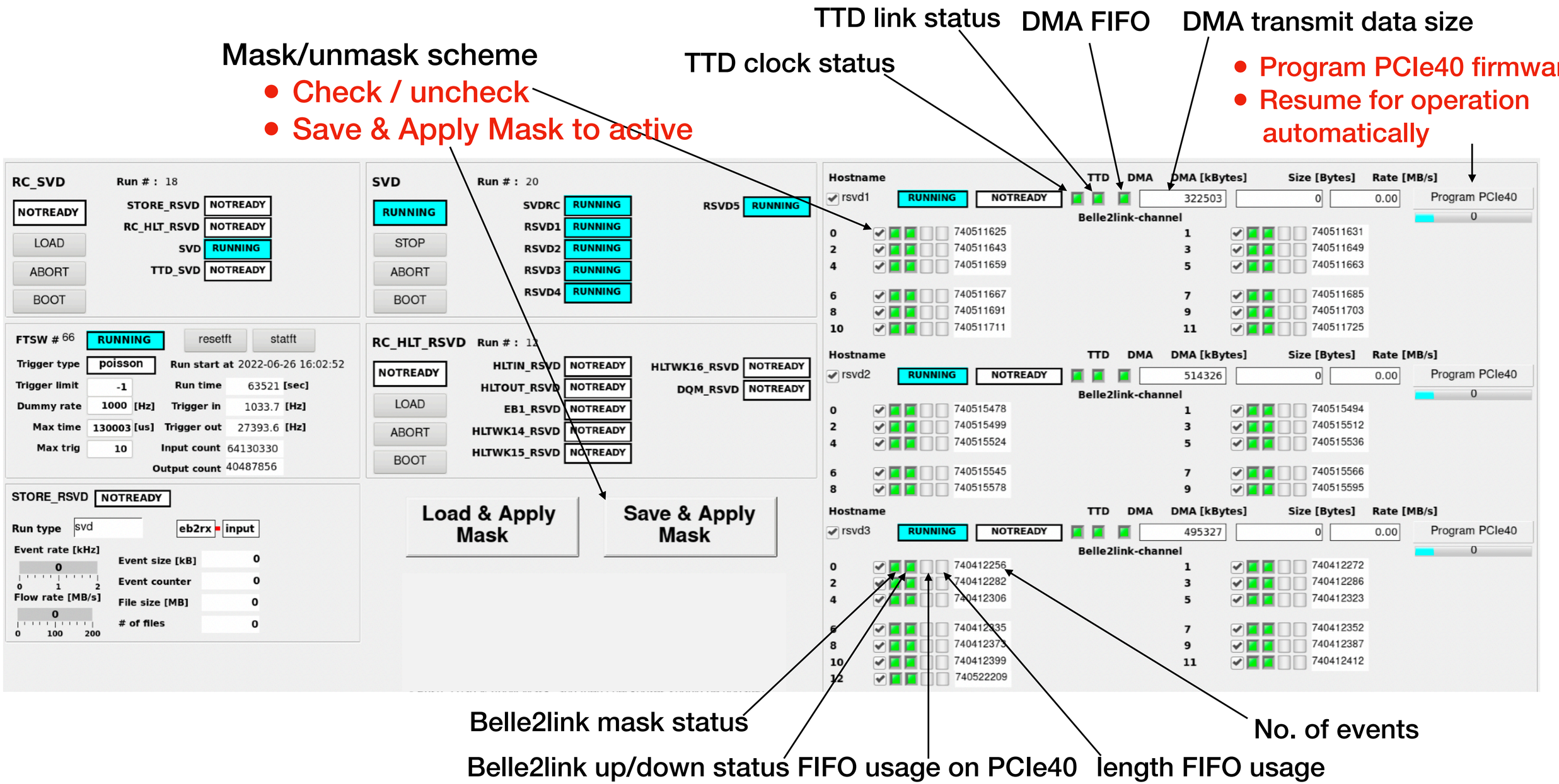
Performance of slow control system

- Belle2link was kept the same as COPPER-HSLB system
- 3 slow control access methods for PCIe40 were implemented and tested
  - A7D8 and A16D32 kept the same features as HSLB
  - Streaming file method separated based on packet size;
    KLM (6 words / pocket), ARICH (100 words / pocket)
- A16D32 access:
  - 83 us / access <—>1 ms / access for HSLB
- Streaming file:
  - 360 KBps (KLM) <—> 350 KBps for HSLB
  - 1-2 sec downloading ARICH firmware <—> 1-2 sec for HSLB
- Parallel access of slow control + data acquisition with multiple links is working well
  - It takes the same time for the access w/ and w/o parallel access
- Slow control configuration for FEEs of KLM, TOP, ARICH has been tested and working fine.

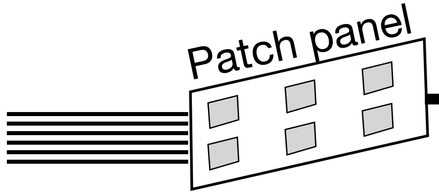
Detector	A7D8	A16D32	byte stream
SVD	○		
CDC		○	
TOP		○	
ARICH		○	○ (~3MB)
ECL	○	○	
KLM		○	○

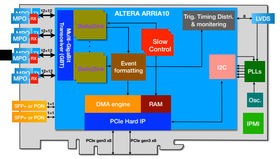


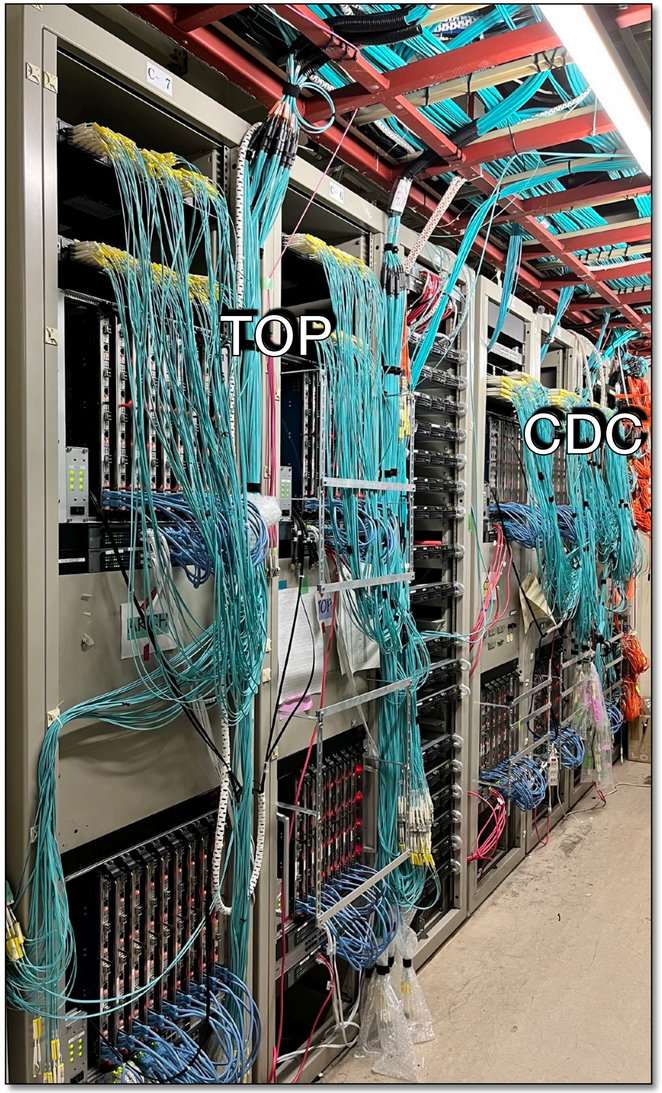
Operation panel for sub-detector



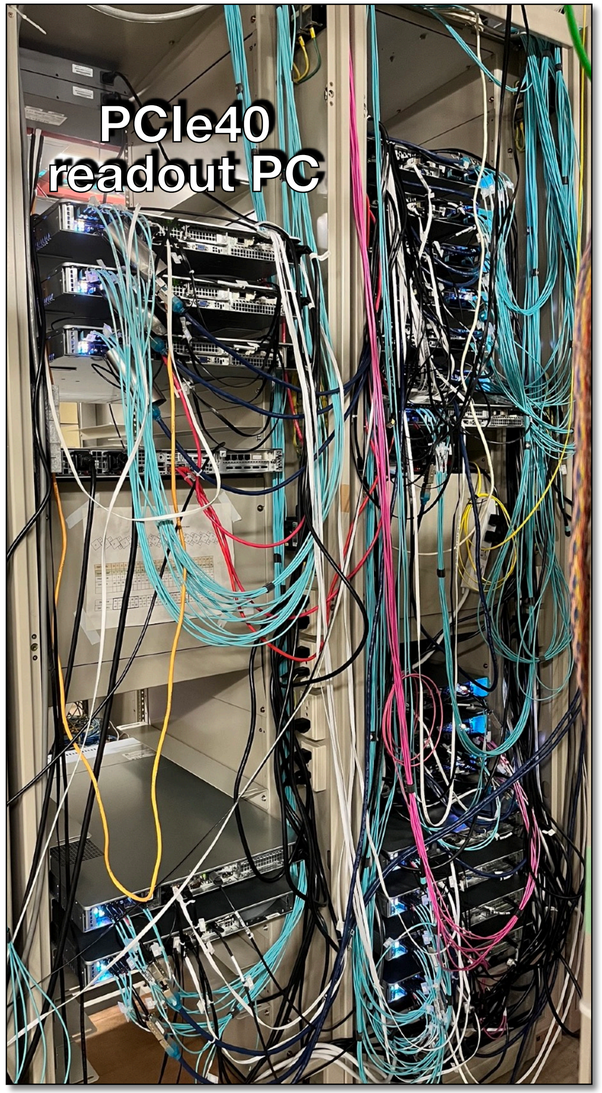
Installation of new readout system



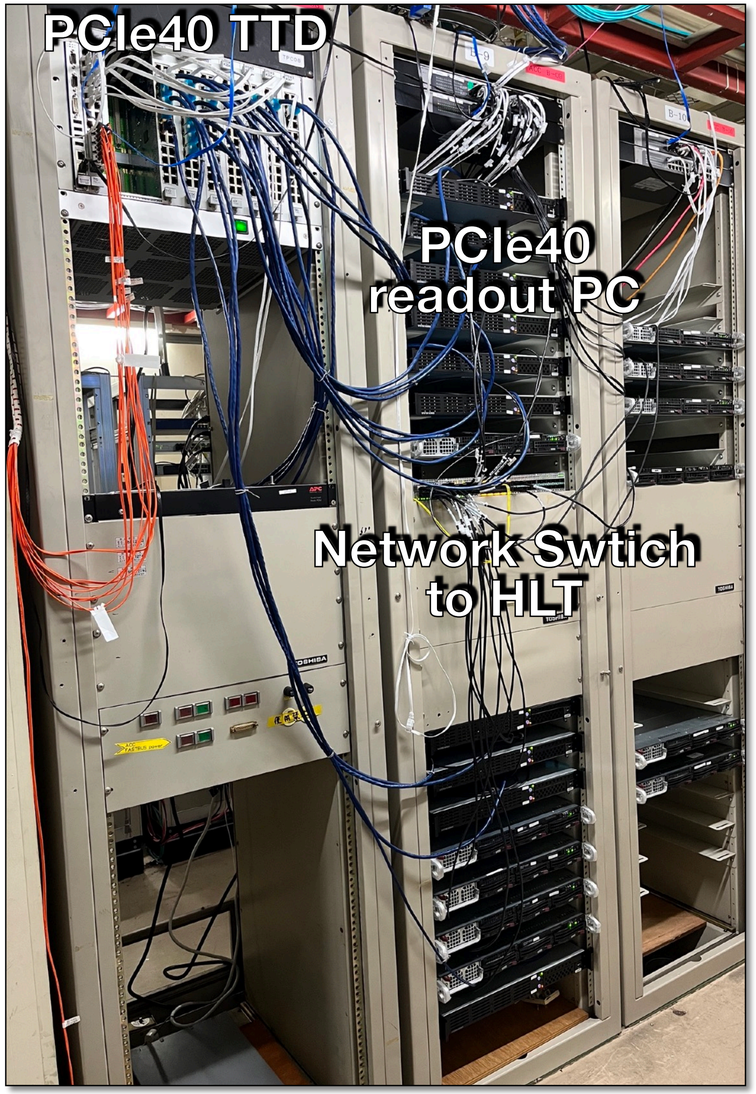




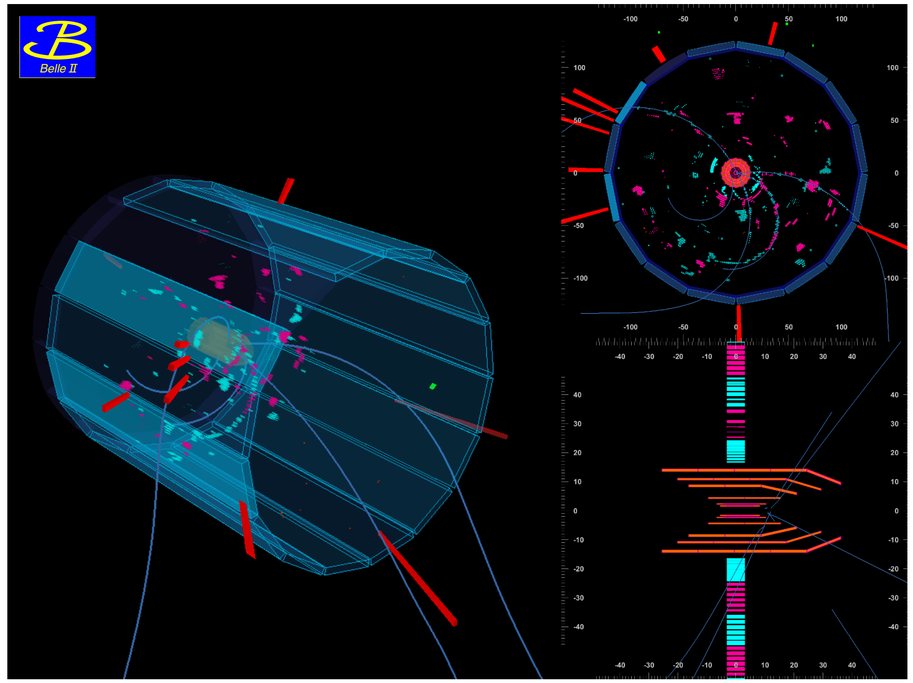
Back view

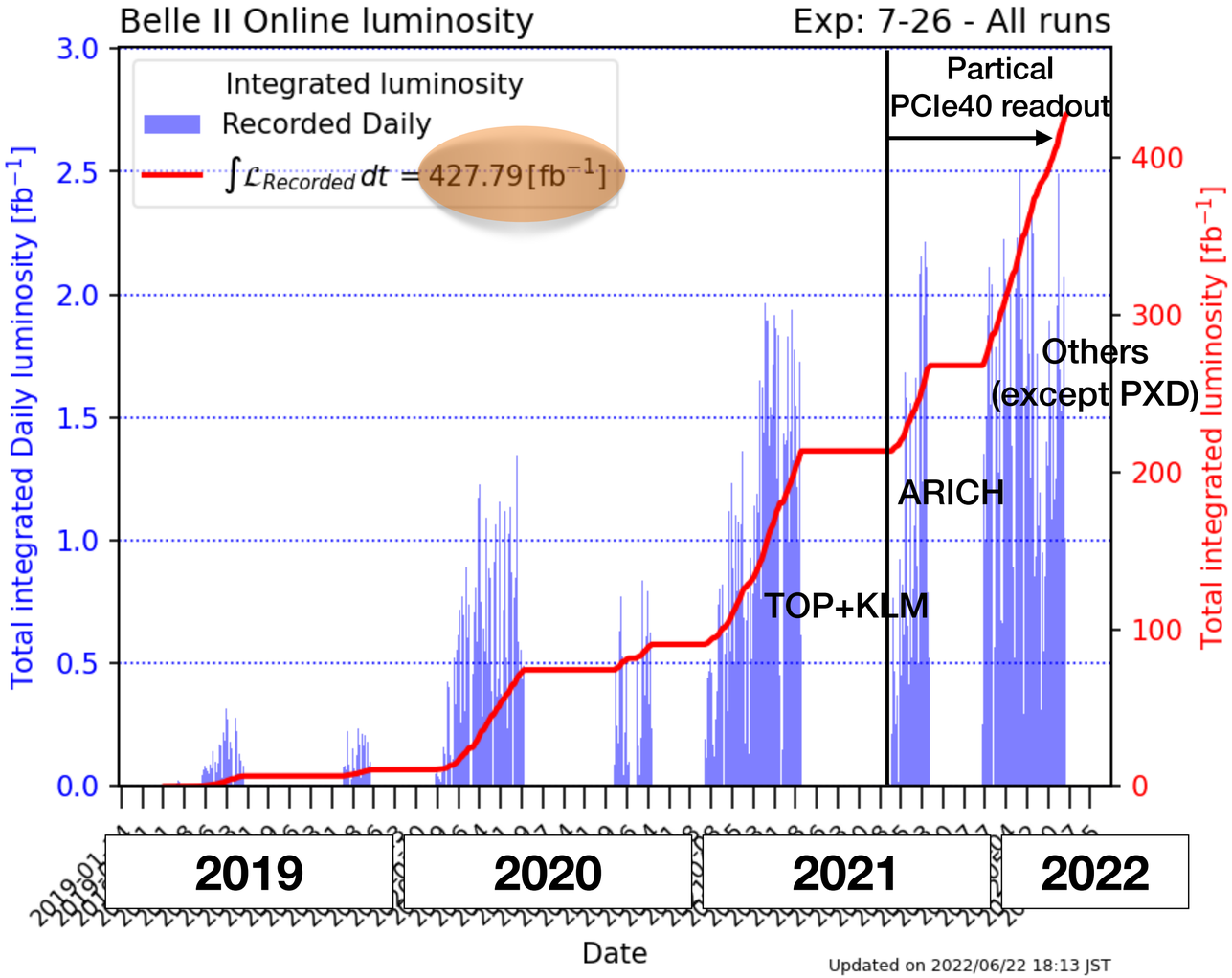


Front view



Operation status and integrated luminosity





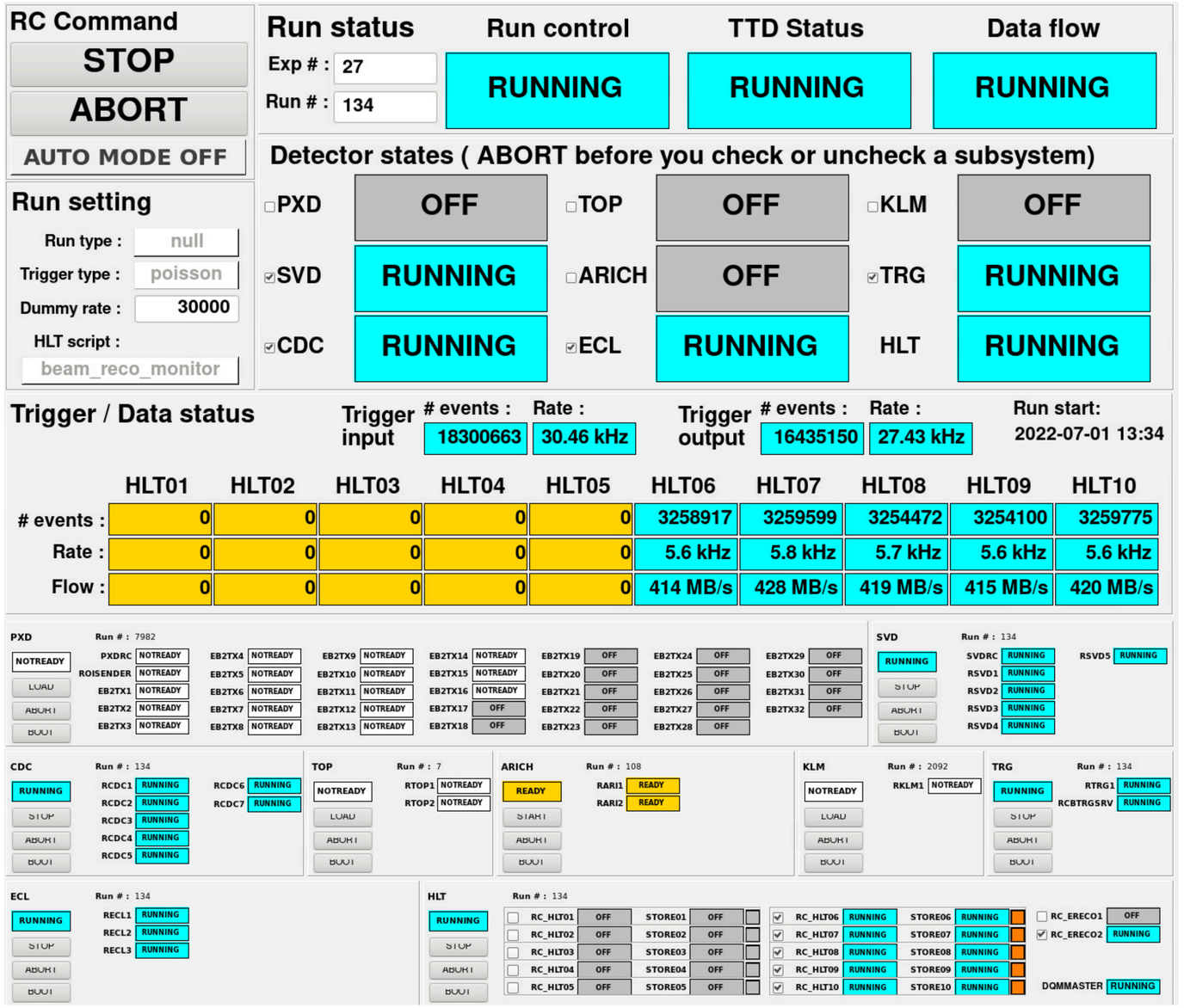
- Partial replacement of the Belle II readout system started in the 2021 summer shutdown period
  - 2021c run: TOP+KLM
  - 2022ab run: ARICH
- DAQ upgrade succeed

Belle II data taking efficiency ~90%

- ~427 fb^{-1} till now (Belle: 1 ab^{-1})
- Long shutdown 1 (LS1: 2022-2023): other sub-detectors (SVD, CDC, ECL and TRG) will be replaced

Commissioning with remaining sub-detector

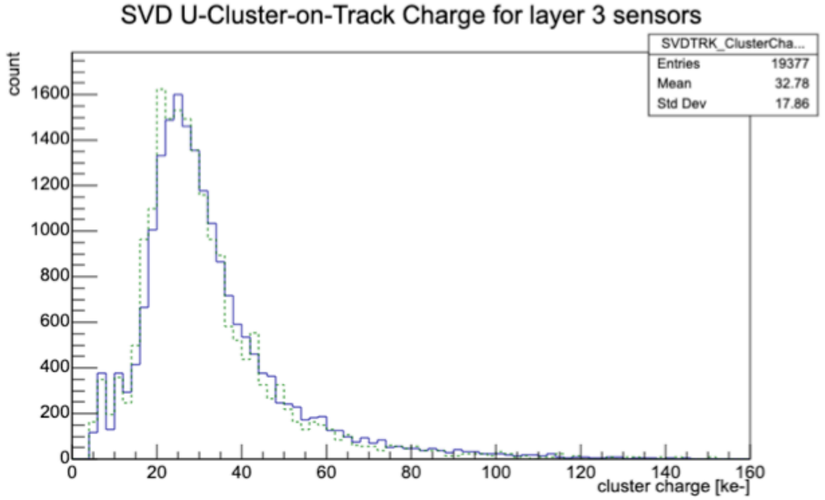
- Developments of replacement for SVD, CDC, ECL, TRG have been done
  - Data flow
  - Slow control / monitoring
  - TTD system
  - Data unpack software
- Data flow from frontend to storage
  - Local run and global run
- Slow control functionality tested
  - “Program PCIe40”, masking, etc.
- Stress test with global run
  - 30 kHz, poisson trigger.
  - All sub-detectors connect to PCIe40



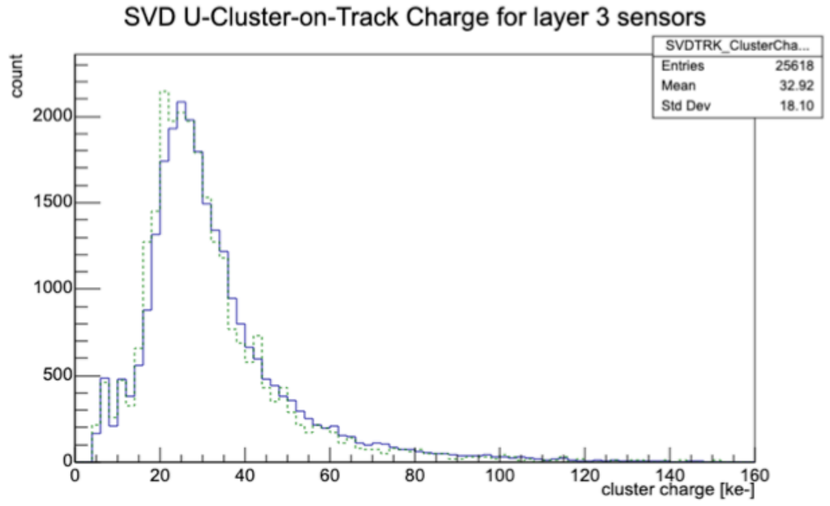
Cosmic ray test for data quality check

- Cosmic ray test to check data quality
  - SVD, CDC, ECL, TRG
  - Data unpack software check
  - Checks of individual channel
  - Compare data quality plots between COPPER and PCIe40
- Data quality monitor (DQM) used for check
  - All four detector show similar data quality between COPPER and PCIe40 readout

PCIe40 readout

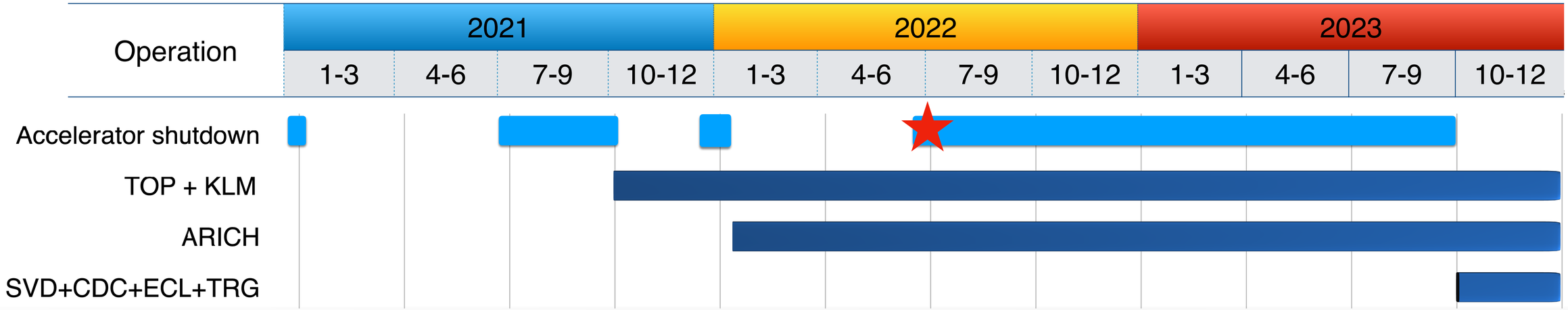


COPPER readout



Future plan and improvement

Full replacement schedule from COPPER to PCIe40



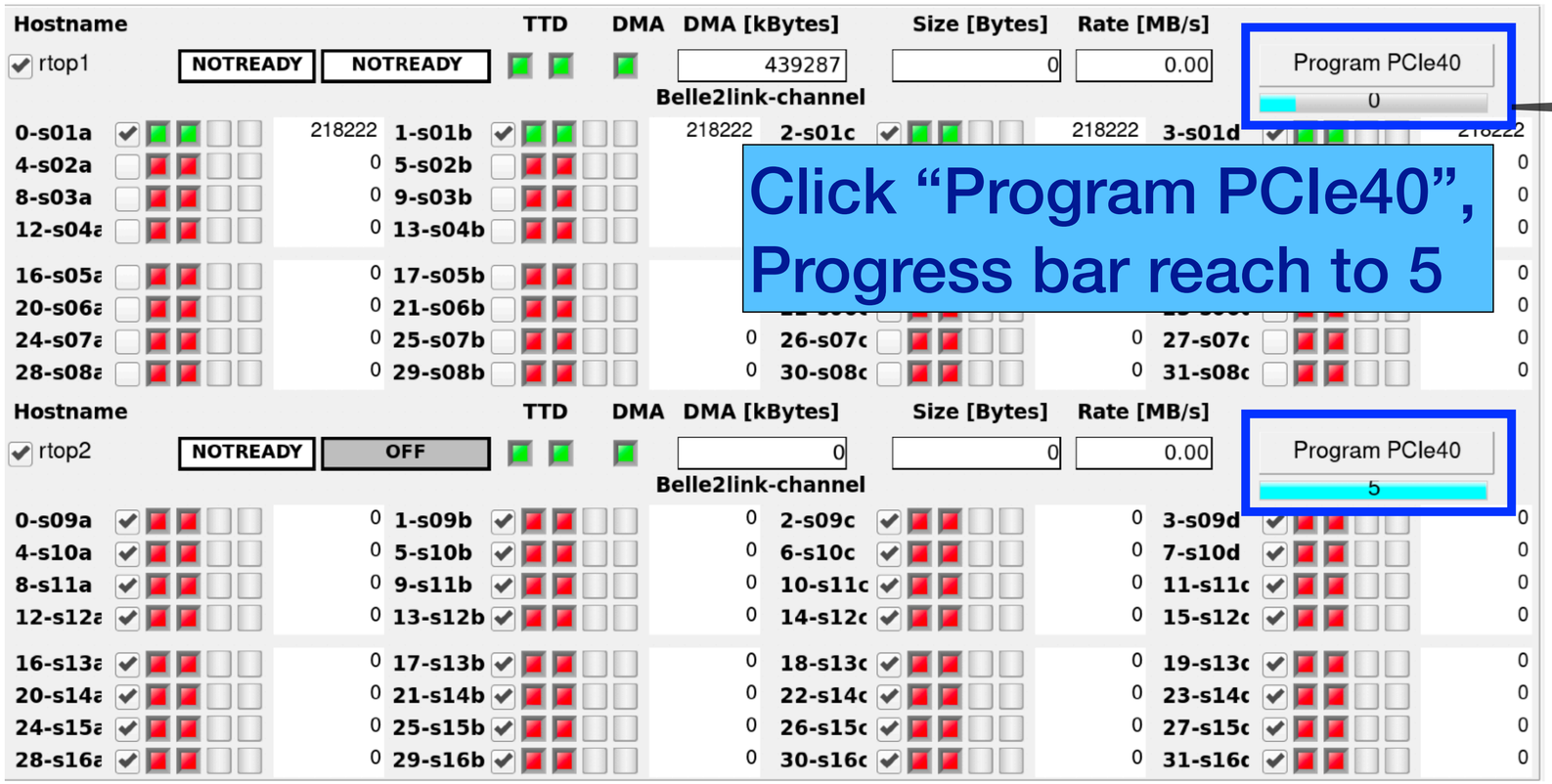
- b2tt link (TTD-PCIe40) lost happened during last run
  - External noise is one of the causes
  - 10 m CAT-7 cables (FTSW-FTSW) were replaced by optical fibers
  - Expert is now working on replacement of CAT-7 cable of FTSW-PCIe40 by fiber
- Bottleneck of PCIe40 readout is data processing (checksum calculation) 630 MB/s per ROPC
  - Can be move to firmware (currently, this check is done by both firmware and software)
  - Next will be 10 Gb Ethernet 870 MB/s per ROPC
- Longer term developments
  - Double DMA interface -> double data throughput
  - Event building in software -> reduce possible dead time when luminosity increased

Summary

- PCIe40-based readout has been developed for the upgrade of Belle II DAQ system
- Basic features (data processing, slow control) of the new readout system worked fine
  - Maximum 31 Gbps readout (just 1 out 2 PCIe40x8 interfaces used)
  - Slow control access for multiple channels in parallel
- TOP, KLM, ARICH PCIe40 readout during physics run
- Data-taking was running stably with new readout system
- Belle II data-taking efficiency close to 90%
- SVD, CDC, ECL, TRG with PCIe40 readout are ready, full PCIe40 readout from next run
- Development of double DMA interface and software event building is ongoing

Backup

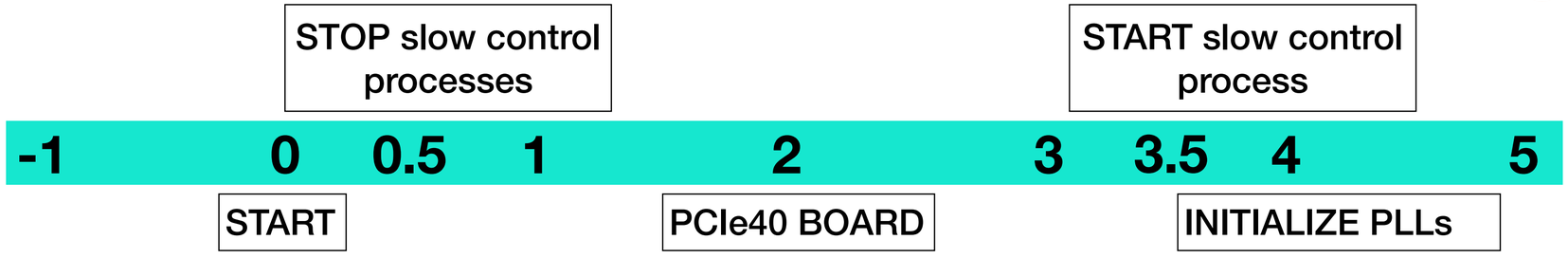
Simplified procedure of programing PCIe40

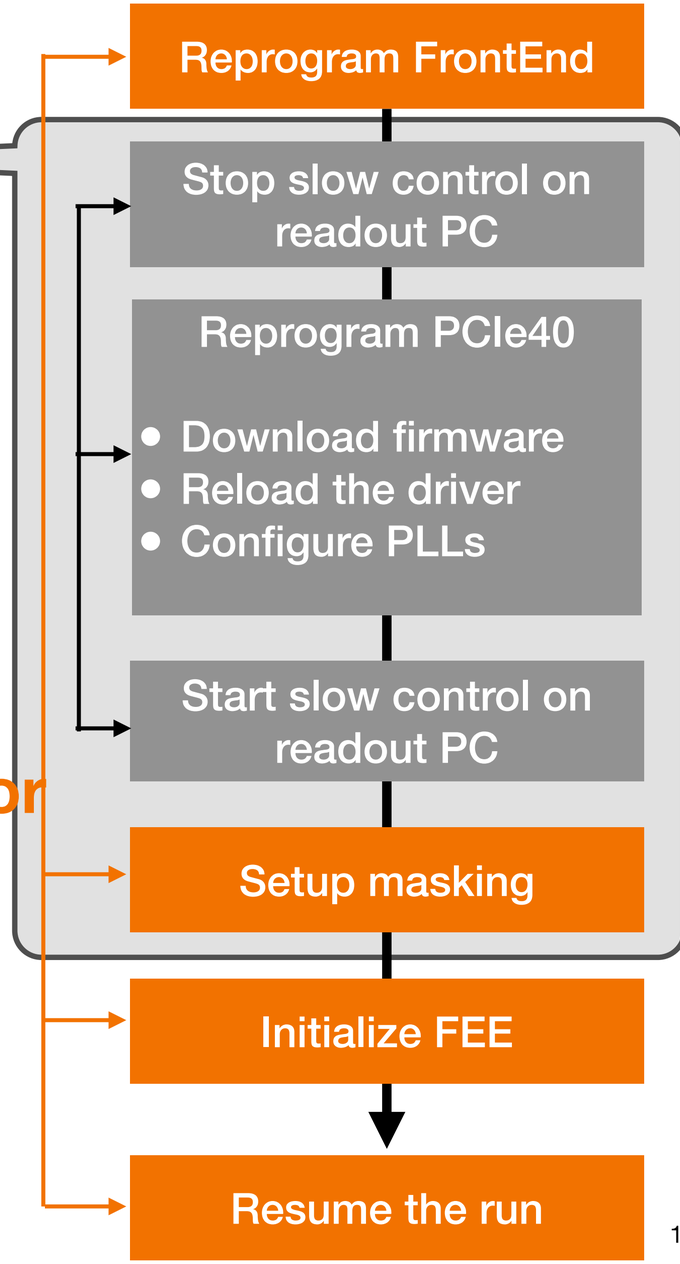


Click “Program PCIe40”, Progress bar reach to 5

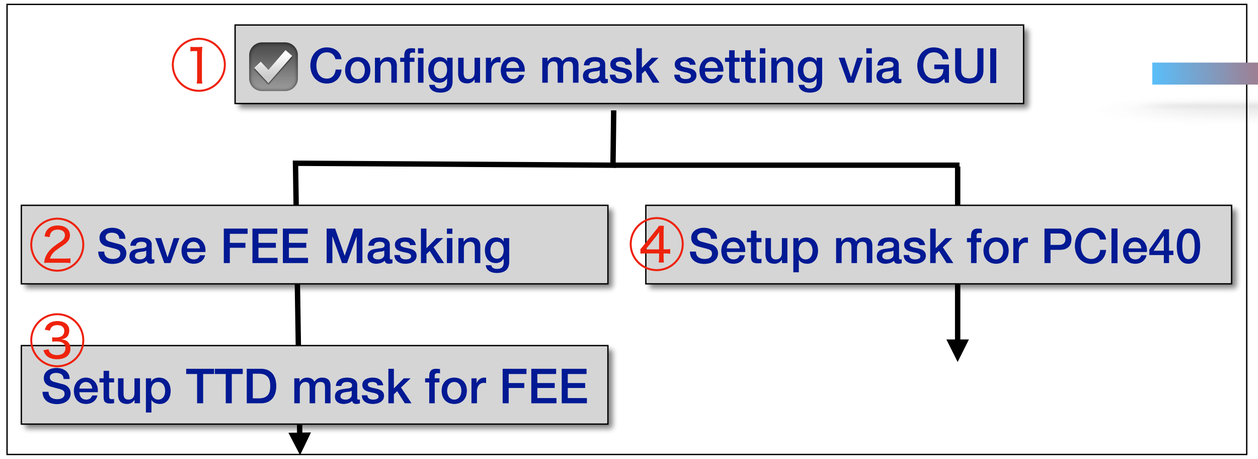
DAQ shifter

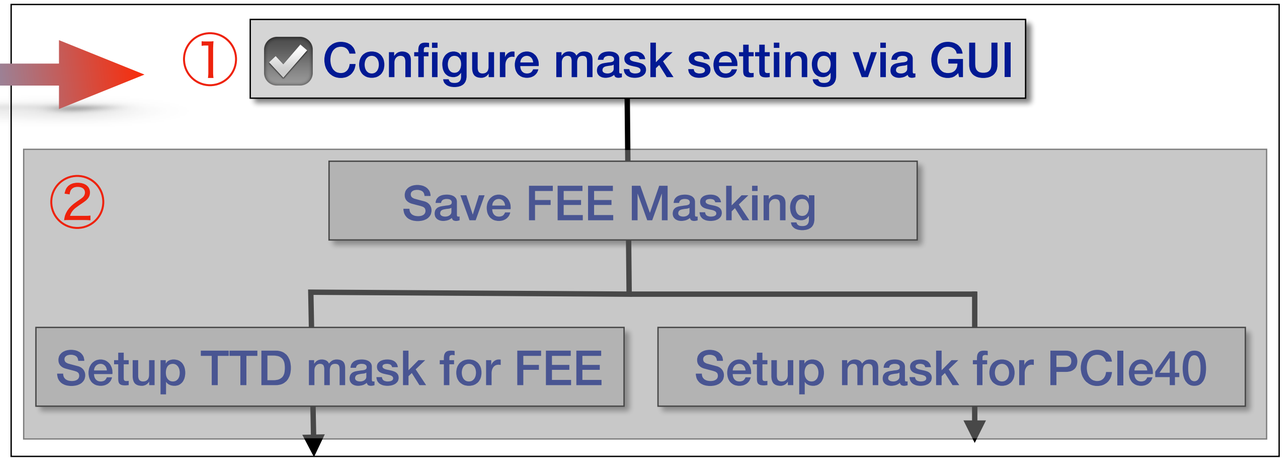
Detector shifter



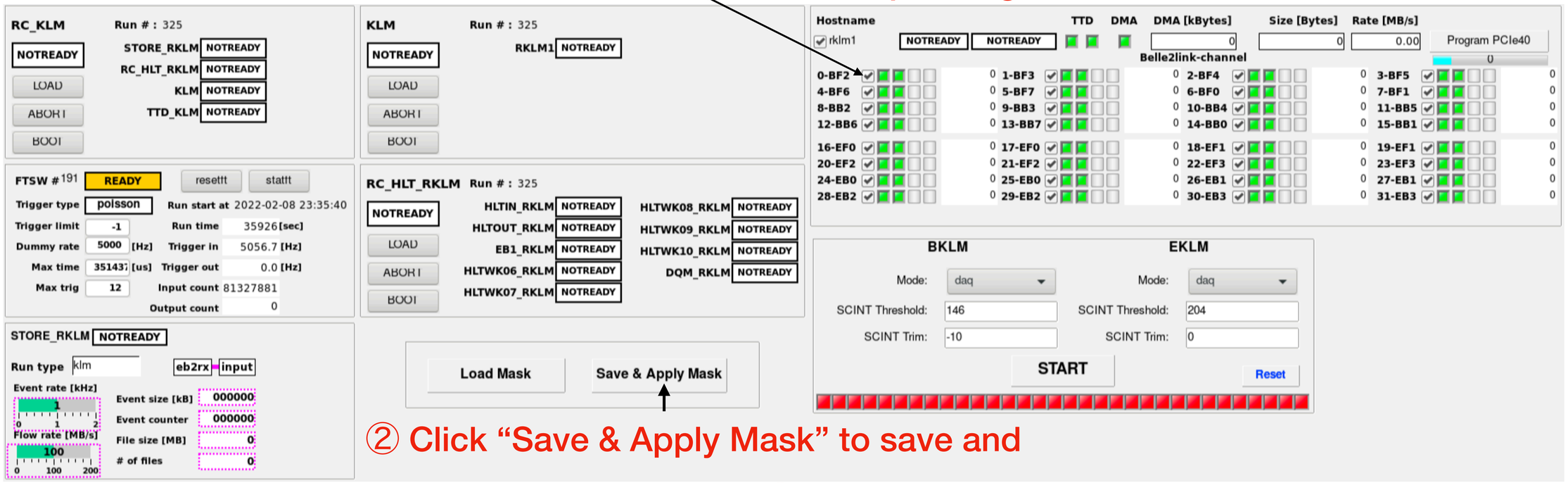


Improvement of masking scheme





① Check/uncheck to mask/unmask corresponding channel



② Click “Save & Apply Mask” to save and apply the mask on both PCIe40 and TTD

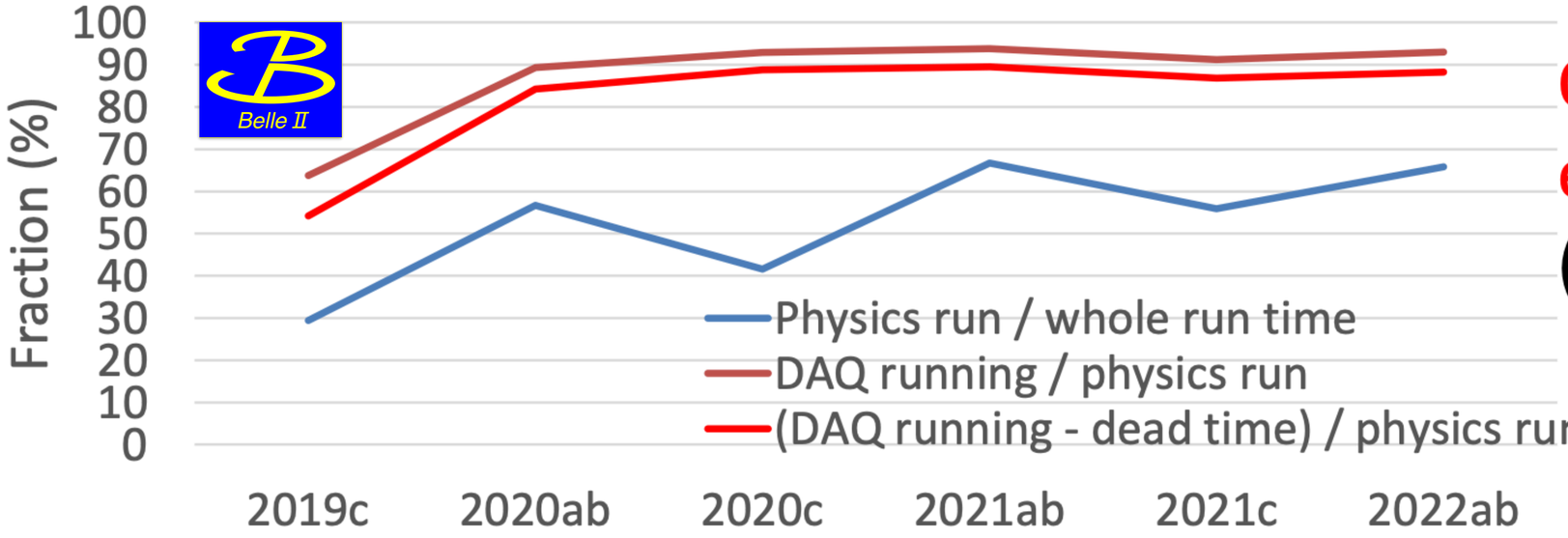
PCIe40 related DAQ troubles (>30 mins)

Sub-detector	Error	Recovery
TOP	Frontend configuration failure	Reprogram PCIe40 firmware
	Corrupted data (event No. jump)	Masked specific frontend (board ID info missing in the error message)
KLM	Belle2link lost from a frontend	Reprogram KLM frontend and PCIe40 firmware
	Belle2link lost from a frontend	Reprogram KLM frontend and PCIe40 firmware
	Belle2link lost from a frontend	Reprogram KLM frontend and PCIe40 firmware
	Frequent b2tt link lost b/w PCIe40 and TTD	Reprogram PCIe40 firmware

- Recovery from a DAQ trouble sometimes takes > 30 mins
  - Programming PCIe40 firmware
  - Masking a problematic frontend and PCIe40 channel
- Improvement during last winter shutdown of accelerator
  - User-friendly tools
  - Redesigned schemes
  - Informative error messages
  - b2tt link via optical fiber, instead of long CAT-7 cable

DAQ operation status

TOP, KLM, (ARICH) upgrade to PCIe40 readout from 2021c (2022ab) run

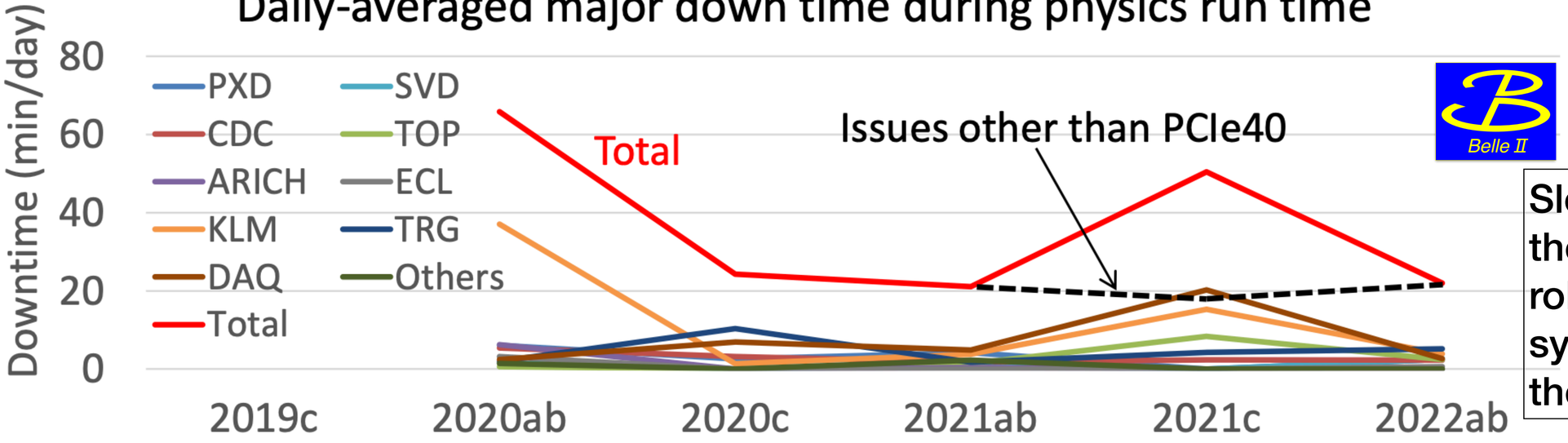


Overall data taking efficiency = 88.2%

(Target 90%)

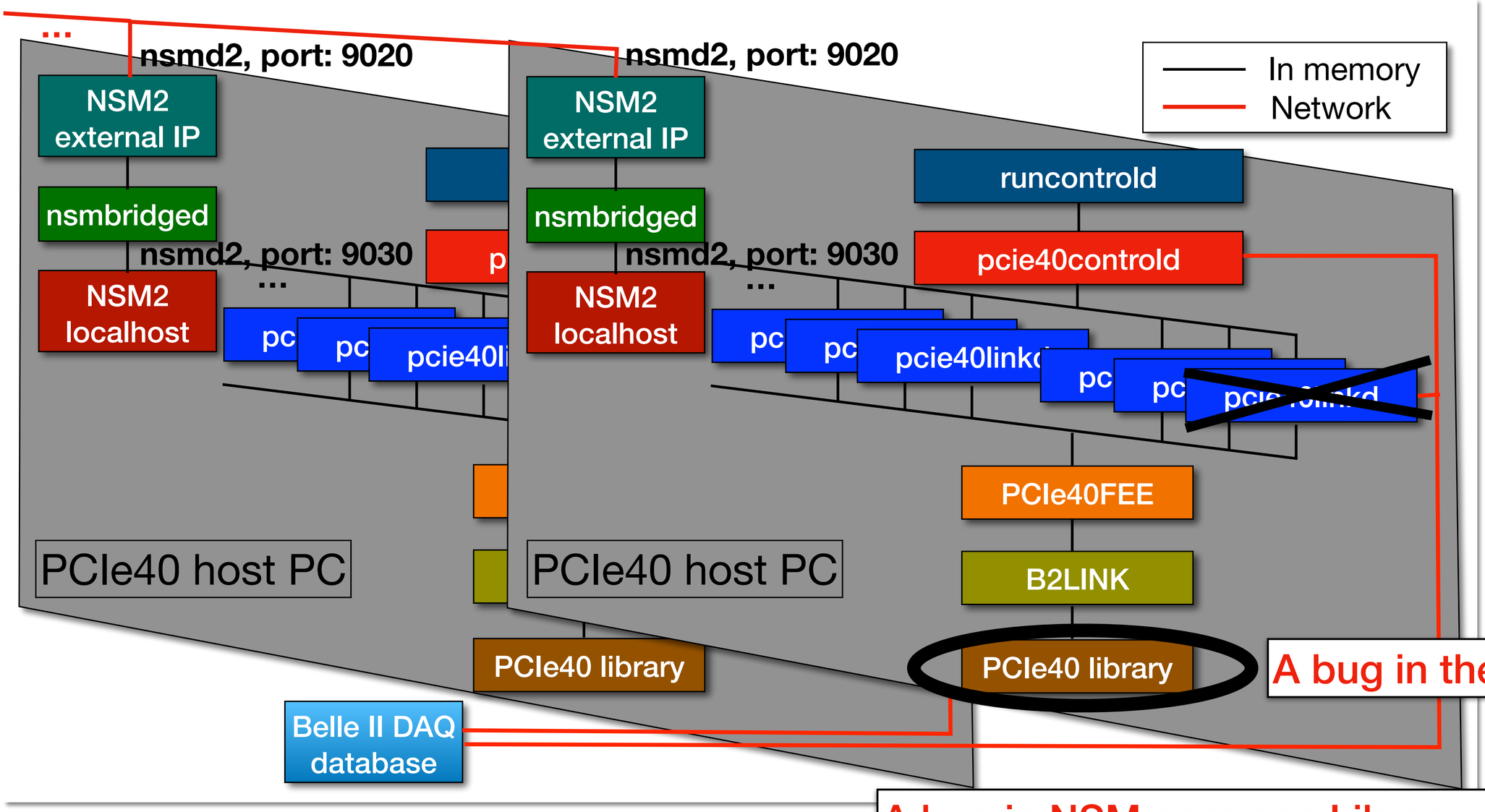
Getting worse with the beam background.

Daily-averaged major down time during physics run time



Slow control issue in the common library, roll back to COPPER system, resumed after the issue been fixed

TOP FATAL issue on Nov. 2-3



A bug in the PCIe40 library

A bug in NSM common Library used for BELLE II cased buffer overwritten