Cold Demonstrator Readout

Nicolò Tosi – INFN Bologna – 11/11/2021 – DUNE Italia Meeting

The SiPMat Camera

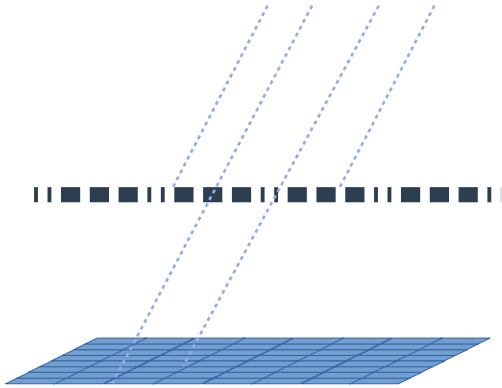
A SiPM based imaging sensor

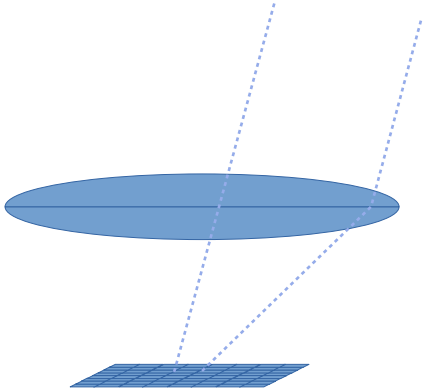
Suitable for both masks and lenses

16 x 16 SiPM Matrix, multiple options

Cryo readout ASICs by INFN Torino

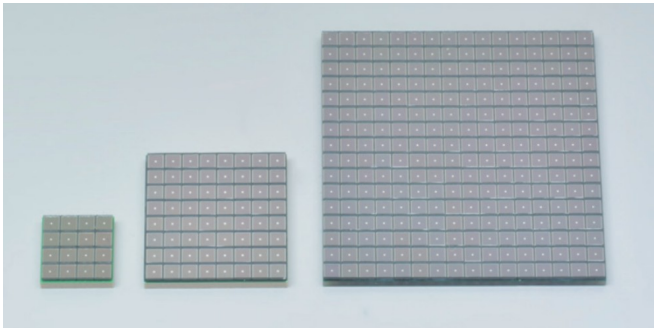
Warm FPGA backend

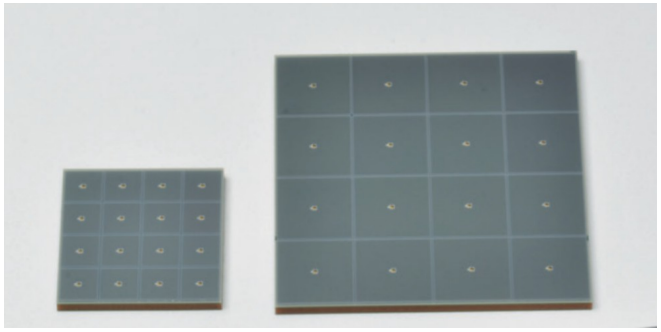




Preferred to a “conservative” warm electronics ~ 1 year ago, because that, while easier, would not have proved anything for GRAIN.

Multiple options for SiPM matrices (Hamamatsu)





One 16x16 S13615-1050N-16

Cell pitch 50 um, pixel area 1 mm^2

Active area 256 mm^2, total area 368 mm^2

Four 8x8 S14161-3050HS-08

Cell pitch 50 um, pixel area 9 mm^2

Active area 2304 mm^2, total area 2641 mm^2

Other options exist in Hamamatsu catalogue, with pixel area up to 36 mm^2

A cold readout for the cold demonstrator

The ALCOR ASIC by INFN Torino

Can operate in cryogenic conditions

32 Channels, each with multiple TDCs

< 100 ps TDC resolution, amplitude from time over threshold

Quite a few limitations, first chip of its kind:

- Yet to be demonstrated in the full system
- High power consumption per channel (several mW)
- Insufficient density, limited number of physical channels per output lane

A stack of boards

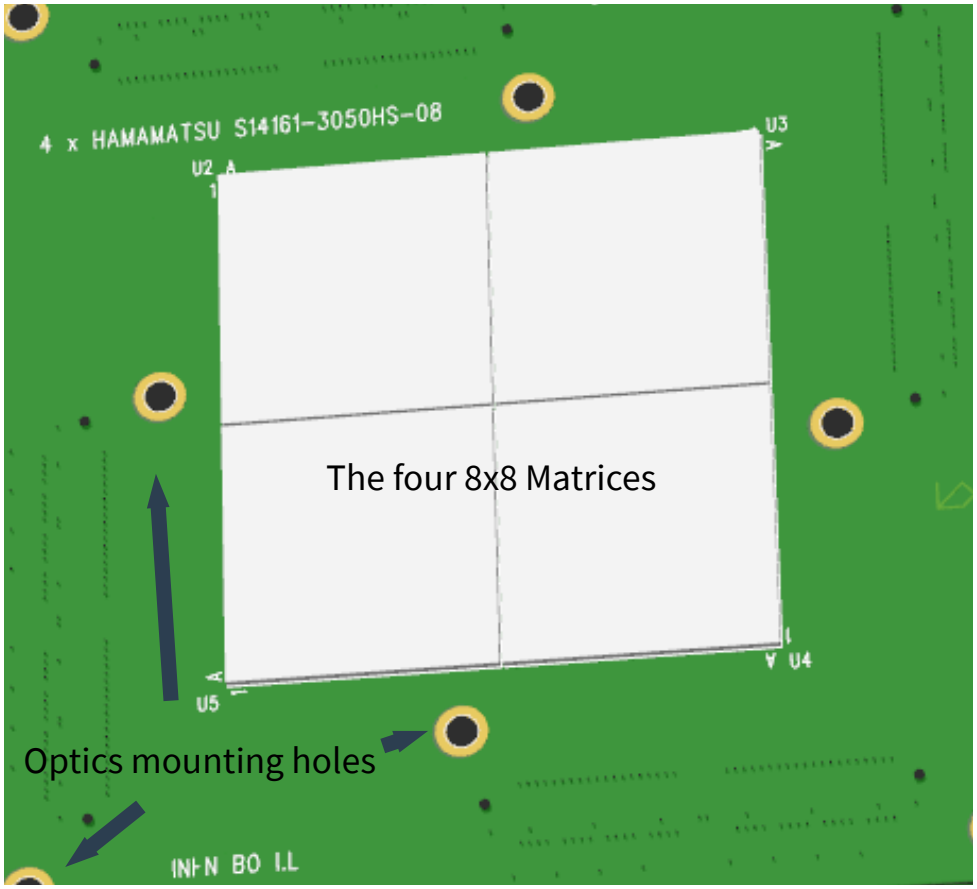
To allow easy swapping of matrices, they are on a separate board

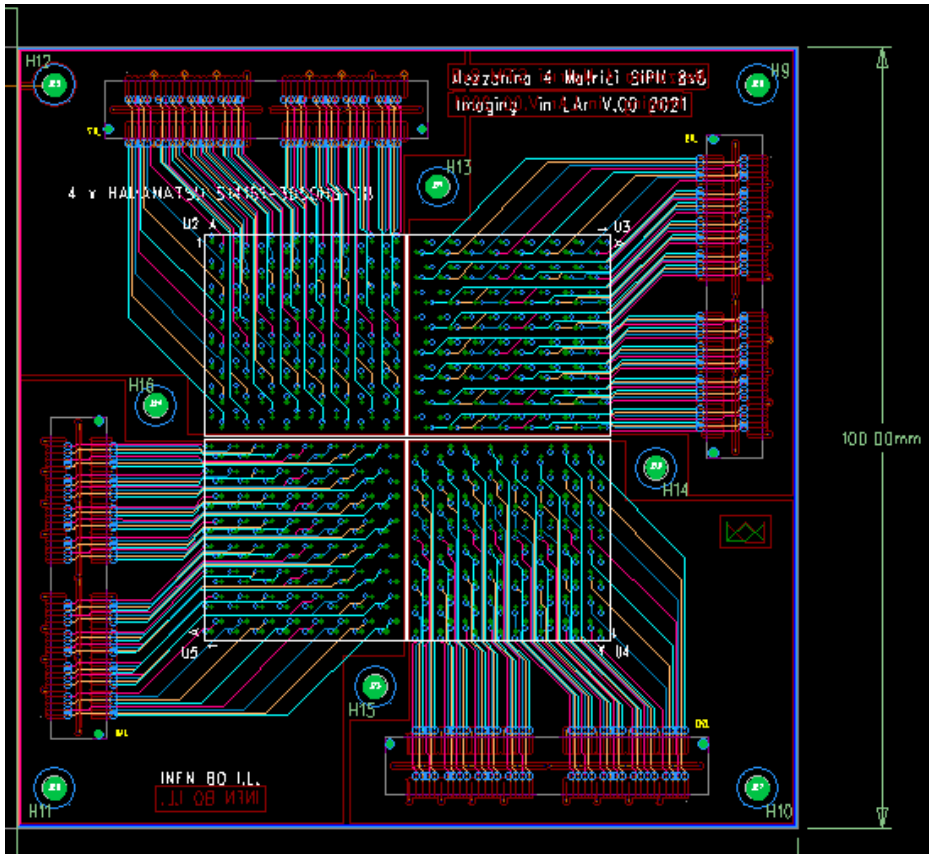
SiPM board (s)

ALCOR board (8 ASICs)

A mechanical mock up of this has been tested in LN

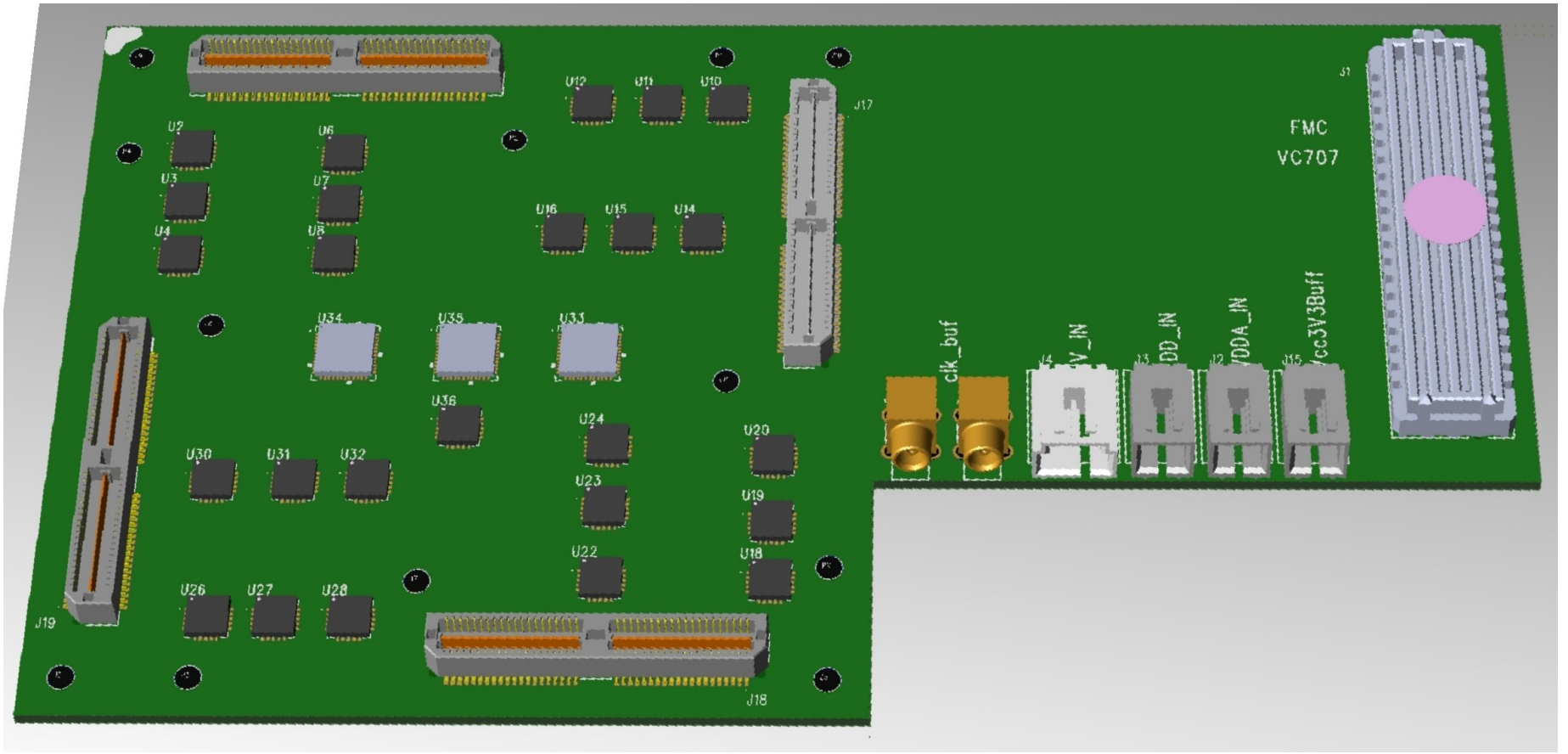
SiPM board (top)



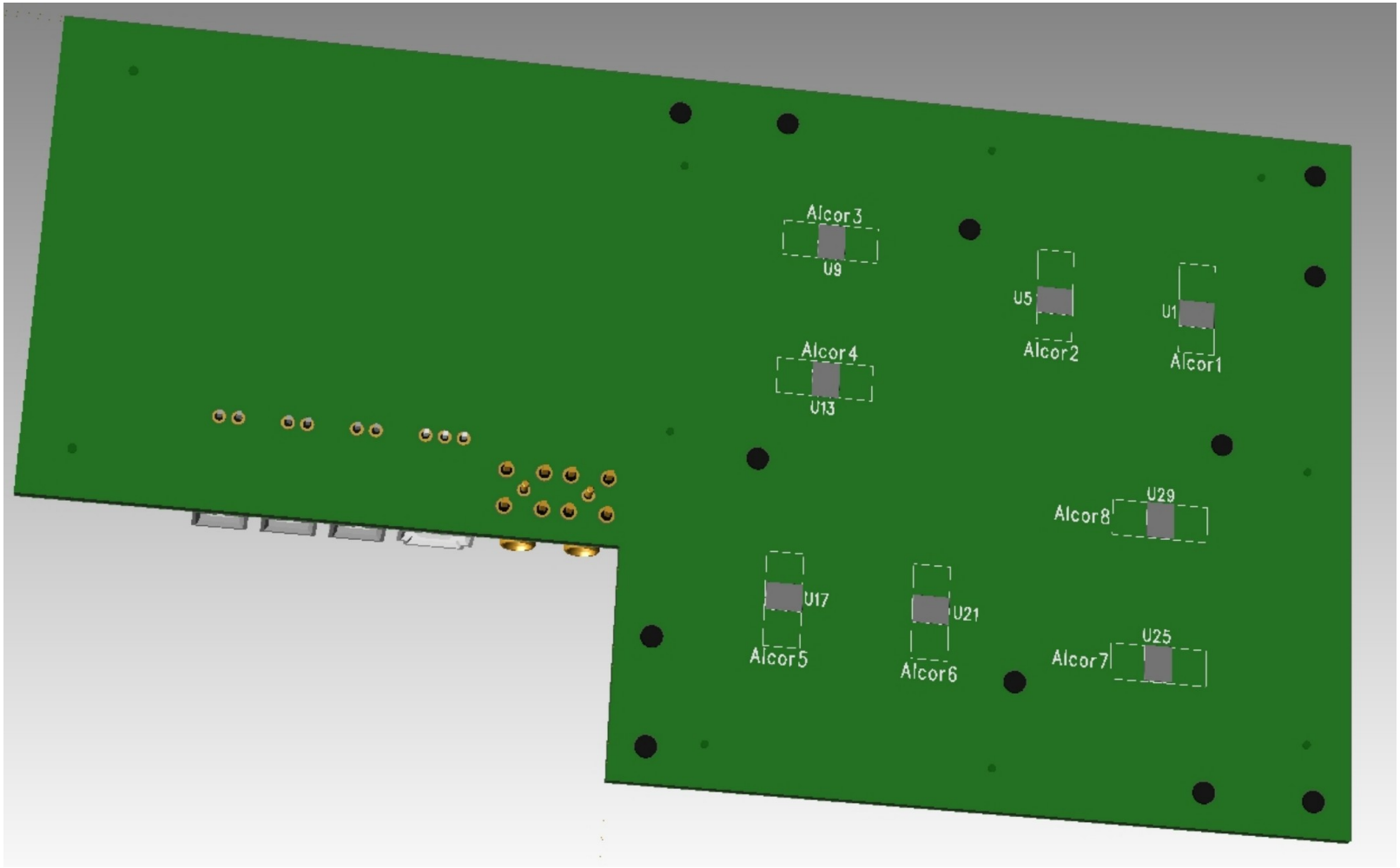


Connected to ALCOR board with high density Samtec Q series strips

ALCOR board (top)



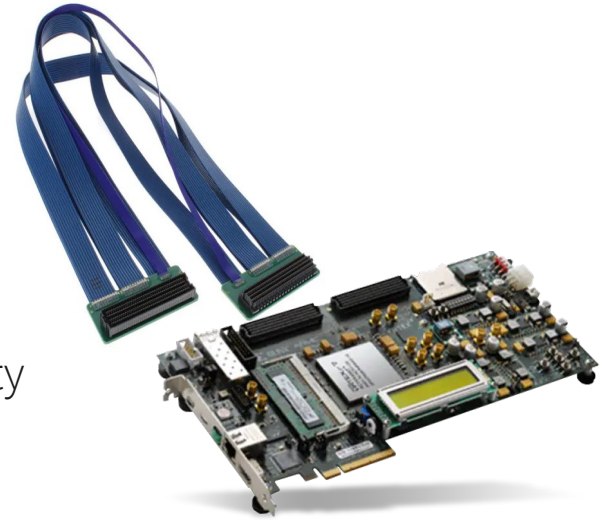
ALCOR board (bottom)



Back End FPGA

Commercial, choice dictated by ALCOR connectivity

- Each ASIC requires 12 LVDS pairs, of which 6 @ 320 MHz / 640 Mbps DDR
- Could go slower, but cannot decouple TDC clock from I/O clock
  - Some slow pairs can be buffered
  - Some testing was needed to select LVDS buffer working in cryo conditions
- Still around 70 pairs => Requires full HPC FMC
- Very few boards have this fully routed
- Selected Xilinx VC 707, somewhat old but quite power
  - Use commercial Twinax FMC extension cable for better integrity



Back end Firmware

Features

- ALCOR data readout via LVDS links @ 640 Mbps
  - Modified from reference Torino code (was single chip only, used too many global buffers)
- ALCOR slow control via SPI
  - Standard SPI IP core
- Low jitter clock distribution, versatile configuration
  - Daisy chain/external oscillator/...
- Software interface with IPbus/Ethernet
- Trigger interface (input or output)

Current status

SiPM board

Matrices in hand, board design final, waiting for delivery

Ordered 3 assembled and 5 additional PCBs each for 1 mm and 3 mm pitch

ALCOR board

Schematic finalized, placement done, layout in progress. Waiting for ALCORs.

Back end

One VC707 in hand (borrowed), two on order.

FW 80% features implemented, waiting for hardware to test. SW to de bone.

Outlook (GRAIN scalability)

Primary concern for GRAIN: this ASIC does not scale

It’s the first of its kind, could not expect more!

The final ASIC needs

More channels per die AND more channels per I/O link

Lower power consumption per channel

Larger buffers to exploit beam duty cycle and relax peak link throughput

Decoupled TDC clock (as is or higher) from I/O clock (prefer lower)

Charge Integrator ADC in addition or instead of ToT (wishful thinking)