The ALCOR ASIC for EIC applications

Terza Giornata Nazionale EIC_NET
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Istituto Nazionale di Fisica Nucleare

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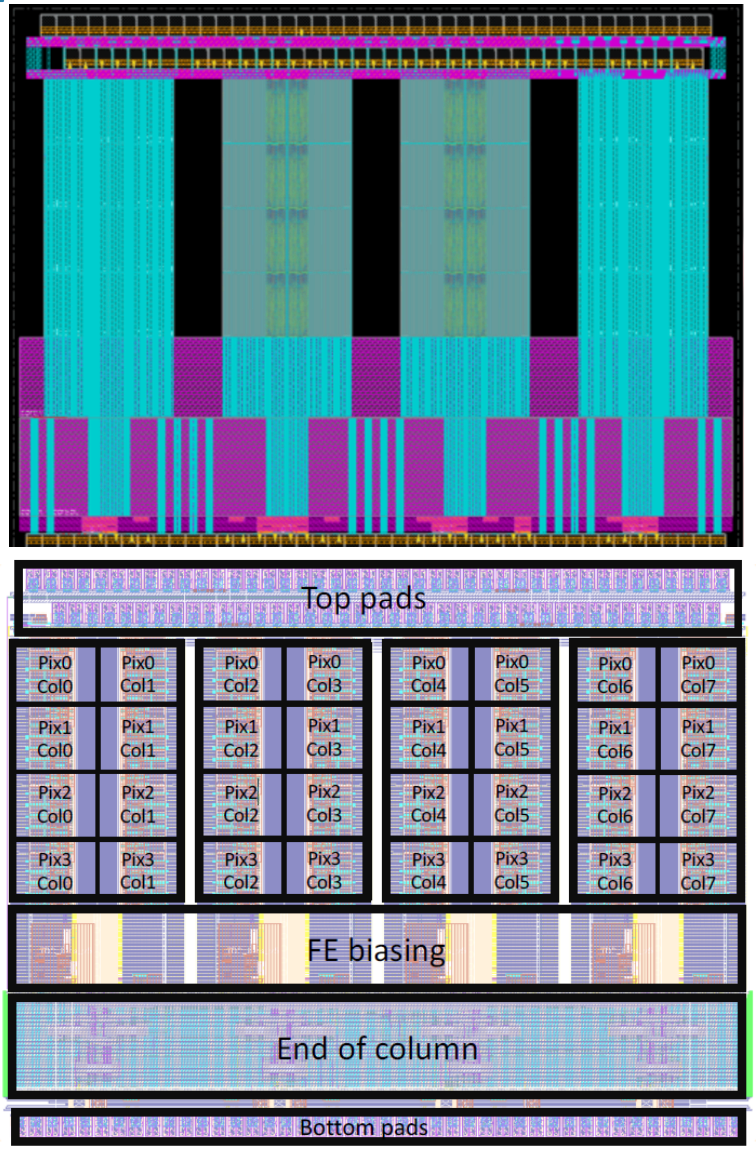
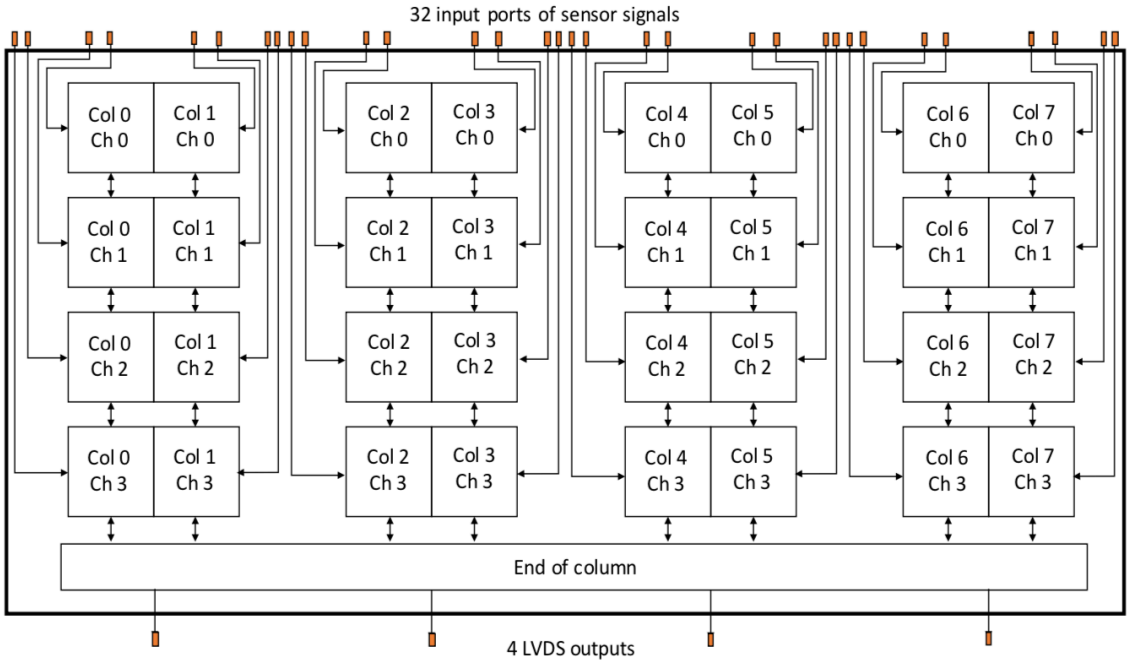
on behalf of the ALCOR Design and Test Team

ALCOR ASIC for fast-timing with SiPMs



- towards a 3D a-SiPM "digital tile"
- Developed by INFN (CSN2) for the readout of SiPMs at 77K, in the framework of Darkside
- 32-pixel matrix mixed signal ASIC
- the chip performs amplification, signal conditioning and event digitisation, and features fully digital I/O
- Single-photon time tagging mode or time and charge measurement
- 4 LVDS TX data links, SPI configuration
- operation up to 320 MHz (TDC binning down to 50 ps)

Chip Architecture and data payload



- 32-pixel matrix (4×8 array) mixed-signal ASIC
- SPI-based chip configuration

Event word

Column ID	Channel ID	TDC ID	Coarse counter	Fine counter
3 bits	3 bits	2 bits	15 bits	9 bits

31 0

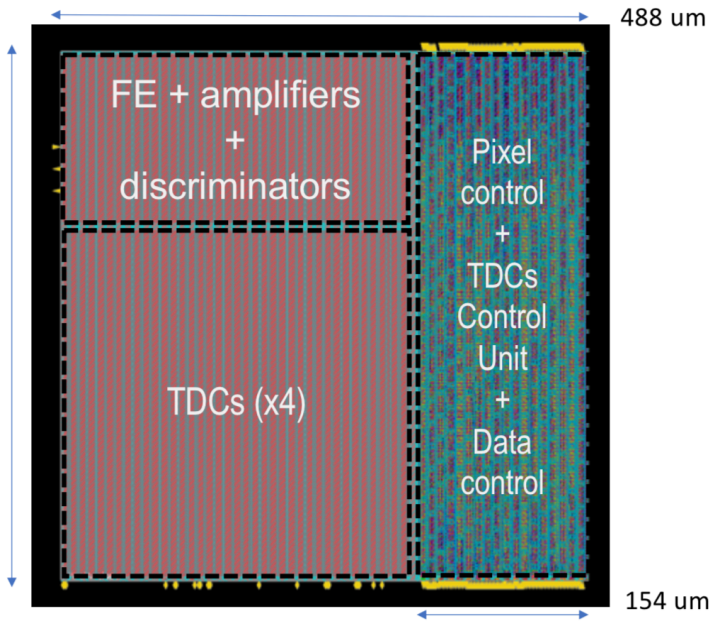
Status word

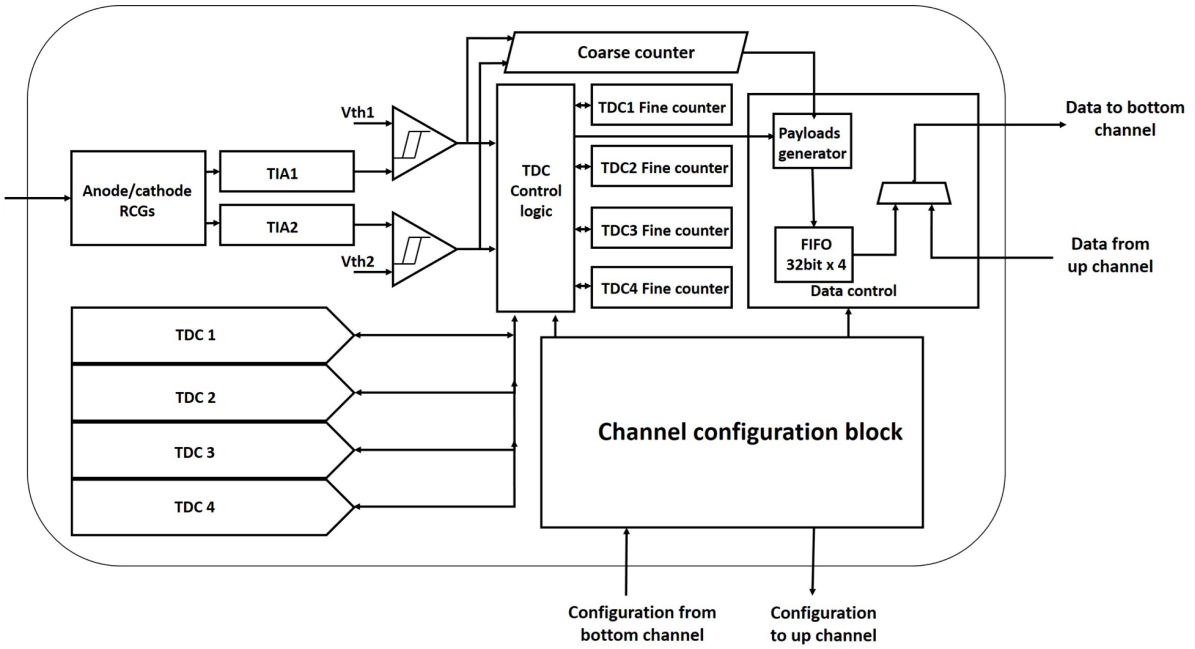
Column ID	Pixel ID	Lost event counter	Lost e.w. counter TDC1	Lost e.w. counter TDC2	Lost e.w. counter TDC3	Lost e.w. counter TDC4	SEU counter
3 bits	3 bits	6 bits	4 bits	4 bits	4 bits	4 bits	4 bits

31 0

- 64-bit (32-bit on time tagging mode) event and status data is generated on-pixel and propagated down the column
- End of Column collects digitised data from pixels and transmits it off-chip using (up to) 4 LVDS Tx links
- End of Column provides also configuration (and analogue bias) to the pixel "matrix"

Pixel floorplan and Architecture

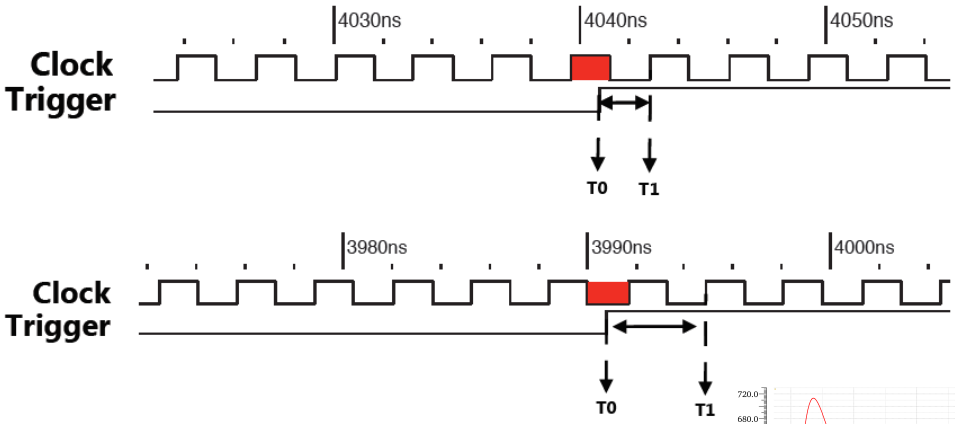


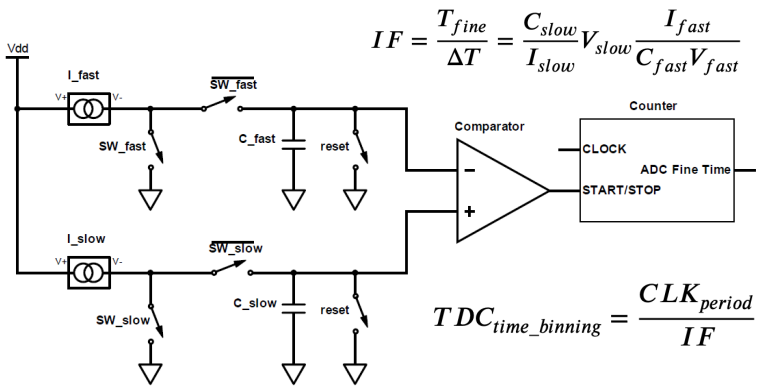


- dual-polarity RCG-based preamplifier: high bandwidth and low input-impedance (10-20 Ω)
- 2 independent post-amp branches and 4 gain settings
- Dual leading edge discriminators with independent (and per pixel) threshold settings (6-bit DAC)
- Pixel control logic handles quad-TDC operation, pixel configuration and data transmission

Time-to-Digital Converters

- A coarse time stamp is extracted from the system clock running at 320 MHz
- A Low-power Analogue interpolation TDC measures phase between event trigger (T0) and clock (T1)

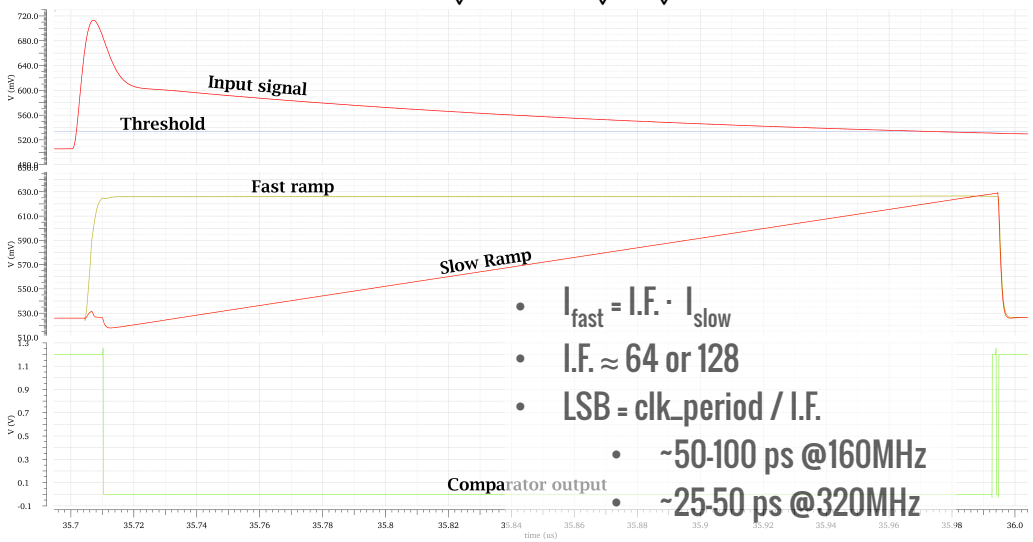




$$IF = \frac{T_{fine}}{\Delta T} = \frac{C_{slow}}{I_{slow}} V_{slow} \frac{I_{fast}}{C_{fast} V_{fast}}$$

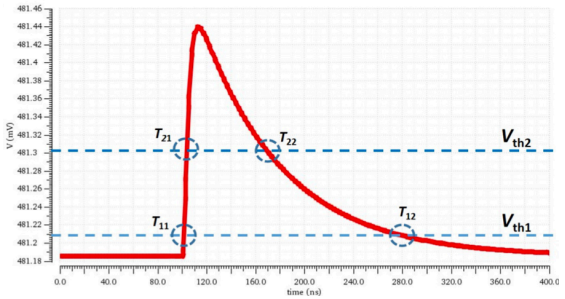
$$TDC_{time\_binning} = \frac{CLK_{period}}{IF}$$

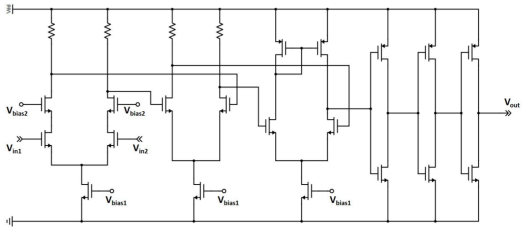
- The phase between event trigger and clock is encoded with a Time-to-Analogue Converter (TAC)
- A Wilkinson ADC is then used to digitise the voltage, generating the fine time information (Tfine)

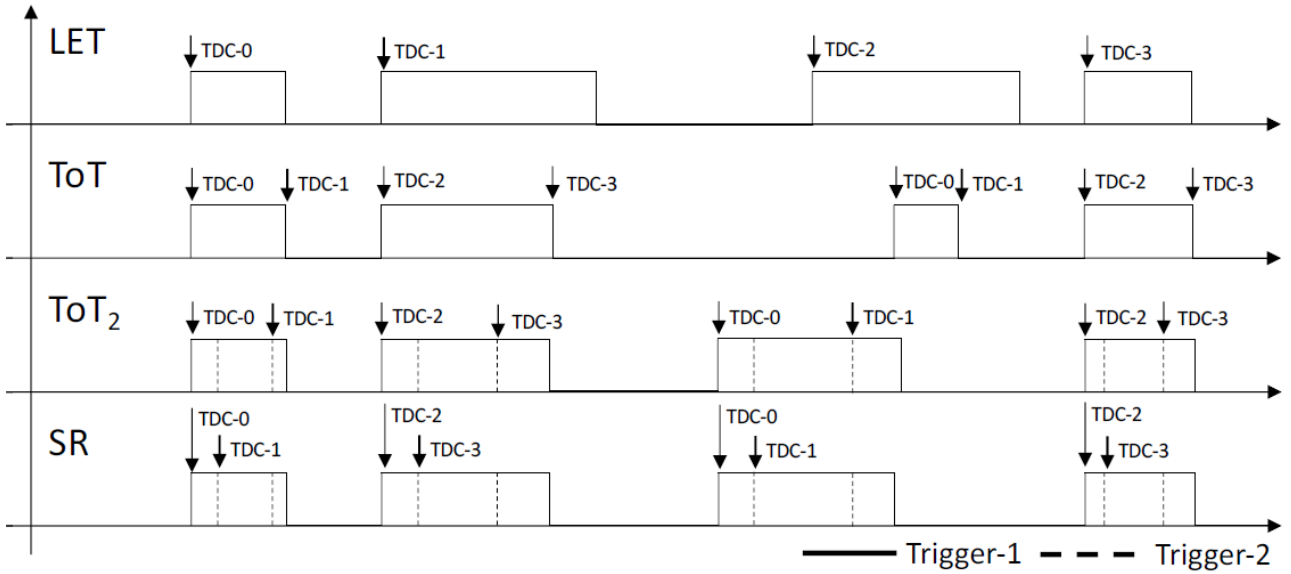


- I_{fast} = I.F. · I_{slow}
- I.F. ≈ 64 or 128
- LSB = clk_period / I.F.
  - ~50-100 ps @160MHz
  - ~25-50 ps @320MHz

Pixel Operation Modes



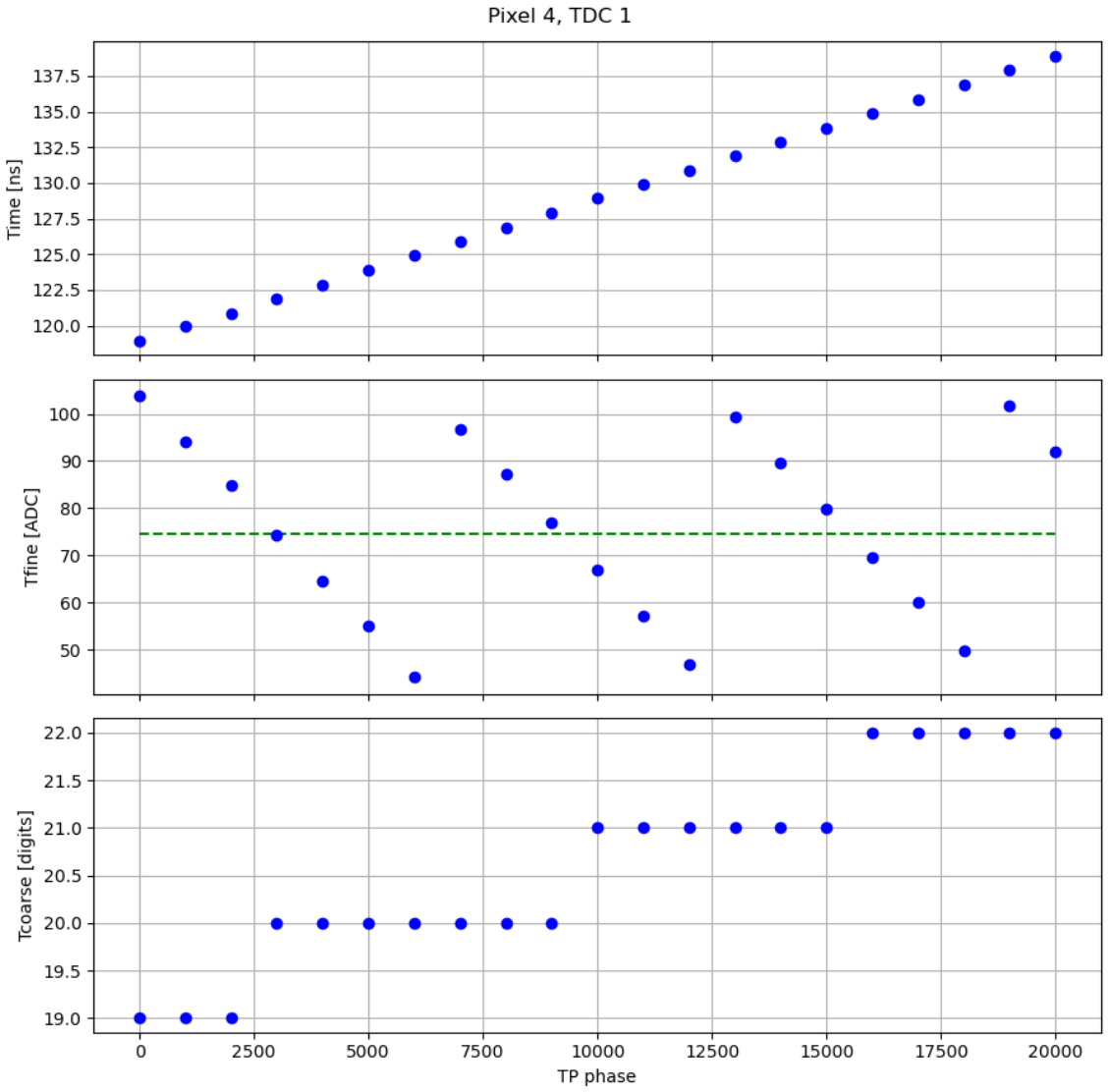




- **LET** leading edge threshold measurement, high-rate time-stamp architecture
- **TOT** Time-over-Threshold (selectable branch for falling edge measurement)
- **SR** slew-rate measurement for signal shape characterisation
- Pixel can be disabled, in normal (trigger less) acquisition mode or can be triggered by a test-pulse,
  - either generated by the on-chip calibration circuitry or propagated from the DAQ,
  - either injecting a configurable charge to the front-end or triggering asynchronously the pixel logic for characterisation and calibration of the TDCs

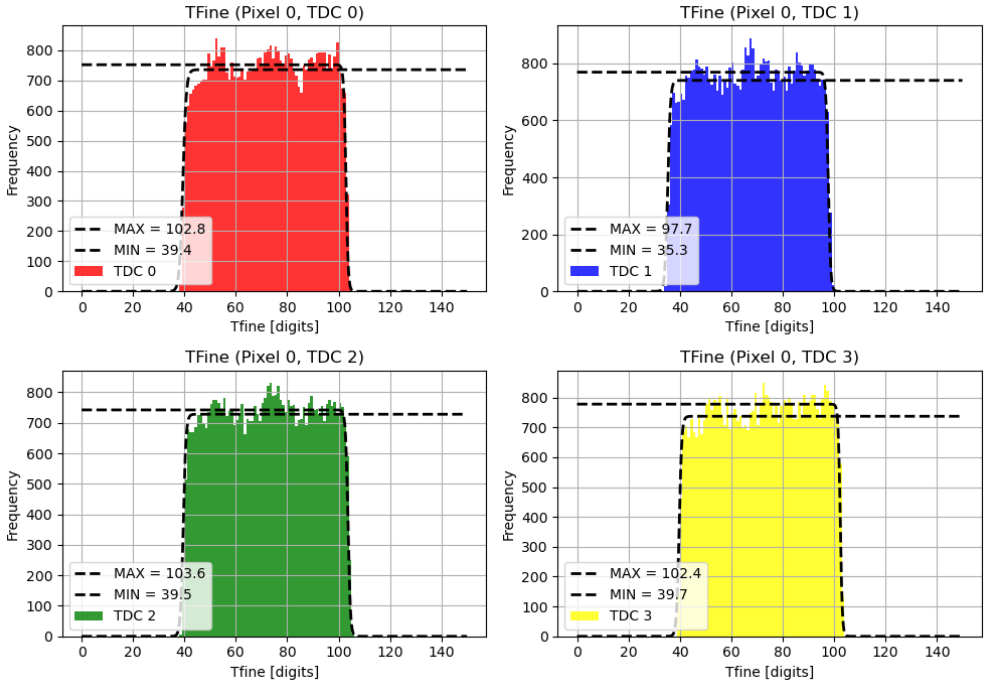
Calibration of the TDCs with Test Pulse

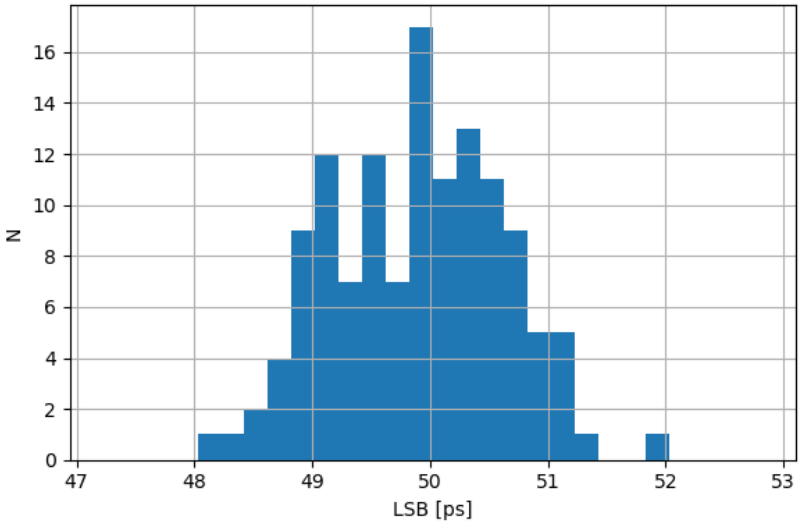
- 20 ns digital test-pulse phase scan
- Extract Tfine MIN and MAX for each TDC of each pixel, save (32 pixels x 4 TDCs) 128 entries LUT
  - IF = MAX - MIN
  - LSB = clk_period / I.F. ≈ 50 ps
  - CUT = (MAX + MIN) / 2
- Apply calibration for each event:
  - Time [ns] = Tcoarse· clk_period - (Tfine – MIN)· LSB (if Tfine < CUT)
  - Time [ns] = Tcoarse· clk_period - (Tfine – MIN)· LSB + clk_period (if Tfine > CUT)
- Tfine points across the CUT region may have a shift of 1 clock period



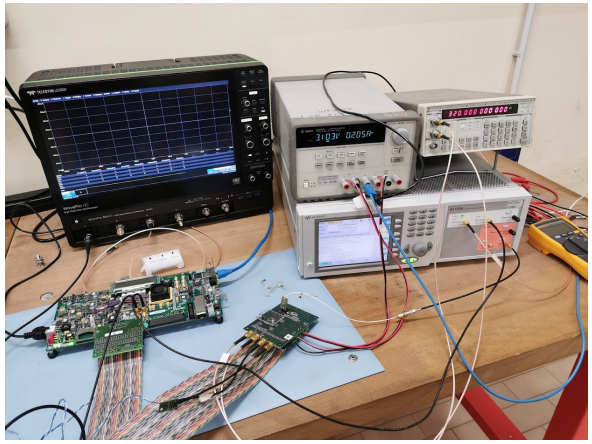
Calibration of the TDCs with DCR

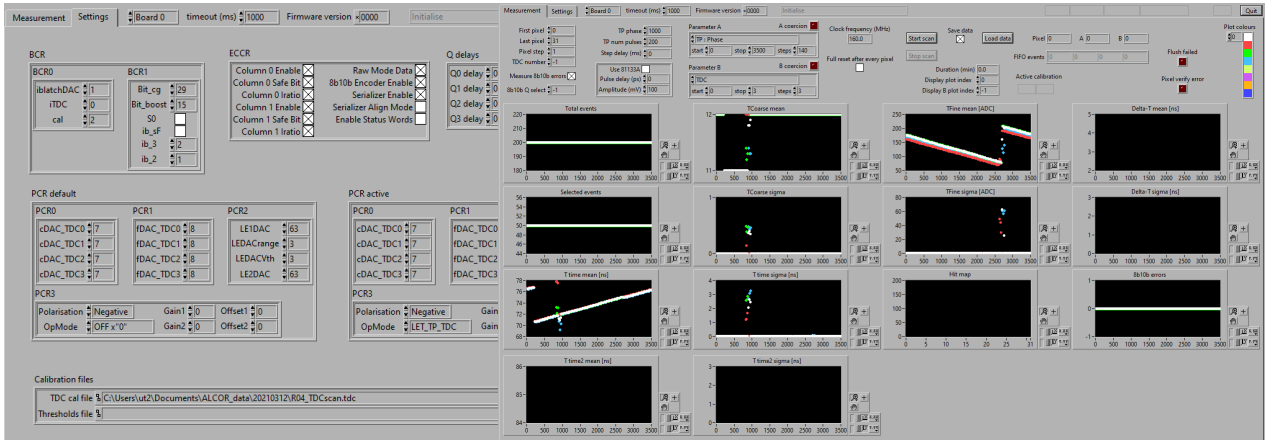
TDCs calibration can be performed also using data from a run with SiPMs collecting Tfine payload from dark counts events.

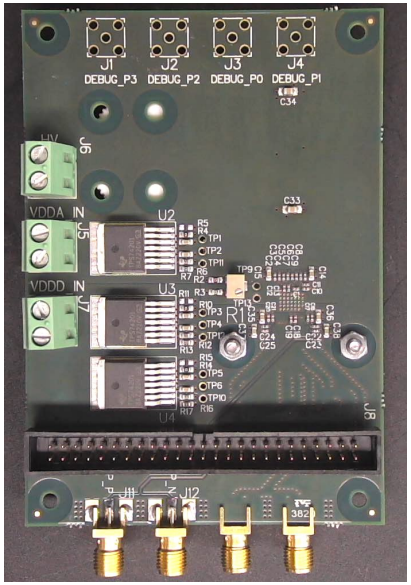


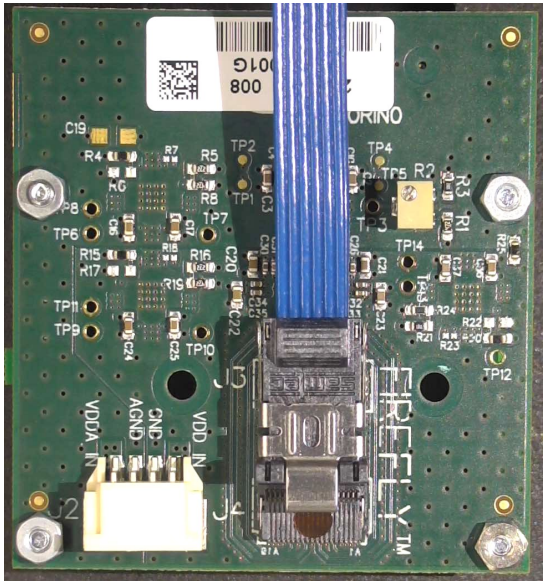


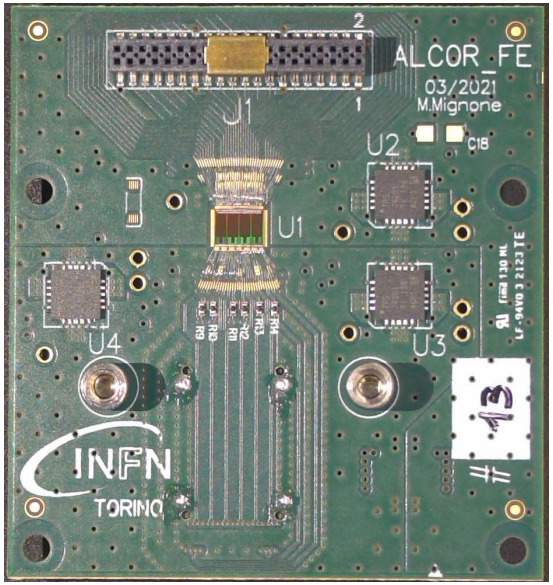
ALCOR FEBs and test environment





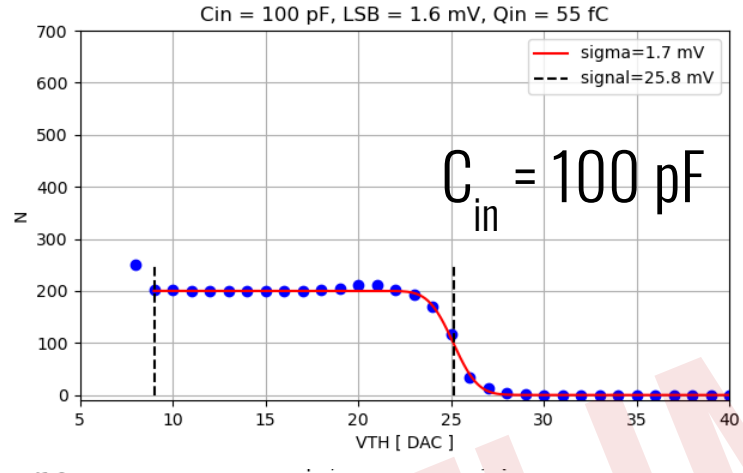


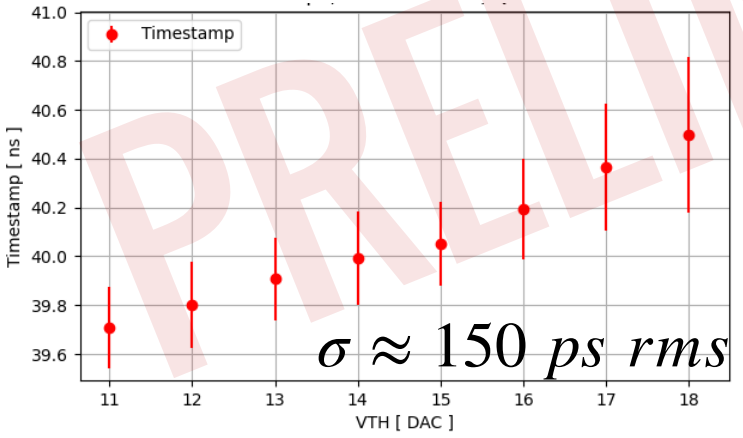


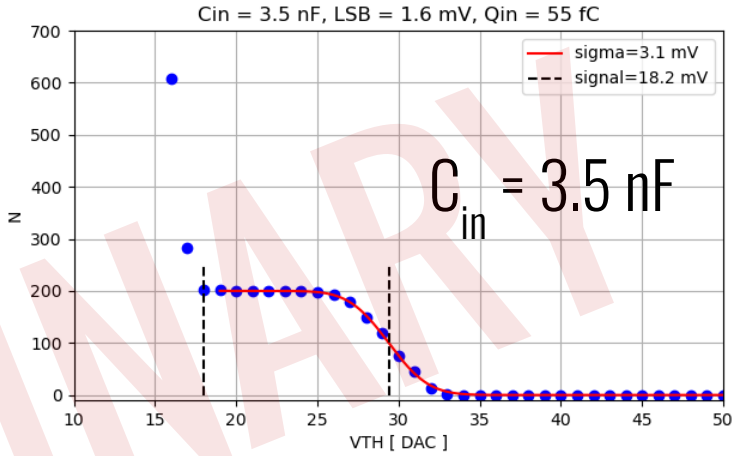


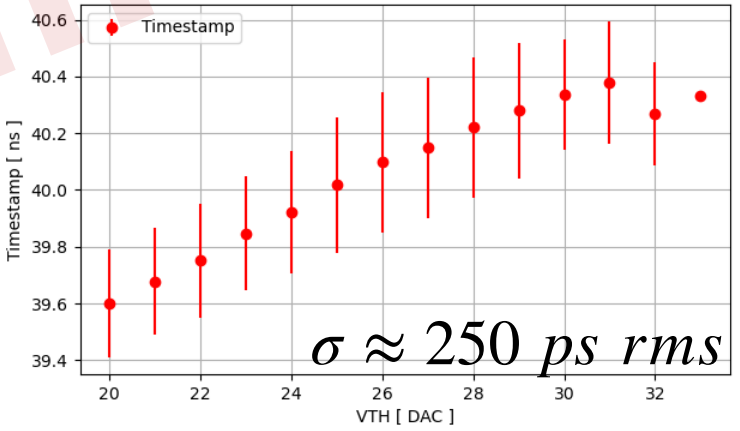
Intrinsic time resolution

- Repeated test-pulses (N=200) using on-chip calibration circuit, external capacitor mounted on one ALCOR channel
- Vth scan to evaluate noise and time resolution
- Note: contribution to noise and time resolution from test-pulse generator still to be disentangled. Room temperature.

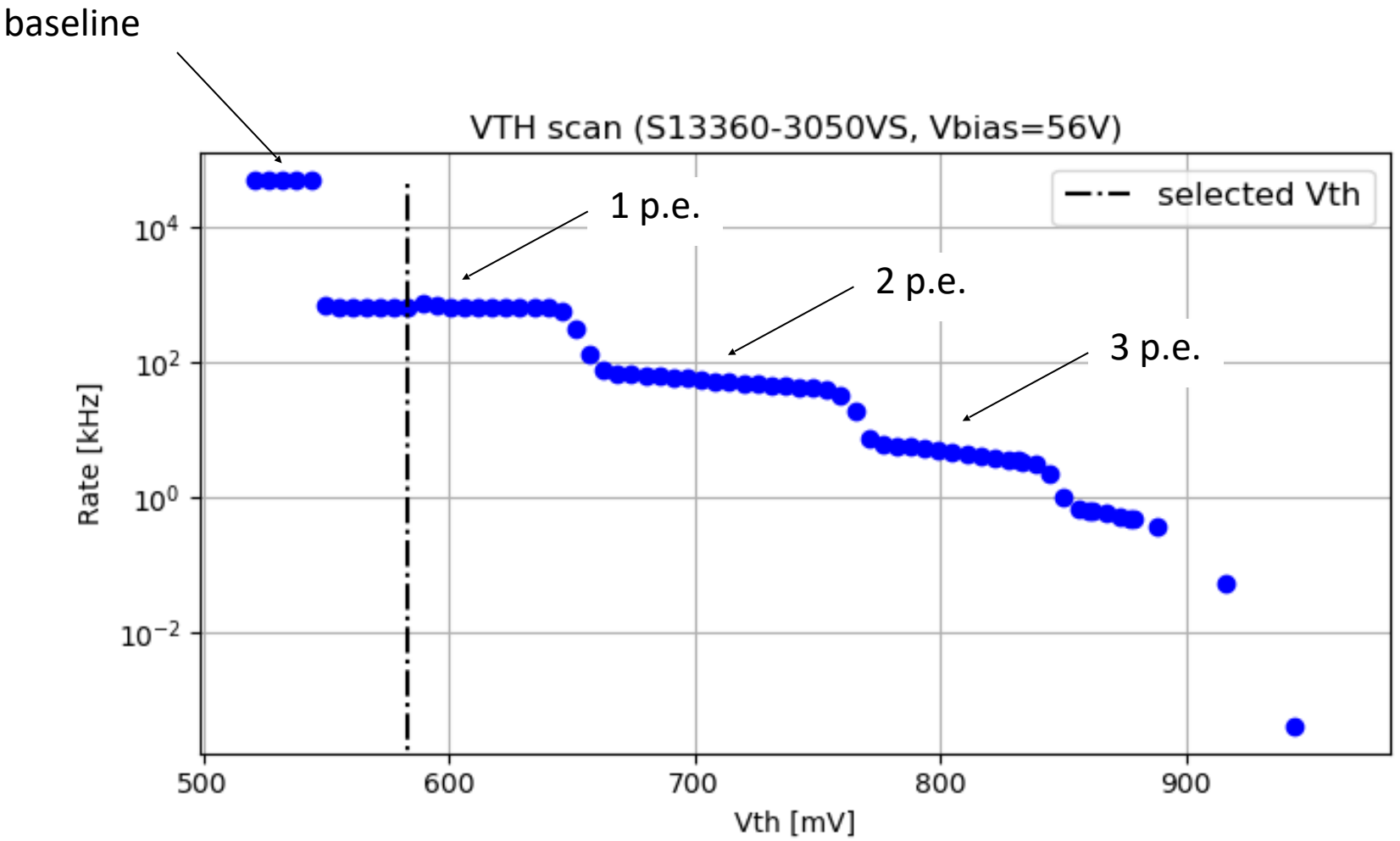








Threshold scan with SiPMs



Summary and next steps

- ALCOR stems from an INFN R&D as a mixed-signal ASIC for the readout of SiPMs at LAr temperatures. Optimised for cryogenic operation and low power.
- Electrical tests at 77K and RT tests with SiPMs (in the framework of EIC-NET) show good data, first silicon chip is fully functional. First beam test results: up next presented by Simone Vallarino.
- Bug fixing (TDC control logic) and improvements to the design are under way.
- Optimised version **ALCOR-EIC** scheduled for tapeout by mid-2022: features higher amplifier gain, revision of front-end circuit (AC coupling), increased TDC rate capability.
- Future R&D towards advanced integration solutions: Flip Chip on Board (FCOB).

The ALCOR ASIC for EIC applications

Thank You for your time!

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